# LF198/298/398

## *Monolithic Sample and Hold Circuits*

### Distinctive Characteristics

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at $C_h$ = 0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth



### GENERAL DESCRIPTION

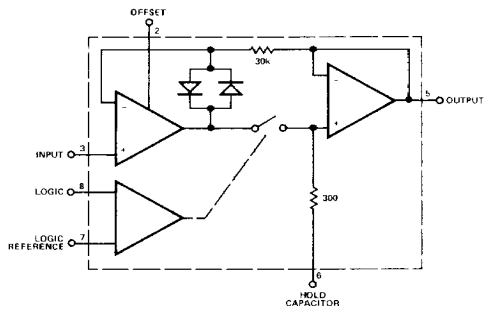
The LF198/LF298/LF398 are BI-FET monolithic sample and hold circuits with ultra-high DC accuracy, fast acquisition time (6μs to 0.01%) and low droop rate. A bipolar input stage is used to obtain the lowest possible offset voltage and wide bandwidth. These circuits are designed to have high common mode rejection and a gain accuracy of 0.002%. High input impedance ($10^{10}\Omega$) permits their use with a high impedance source without degrading accuracy.

The output buffer has a p-channel JFET input with a typical input current of 30pA, giving a droop rate as low as 5mV/Min with a 1μF hold capacitor. The JFET has a very low noise level and high temperature stability.

A differential logic input allows the logic to be referenced to a separate ground from analog ground, permitting a direct interface to nearly any logic family. The LF198 series guarantees no feed through in the hold mode including input signal swings equal to the power supply.

The LF198A series has tightened electrical specifications.

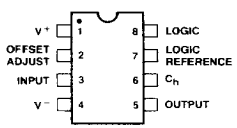
### FUNCTION DIAGRAM



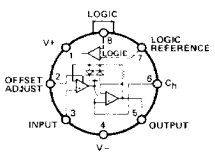

LIC-204

### CONNECTION DIAGRAMS – Top Views

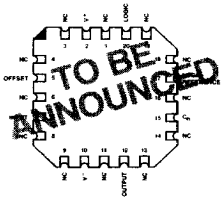
**P-8-1**




**H-8-1**




**L-20-1**




LIC-205

### ORDERING INFORMATION

| Part Number | Package Type | Temperature Range | Order Number |
|---|---|---|---|
| LF398 | Metal Can | 0 to +70°C | LF398H |
| | Plastic | 0 to +70°C | LF398N |
| | Leadless | 0 to +70°C | LF398L** |
| | Dice | 0 to +70°C | LD398 |
| LF298 | Metal Can | −25 to +85°C | LF298H |
| | Leadless | −25 to +85°C | LF298L** |
| LF198* | Metal Can | −55 to +125°C | LF198H |
| | Leadless | −55 to +125°C | LF198L** |
| | Dice | −55 to +125°C | LD198 |

*Also available with burn-in processing. To order add suffix B to part number.
**To be announced.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating Ambient Temperature Range<br>LF198/LF198A | −55°C to +125°C |
| LF298 | −25°C to +85°C |
| LF398/LF398A | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Power Dissipation (Package Limitation, Note 1) | 500mW |
| Derate above 25°C | 6.8mW/°C |
| Supply Voltage | ±18V |
| Input Voltage | Equal to Supply Voltage |
| Logic to Logic Reference Differential Voltage (Note 2) | +7V, −30V |
| Hold Capacitor Short Circuit Duration | 10 sec |
| Lead Temperature (Soldering 10 seconds) | 300°C |

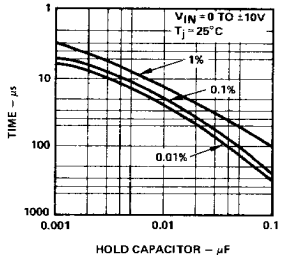
## ELECTRICAL CHARACTERISTICS (Note 3)

| Parameter | Test Conditions | LF198/LF298 Min. | LF198/LF298 Typ. | LF198/LF298 Max. | LF398 Min. | LF398 Typ. | LF398 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage, (Note 6) | $T_j = 25°C$ | | 1 | 3 | | 2 | 7 | mV |
| | Full Temperature Range | | | 5 | | | 10 | mV |
| Input Bias Current, (Note 6) | $T_j = 25°C$ | | 5 | 25 | | 10 | 50 | nA |
| | Full Temperature Range | | | 75 | | | 100 | nA |
| Input Impedance | $T_j = 25°C$ | | $10^{10}$ | | | $10^{10}$ | | Ω |
| Gain Error | $T_j = 25°C$, $R_L = 10k\Omega$ | | 0.002 | 0.005 | | 0.004 | 0.01 | % |
| | Full Temperature Range | | | 0.02 | | | 0.02 | % |
| Feedthrough Attenuation Ratio at 1 kHz | $T_j = 25°C$, $C_h = 0.01\mu F$ | 86 | 96 | | 80 | 90 | | dB |
| Output Impedance | $T_j = 25°C$, "HOLD" mode | | 0.5 | 2 | | 0.5 | 4 | Ω |
| | Full Temperature Range | | | 4 | | | 6 | Ω |
| "HOLD" Step, (Note 4) | $T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$ | | 0.5 | 2.0 | | 1.0 | 2.5 | mV |
| Supply Current, (Note 6) | $T_j \geq 25°C$ | | 4.5 | 5.5 | | 4.5 | 6.5 | mA |
| Logic and Logic Reference Input Current | $T_j = 25°C$ | | 2 | 10 | | 2 | 10 | μA |
| Leakage Current into Hold Capacitor (Note 6) | $T_j = 25°C$, (Note 5)<br>Hold Mode | | 30 | 100 | | 30 | 200 | pA |
| Acquisition Time to 0.1% | $\Delta V_{OUT} = 10V$, $C_h = 1000$ pF | | 4 | | | 4 | | μs |
| | $C_h = 0.01\mu F$ | | 20 | | | 20 | | μs |
| Hold Capacitor Charge Current | $V_{IN} - V_{OUT} = 2V$ | | 5 | | | 5 | | mA |
| Supply Voltage Rejection Ratio | $V_{OUT} = 0$ | 80 | 110 | | 80 | 110 | | dB |
| Differential Logic Threshold | $T_j = 25°C$ | 0.8 | 1.4 | 2.4 | 0.8 | 1.4 | 2.4 | V |

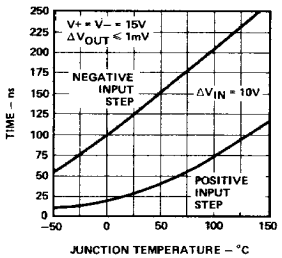
Notes:
1. The maximum junction temperature is 150°C for the LF198, 115°C for the LF298, and 100°C for the LF398. When used at a higher ambient temperature the metal can package must be derated based on a thermal resistance ($\theta jA$) of 150°C/W. Derate N package 5.6mW/°C above 36°C.
2. The differential voltage may not exceed this limit. The common mode voltage on the logic pins may equal the supply voltage without causing damage to the device. For the LF198 to operate properly, one of the logic pins must be at least 2V below the positive supply and 3V above the negative supply.
3. The following conditions apply unles otherwise noted: Device is in "sample mode." $T_j = 25°C$, $V_S = \pm 15V$, $-11.5V < V_{IN} < +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V. Logic input voltage = 2.5V.
4. The hold step is produced by a charge which is coupled from the logic input signal to the hold capacitor via parasitic capacitance and internal operating point changes. Stray capacitance equal to 1pF will create a 0.5mV step with a 5 volt logic swing and a 0.01μF hold capacitor. This step can be reduced by increasing the magnitude of the hold capacitor.
5. Leakage current is measured at a junction temperature of 25°C. The junction temperature doubles the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over the full input signal range.
6. These values are guaranteed over the ±5 to ±18V supply range.

## TYPICAL PERFORMANCE CHARACTERISTICS

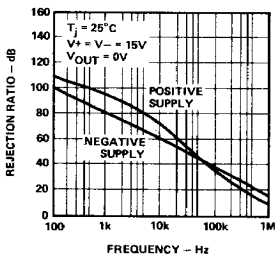
**Acquisition Time**



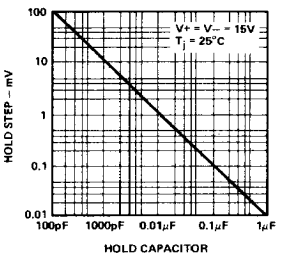

**Aperture Time**



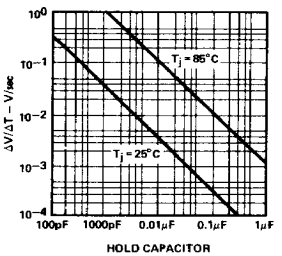

**Power Supply Rejection**



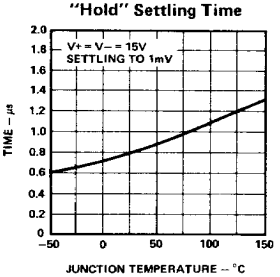

**Hold Step**



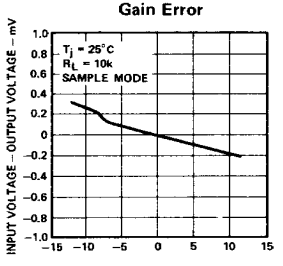

**Output Droop Rate**



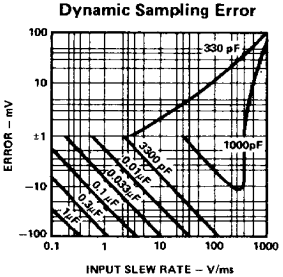

**"Hold" Settling Time**



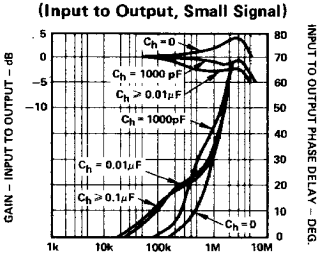

**Gain Error**



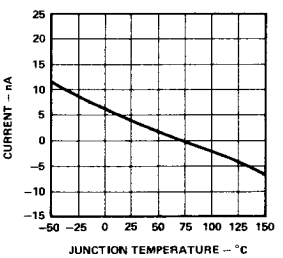

**Dynamic Sampling Error**



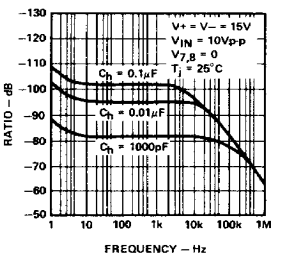

**Phase and Gain (Input to Output, Small Signal)**



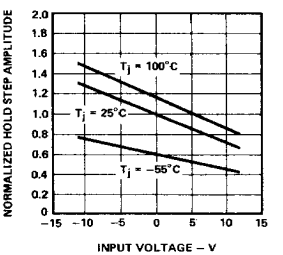

**Input Bias Current**




**Feedthrough Rejection Ratio (Hold Mode)**



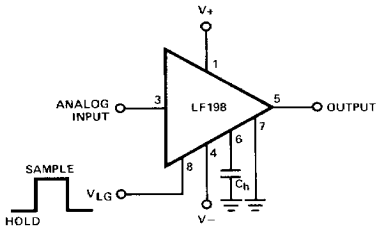

**Hold Step Versus Input Voltage**




LIC-206

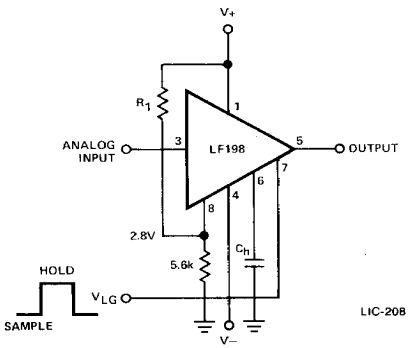
## LOGIC INPUT CONFIGURATIONS

### TTL AND CMOS
### $3V \leq V_{LG}(HI\ STATE) \leq 7V$




LIC-207

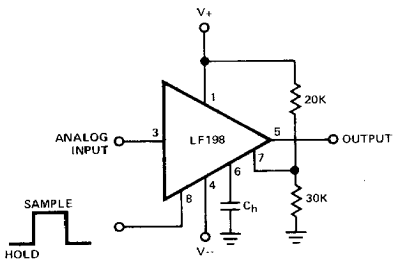
Threshold = 1.4V




LIC-208

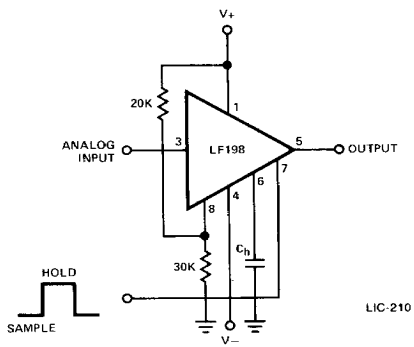
Threshold = 1.4V
$R_1$ select for 2.8V at Pin 8

### CMOS
### $7V \leq V_{LG}(HI\ STATE) \leq 15V$




LIC-209

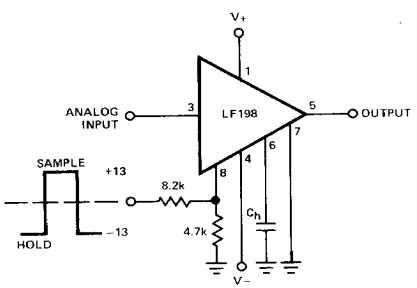
Threshold = 0.6 (V+) + 1.4V




LIC-210

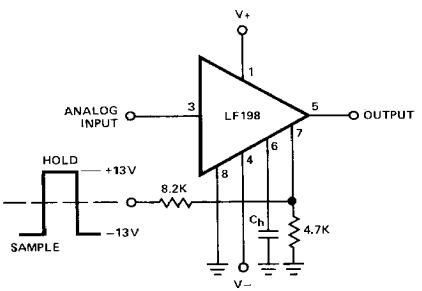
Threshold = 0.6 (V+) − 1.4V

### OP AMP DRIVE
### OUTPUT VOLTAGE = ±13V




LIC-211

Threshold ≈ 4V




LIC-212

Threshold = −4V

## APPLICATION INFORMATION

Freezing the input to an analog-to-digital (A/D) converter is an important application for the sample and hold amplifier. If the analog input to the A/D changes during conversion by the amount ±1/2LSB, an ideal A/D would produce 1 LSB error beyond normal quantization error. A sample and hold amplifier eliminates this problem by holding the input signal to the A/D converter during the conversion interval. The proper choice of hold capacitor value and type is necessary to obtain optimum performance. The capacitor value directly affects several circuit parameters, particularly acquisition time, droop rate, and hold step. The hold step error is inversely proportional to the value of the hold capacitor.

Graphs are provided in this data sheet for use as guides in selecting a suitable value of capacitance. However, the capacitor should have extremely high insulation resistance and low dielectric absorption, or dielectric hysteresis. Polypropylene (below +85°C) and Teflon (above +85°C) types are recommended. The hysteresis error can be significantly reduced if the output of the LF198 is digitized immediately after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10-50ms, thus if A/D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

The logic inputs on the LF198 are fully differential with low input current and will operate from TTL levels up to 15V. Some typical logic input configurations are shown in this data sheet. The logic signal into the LF198 must have a minimum slew rate of 0.2V/μs. Slower signals cause excess hold step errors.

When switched from sample to hold, delay in response to the hold command (aperture time and aperture time uncertainty) can cause the frozen value of a fast moving waveform to differ from the value it had at the instant the hold command is given. However, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip which cancels out some of the error due to aperture time and aperture time uncertainty.

For example, using an analog input of 20 volts p-p at 10kHz, maximum slew rate 0.5V/μs, with no phase delay and 80ns logic delay, one could expect up to (0.08μs) • (0.5V/μs) = 40mV error if the input is sampled during the maximum dv/dt period. A positive going input would give a +40mV error. Assume that the slew rate of the charging amplifier and the RC constant of the analog loop cause a delay of 120ns. If the hold capacitor sees this exact delay, then the analog delay would be (0.5μV/sec)•(.12μs) = −60mV. Total output error is +40mV −60mV = −20mV.

For a sample and hold amplifier in a multiplexed A/D system, acquisition and aperture times are critical parameters. In order to maintain the acquired signal level within the specified accuracy, these times must be considered when selecting the sampling rate. For example, if a 16 channel MUX drives a sample and hold amplifier in which each channel is 5KHz and 2 samples per cycle are needed to satisfy the Nyquist criteria, the minimum sampling rate = 160000 samples/sec. ((5KHz X 16) cycles/sec X 2 samples/cycle). The minimum channel period is the reciprocal of the sampling rate of 6.25μs. During the hold mode the MUX can switch to another channel. This eliminates the need to consider the MUX and source settling time and shortens the channel period.

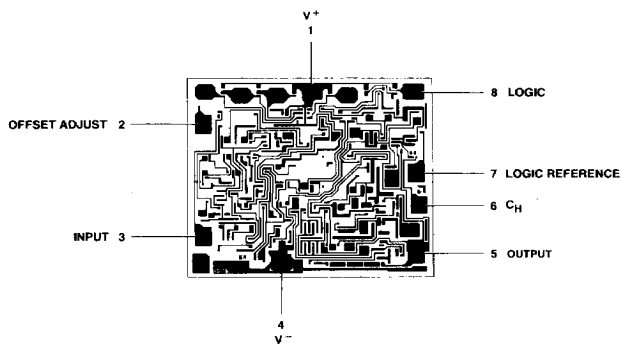
Calculating the sum of the sample and hold acquisition time, aperture time and A/D conversion time is usually a convenient method for estimating maximum channel period.

In multiplex applications, sample and hold feed-through is a significant problem. Since each channel voltage differs, the sample and hold input signal becomes a series of varied height pulses that cause errors in the sample and hold voltage.

Digital feed through occurs when a fast rising logic signal is coupled into the analog input. To minimize it, the logic signal trace in the PCB layout should be kept as far as possible from the analog input. Guarded trace may also be used around the input pin for shielding purposes.

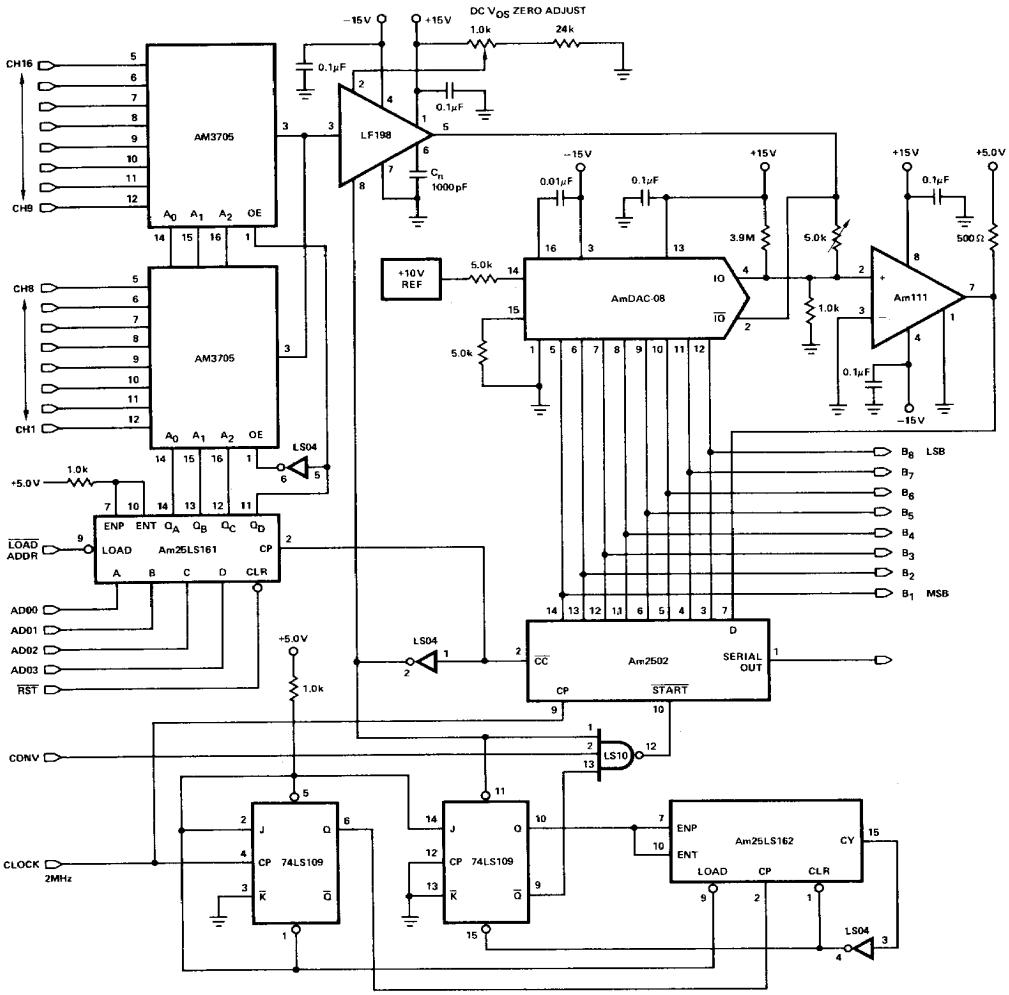
To adjust the DC offset zeroing, the wiper of a 1K potentiometer is connected to the offset adjust pin. One end of the potentiometer is connected to VCC and the other is connected through a resistor to ground. The value of the resistor is selected such that the current flows through it at approximately 6mA.

**Metallization and Pad Layout**

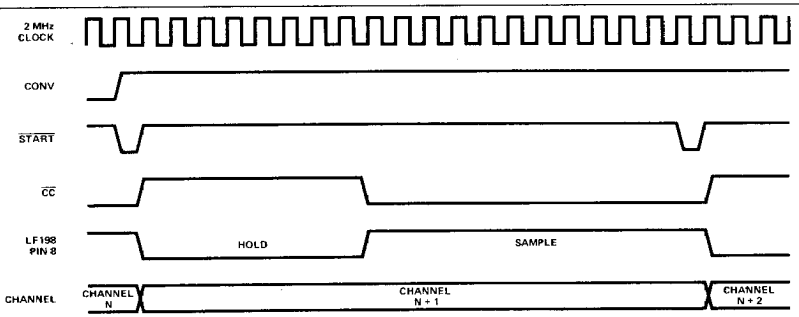



DIE SIZE: 0.051" X 0.070"

## APPLICATIONS

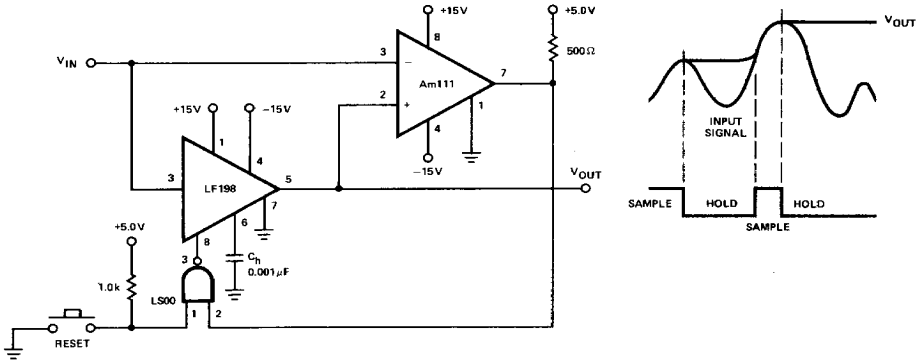



SEQUENTIAL ADDRESSING OVERLAP MODE A/D CONVERSION LIC-213



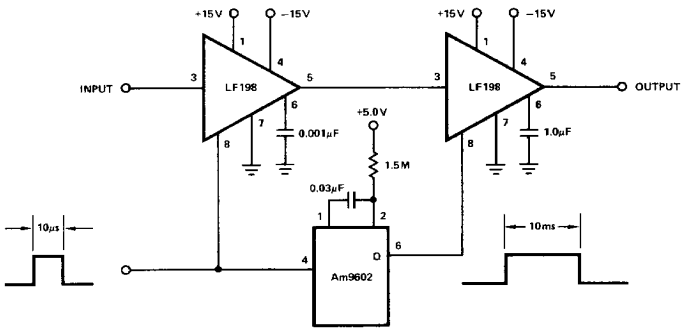

TIMING DIAGRAM FOR SEQUENTIAL ADDRESSING OVERLAP MODE A/D CONVERSION LIC-214

## APPLICATIONS (Cont.)




TRACK AND HOLD PEAK RECORDER

LIC-215




FAST ACQUISITION, LOW DROOP SAMPLE AND HOLD

LIC-216

### DEFINITION OF TERMS

**Acquisition Time** – The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

**Aperture time** – The delay between the command to hold and the actual opening of the hold switch.

**Aperture time uncertainty** – The tolerance, or jitter of the aperture time.

**Droop rate** – The rate of change of output voltage in the hold mode. It is caused by leakage currents at the hold capacitor node.

**Feed-through** – During hold, a small part of the input signal feeds through the capacitor of the switch to the hold capacitor and output. This is usually a function of the level and frequency of the input signal and is expressed in dB.

**Dynamic sampling error** – The error introduced into the outputs due to input voltage varying when the hold command is issued. Error is expressed in mV with a given hold capacitor.

**Gain error** – The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

**Hold step** – The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage.