Magellan™ Motion Processor

MC55000

Electrical Specification

for Pulse and Direction Motion Control

Preliminary

P M D
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Related Documents

MC50000 Motion Processor User's Guide (MC50000UG)

How to set up and use all members of the MC50000 Motion Processor family.

MC50000 Motion Processor Programmer's Command Reference (MC50000PR)

Descriptions of all MC50000 Motion Processor commands, with coding syntax and examples, listed alphabetically for quick reference.

MC50000 Motion Processor Electrical Specifications

Three booklets containing physical and electrical characteristics, timing diagrams, pinouts, and pin descriptions of each:

MC55000 Series, for stepping motion control (MC55000ES);
MC58000 Series, for brushed and brushless servo, microstepping and stepping motion control (MC58000ES).

MC50000 Motion Processor Developer's Kit Manual (DK50000M)

How to install and configure the DK50000 developer's kit PC board.

Table of Contents

1 The MC50000 Family

	MC55020 Series	MC58020 Series	MC55110	MC58110
Number of axes	4,3,2 or 1	4,3,2 or 1	1	1
Number of chips	2 (CP and IO)	2 (CP and IO)	1 (CP)	1 (CP)
Motor type	Stepping	Brushed DC servo Brushless DC servo Stepping	Stepping	Brushed DC servo Brushless DC servo Stepping
Output format	Pulse and direction	Brushed single phase Sinusoidal commutation Microstepping Pulse and direction	Pulse and direction	Brushed single phase Sinusoidal commutation Microstepping Pulse and direction
Communication interface				
Parallel	√	√	√	√
Asynchronous serial	√	√	√	√
CAN 2.0B	√	√	√	√
Position input				
Incremental encoder input	√	√	√	√
Parallel word device input	√	√	√	√
Index & Home signals	√	√	√	√
Position capture	√	√	√	√
Directional limit switches	√	√	√	√
Motor command output				
PWM output	-	√	-	√
Parallel DAC output	-	√	-	√
SPI DAC output	-	√	-	√
Trajectory generation				
Pulse & direction output	√	√	√	√
Trapezoidal profiling	√	√	√	√
S-curve profiling	√	√	√	√
Velocity profiling	√	√	√	√
Electronic gearing	√	√	√	√
On-the-fly changes	√	√	√	√
Servo filter				
PID position loop	-	√	-	√
Dual encoder loop	-	√	-	√
Derivative sampling time	-	√	-	√
Feedforward (accel & vel)	-	√	-	√
Dual bi-quad filter	-	√	-	√

	MC55020 Series	MC58020 Series	MC55110	MC58110
		Miscellaneous		
Data trace/diagnostics	√	√	√	√
Motion error detection	√ (with encoder)	√	√ (with encoder)	√
Axis settled indicator	√ (with encoder)	√	√ (with encoder)	√
Analog input	√	√	√	√
Programmable bit output	√	√	√	√
Software-invertible signals	√	√	√	√
User-defined I/O	√	√	√	√
External RAM support	√	√	√	√
Multi-chip synchronization	√	√	√	√
Chipset part numbers	MC55120 MC55220 MC55320 MC55420	MC58120 MC58220 MC58320 MC58420	MC55110	MC58110
Developer's Kit p/n's:	DK55420	DK58420	DK55110	DK58110

Introduction

This manual describes the operational characteristics of the MC55000 Series Motion Processors from PMD. These devices are members of PMD's third-generation motion processor family.

Each of these devices is a complete chip-based motion processor. They provide trajectory generation, related motion control functions and high-speed pulse and direction outputs. Together these products provide a software-compatible family of dedicated motion processors that can handle a large variety of system configurations.

Each of these chips utilize a similar architecture, consisting of a high-speed computation unit, along with an ASIC (Application Specific Integrated Circuit). The computation unit contains special on-board hardware that makes it well suited for the task of motion control.

Along with similar hardware architecture these chips also share most software commands, so that software written for one series may be re-used with another, even though the type of motor may be different.

Family Summary

MC55000 Series – These chipsets provide high-speed pulse and direction signals for step motor systems. For the MC55020 series two TQFP ICs are required: a 100-pin Input/Output (IO) chip, and a 144-pin Command Processor (CP) chip, while the MC55110 has all functions integrated into a single chip a 144-pin Command Processor (CP) chip.

MC58000 Series – This series outputs motor commands in Sign/Magnitude PWM or DAC-compatible format for use with DC-Brush motors or Brushless DC motors having external commutation; two-phase or three-phase sinusoidally commutated motor signals in PWM or DAC-compatible format for brushless servo motors; pulse and direction output for step motors; and two phase signals per axis in either PWM or DAC-compatible signals for microstepping motors.

For the MC58020 series two TQFP ICs are required: a 100-pin Input/Output (IO) chip, and a 144-pin Command Processor (CP) chip, while the MC58110 has all functions integrated into a single 144-pin CP chip.

1.2 How to Order

When ordering a single-chip configuration, only the CP part number is necessary. For two-IC and multi-axis configurations, both the CP and the IO part numbers are required.

CP (1 or 2 chip configurations)

MC5□ □ □0CP□.□

Motor Type
8 = Multi Motor
5 = Pulse & Direction

 # Axes
1,2,3,4

 # Chips
1 (CP only)
2 (CP & IO)

CP Version
(Call PMD)

IO (2 chip configurations only)

MC50000IO

Developer's Kit

DK5□ □ □0CP□.□50000IO

Motor Type
8 = Multi Motor
5 = Pulse & Direction

 # Axes
1,2,3,4

 # Chips
1 (CP only)
2 (CP & IO)

CP Version
(Call PMD)

2 Functional Characteristics

2.1 Configurations, parameters, and performance

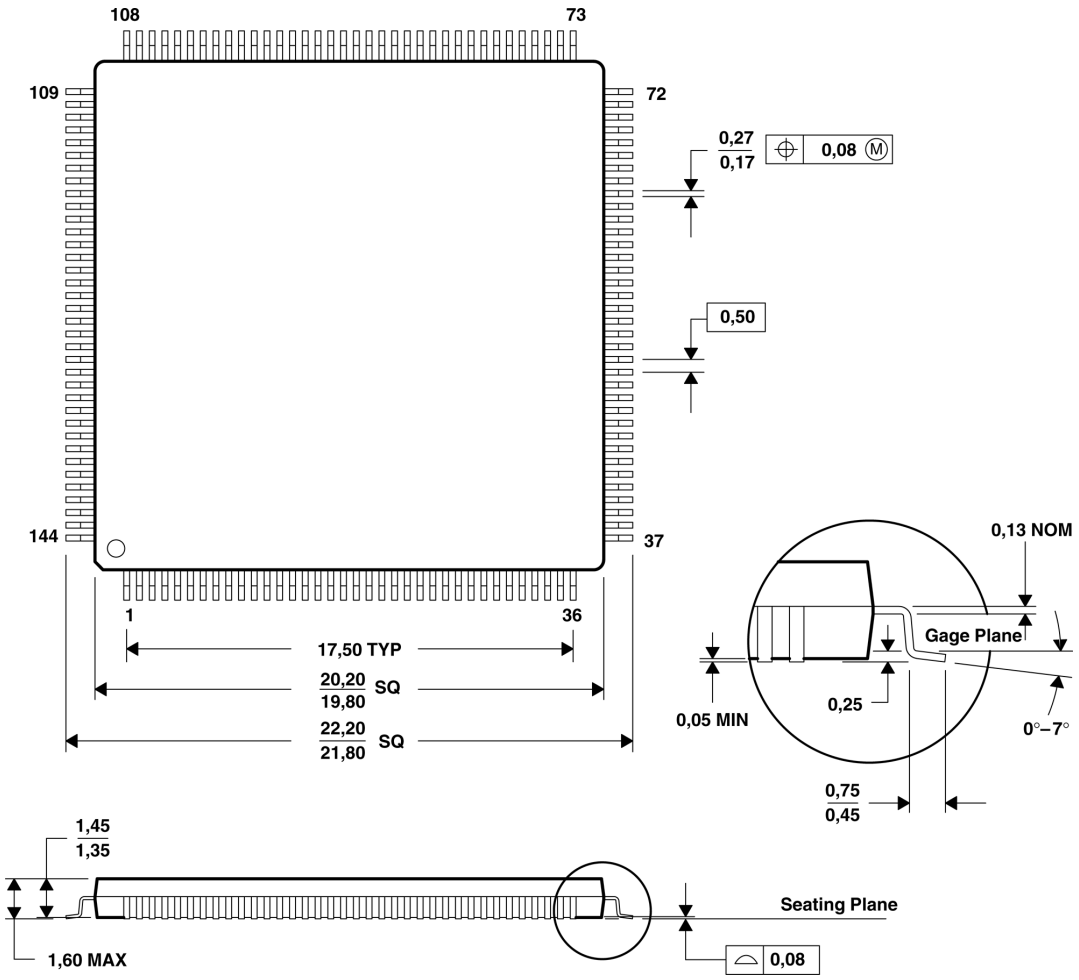
Configuration	4 axes (MC55420)	
	3 axes (MC55320)	
	2 axes (MC55220)	
	1 axis (MC55120 or MC55110)	
Operating modes	Open loop (pulse generator is driven by trajectory generator output, encoder input used for stall detection)	
Communication modes	8/16 parallel	8 bit external parallel bus with 16 bit command word size
	16/16 parallel	16 bit external parallel bus with 16 bit command word size
	Point to point asynchronous serial	
	Multi-drop asynchronous serial	
	CAN bus 2.0B, protocol co-exists with CANOpen	
Serial port baud rate range	1,200 baud to 416,667 baud	
Profile modes	S-curve point-to-point	Velocity, acceleration, jerk, and position parameters
	Trapezoidal point-to-point	Velocity, acceleration, deceleration, and position parameters
	Velocity-contouring	Velocity, acceleration, and deceleration parameters
	Electronic Gear	Encoder or trajectory position of one axis used to drive a second axis. Master and slave axes and gear ratio parameters
	External	All commanded profile parameters are generated by the host and stored in external RAM
Position range	-2,147,483,648 to +2,147,483,647 steps	
Velocity range	-32,768 to +32,767 steps per cycle	
	with a resolution of 1/65,536 steps per cycle	
Acceleration and deceleration ranges	0 to +32,767 steps per cycle[2]	
	with a resolution of 1/65,536 steps per cycle [2]	
Jerk range	0 to ½ steps per cycle [3]	
	with a resolution of 1/4,294,967,296 steps per cycle [3]	
Electronic gear ratio range	-32,768 to +32,767 with a resolution of 1/65,536 (negative and positive direction)	
Position error tracking	Motion error window	Allows axis to be stopped upon exceeding programmable window
	Tracking window	Allows flag to be set if axis exceeds a programmable position window
	Axis settled	Allows flag to be set if axis exceeds a programmable position window for a programmable amount of time after trajectory motion is compete
Motor output modes	Step and Direction (4.98 Mpulses/sec maximum)	
Maximum encoder rate	Incremental (up to 10 Mcounts/sec)	
	Parallel-word (up to 160 Mcounts/sec)	
Parallel encoder word size	16 bits	

Parallel encoder read rate	20 kHz (reads all axes every 50 μsec)
Cycle timing range	51.2 microseconds to 1.048576 seconds
Minimum cycle time	51.2 microseconds
Limit switches	2 per axis: one for each direction of travel
Position-capture triggers	2 per axis: index and home signals
Other digital signals (per axis)	1 AxisIn signal per axis, 1 AxisOut signal per axis
Software-invertable signals	Encoder A, Encoder B, Index, Home, AxisIn, AxisOut, PositiveLimit, NegativeLimit
Analog input	8 10-bit analog inputs
User defined discrete I/O	256 16-bit wide user defined I/O
RAM/external memory support	65,536 blocks of 32,768 16 bit words per block. Total accessible memory is 2,147,483,648 16 bit words
Trace modes	one-time continuous
Maximum number of trace variables	4
Number of traceable variables	19
Number of host instructions	103

2.2 Physical characteristics and mounting dimensions

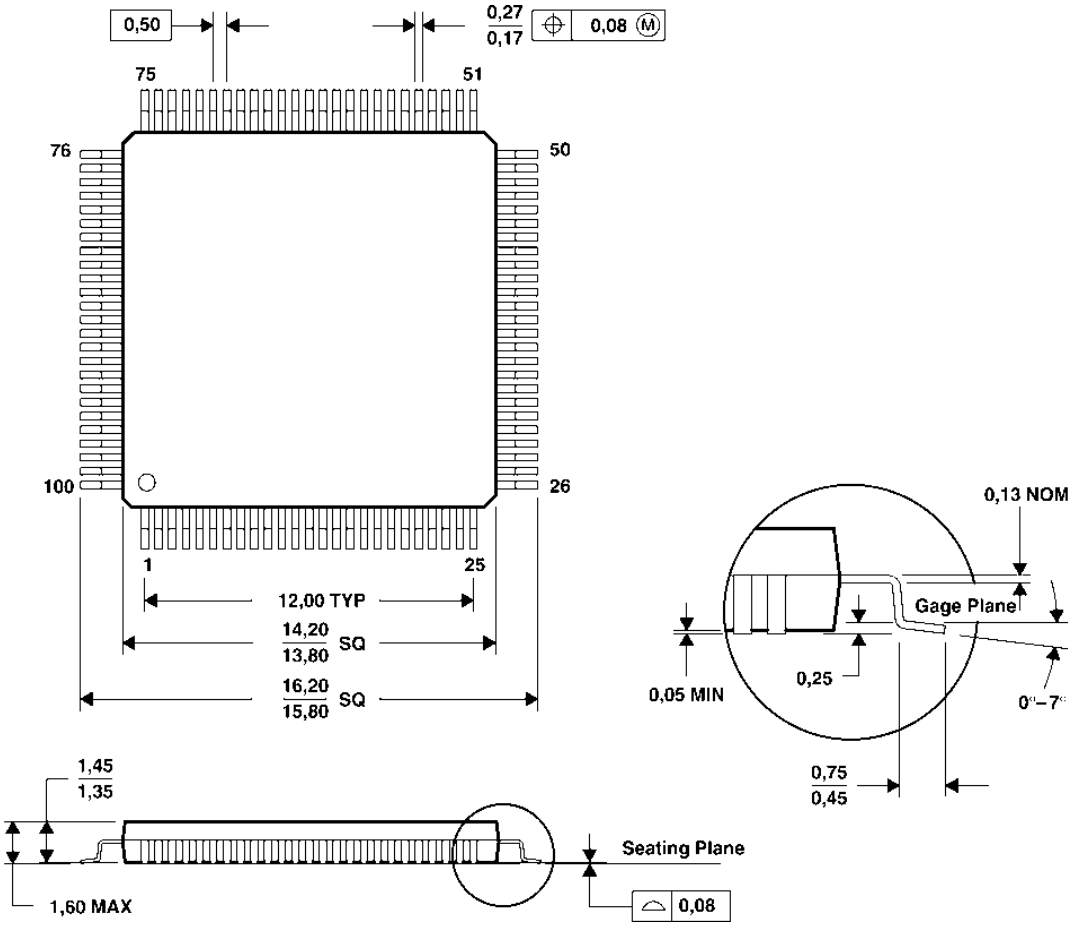
2.2.1 CP chip

All dimensions are in millimeters.



2.2.2 IO chip

All dimensions are in millimeters.

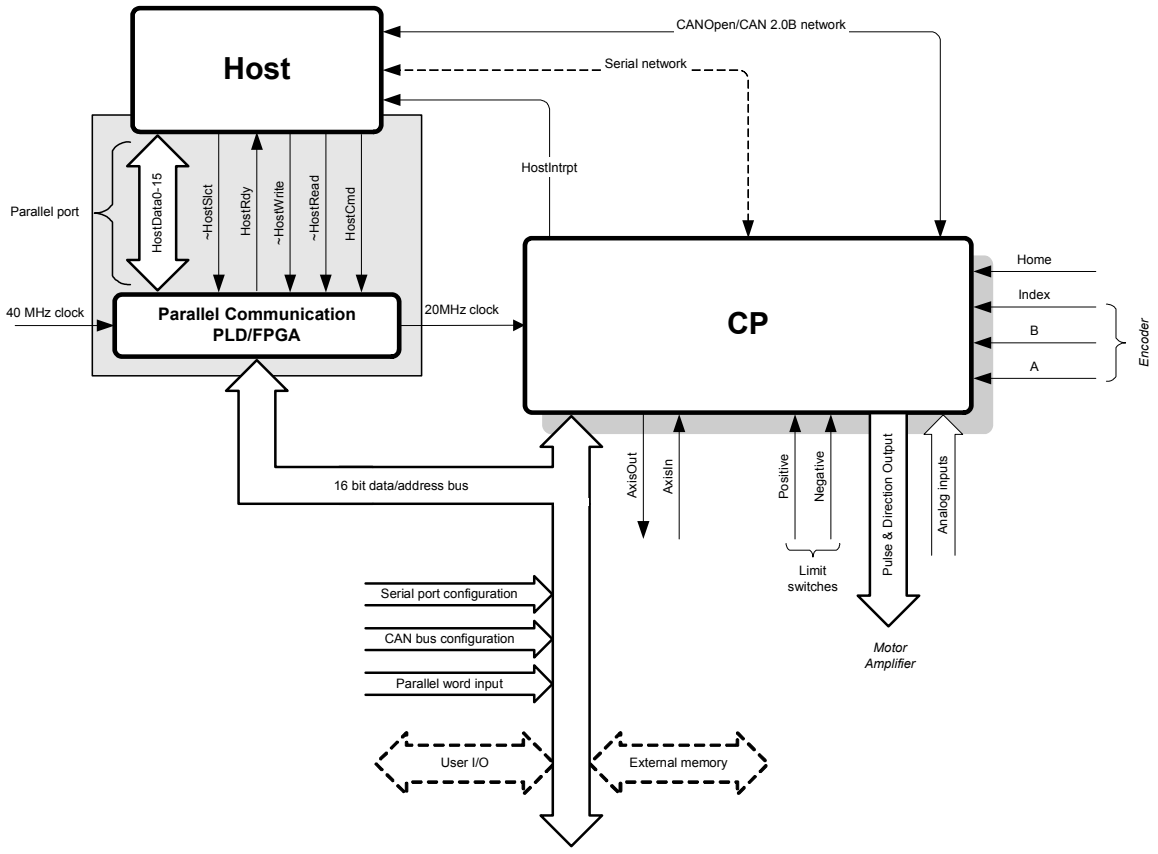


2.3 Environmental and electrical ratings

Storage Temperature (T_s)	-65 °C to 150 °C
Operating Temperature: Standard (T_a)	-40 °C to 85 °C*
Operating Temperature: Extended (T_a)	-40 °C to 125 °C*
Power Dissipation (P_d)	CP 445 mW IO 110 mW
Nominal Clock Frequency (F_{clk})	40.0 MHz
Supply Voltage limits (V_{cc})	-0.3V to +4.6V
Supply Voltage operating range (V_{cc})	3.0V to 3.6V

2.4 MC55110 System configuration – Single chip, 1 axis control

The following figure shows the principal control and data paths in an MC55110 system.



The shaded area shows the CPLD/FPGA that must be provided by the designer if parallel communication is required. A description and the necessary logic (in the form of schematics) of this device are detailed in section Parallel FPGA of this manual.

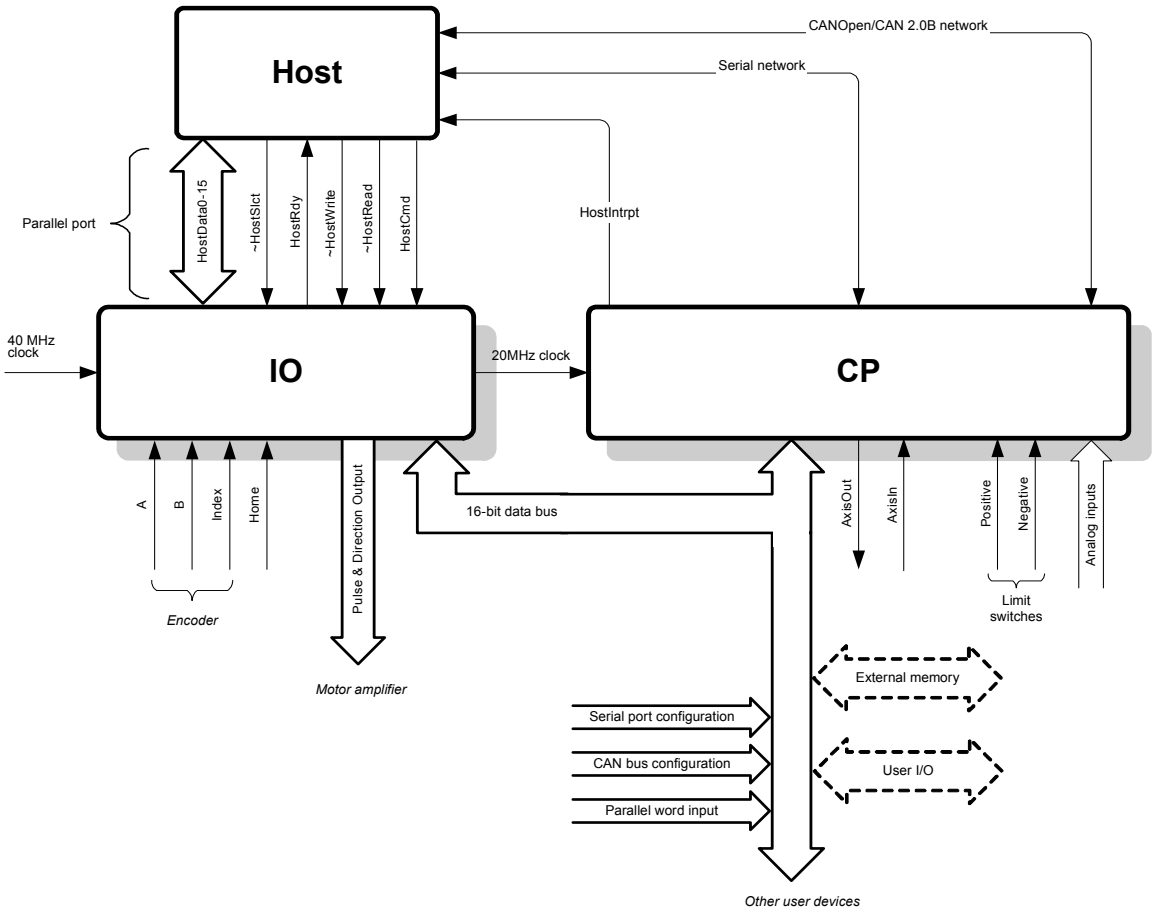
The CP chip is a self-contained motion processor. In addition to handling all system functions, the CP chip contains the profile generator, which calculates velocity, acceleration, and position values for a trajectory. Then the CP chip generates step and direction signals.

Optional axis position information returns to the motion processor in the form of encoder feedback using either the incremental encoder input signals, or via the bus as parallel word input.

The MC55110 can co-exist in a CANOpen network as a slave device. It is CAN 2.0B compliant.

2.5 MC55020 System configuration – Two chip, 1 to 4 axis control

The following figure shows the principal control and data paths in an MC55020 system.



The IO chip contains the parallel host interface, the incremental encoder input along with pulse and direction motor output signals.

The CP chip contains the profile generator, which calculates velocity, acceleration, and position values for a trajectory and communicates the results to the IO chip for output.

Optional axis position information returns to the motion processor in the form of encoder feedback using either the incremental encoder input signals, or via the bus as parallel word input.

The MC55020 can co-exist in a CANOpen network as a slave device. It is CAN 2.0B compliant.

2.6 Peripheral device address mapping

Device addresses on the CP chip's external bus are memory-mapped to the following locations:

Address	Device	Description
0200h	Serial port configuration	Contains the configuration data (transmission rate, parity, stop bits, etc) for the asynchronous serial port
0400h	CAN port configuration	Contains the configuration data (baud rate and node ID) for the CAN controller
0800h	Parallel-word encoder	Base address for parallel-word feedback devices
1000h	User-defined	Base address for user-defined I/O devices
2000h	RAM page pointer	Page pointer to external memory
8000h	Reserved	

3 Electrical Characteristics

3.1 DC characteristics

(V_{cc} and T_a per operating ratings, F_{clk} = 40.0 MHz)

Symbol	Parameter	Minimum	Maximum	Conditions
V_{cc}	Supply Voltage	3.00 V	3.6 V	
I_{dd}	Supply Current		135 mA CP 33 mA IO	open outputs
	Input Voltages			
V_{ih}	Logic 1 input voltage	2.0 V	V_{cc}	@CP
V_{il}	Logic 0 input voltage		0.8 V	@CP
	Output Voltages			
V_{oh}	Logic 1 Output Voltage	2.4 V		-2 mA@CP
V_{ol}	Logic 0 Output Voltage		0.4 V	8 mA@CP
	Other			
I_{out}	Tri-State output leakage current	-2 µA	2 µA	@CP $0 < V_{out} < V_{cc}$
I_{in}	Input current	-25 µA	25 µA	@CP $0 < V_i < V_{cc}$
I_{inclk}	Input current, CPClk	-25 µA	25 µA	$0 < V_i < V_{cc}$
C_{io}	Input/Output capacitance	2/3 pF		@CP typical
	Analog Input			
Z_{ai}	Analog input source impedance		10Ω	
E_{dnl}	Differential nonlinearity error. Difference between the step width and the ideal value.	-1	±2 LSB	
E_{inl}	Integral nonlinearity error. Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error.		±2 LSB	

3.2 AC characteristics

See timing diagrams, Section 4, for *Tn* numbers. The symbol "~" indicates active low signal.

Timing Interval	*Tn*	Minimum	Maximum
Clock Frequency (F_{clk})		4 MHz	40 MHz ***(note 1)***
Clock Pulse Width	T1	20 nsec	30 nsec
Clock Period ***(note 3)***	T2	50 nsec	250 nsec
Encoder Pulse Width	T3	150 nsec	
Dwell Time Per State	T4	75 nsec	

Timing Interval	*Tn*	Minimum	Maximum
Index Setup and Hold (relative to Quad A and Quad B low)	T5	0 nsec	
~HostSlct Hold Time	T6	0 nsec	
~HostSlct Setup Time	T7	0 nsec	
HostCmd Setup Time	T8	0 nsec	
HostCmd Hold Time	T9	0 nsec	
Read Data Access Time	T10		25 nsec
Read Data Hold Time	T11		10 nsec
~HostRead High to HI-Z Time	T12		20 nsec
HostRdy Delay Time	T13	100 nsec	150 nsec
~HostWrite Pulse Width	T14	70 nsec	
Write Data Delay Time	T15		25 nsec
Write Data Hold Time	T16	0 nsec	
Read Recovery Time ***(note 2)***	T17	60 nsec	
Write Recovery Time ***(note 2)***	T18	60 nsec	
Read Pulse Width	T19	70 nsec	
External Memory Read Timing			
ClockOut low to control valid	T20		4 nsec
ClockOut low to address valid	T21		8 nsec
Address valid to ~ReadEnable low	T22	31 nsec	
ClockOut high to ~ReadEnable low	T23		5 nsec
Data access time from Address valid	T24		40 nsec
Data access time from ~ReadEnable low	T25		31 nsec
Data hold time	T26	0 nsec	
ClockOut low to control inactive	T27		5 nsec
Address hold time after ClockOut low	T28	2 nsec	
ClockOut low to Strobe low	T29		5 nsec
ClockOut low to Strobe high	T30		6 nsec
W/~R low to R/~W rising delay time	T31		5 nsec
External Memory Write Timing			
ClockOut high to control valid	T32		4 nsec
ClockOut high to address valid	T33		10 nsec
Address valid to ~WriteEnable low	T34	29 nsec	
ClockOut low to ~WriteEnable low	T35		6 nsec
Data setup time before ~WriteEnable high	T36	33 nsec	
Data bus driven from ClockOut low	T37	-3 nsec	
Data hold time	T38	2 nsec	
ClockOut high to control inactive	T39		5 nsec
Address hold time after ClockOut low	T40	-5 nsec	
ClockOut low to Strobe low	T41		6 nsec
ClockOut low to Strobe high	T42		6 nsec
R/~W low to W/~R rising delay time	T43		5 nsec
ClockOut high to control valid	T44		6 nsec
Peripheral Device Read Timing			
Address valid to ~ReadEnable low	T22-45	56 nsec	
Data access time from Address valid	T24-46		65 nsec
Data access time from ~ReadEnable low	T25-47		56 nsec

Timing Interval	*Tn*	Minimum	Maximum
Peripheral Device Write Timing			
Address valid to ~WriteEnable low	T34-48	54 nsec	
Data setup time before ~WriteEnable high	T36-49	58 nsec	
Device Ready/ Outputs Initialized	T57		1 msec

Note 1 Performance figures and timing information valid at F_{clk} = 40.0 MHz only. For timing information and performance parameters at F_{clk} < 40.0 MHz, contact PMD.

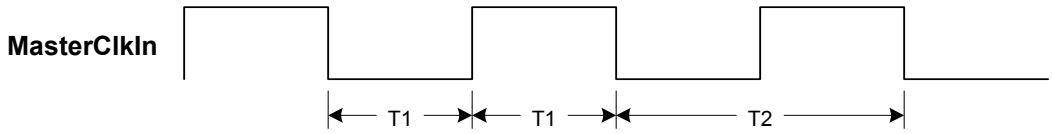
Note 2 For 8/16 interface modes only.

Note 3 The clock low/high split has an allowable range of 40-60%.

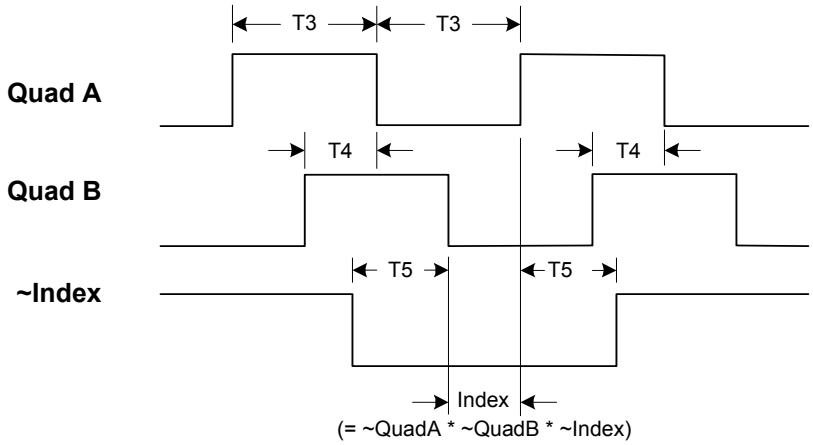
4 I/O Timing Diagrams

For the values of *Tn*, please refer to the table in Section 3.2.

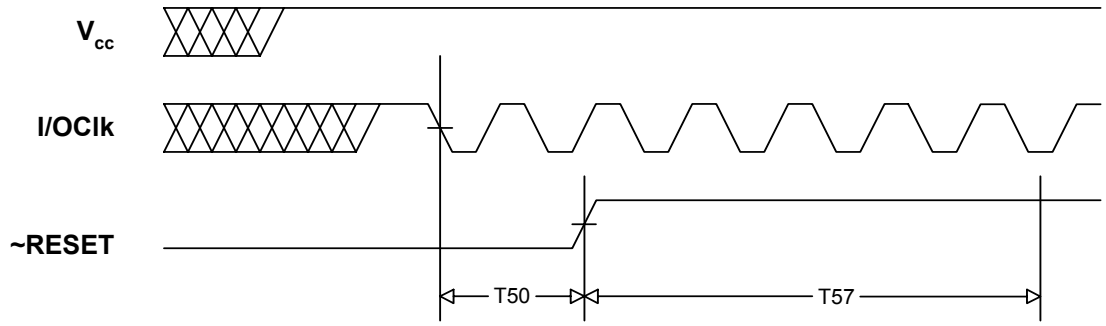
4.1 Clock



4.2 Quadrature encoder input

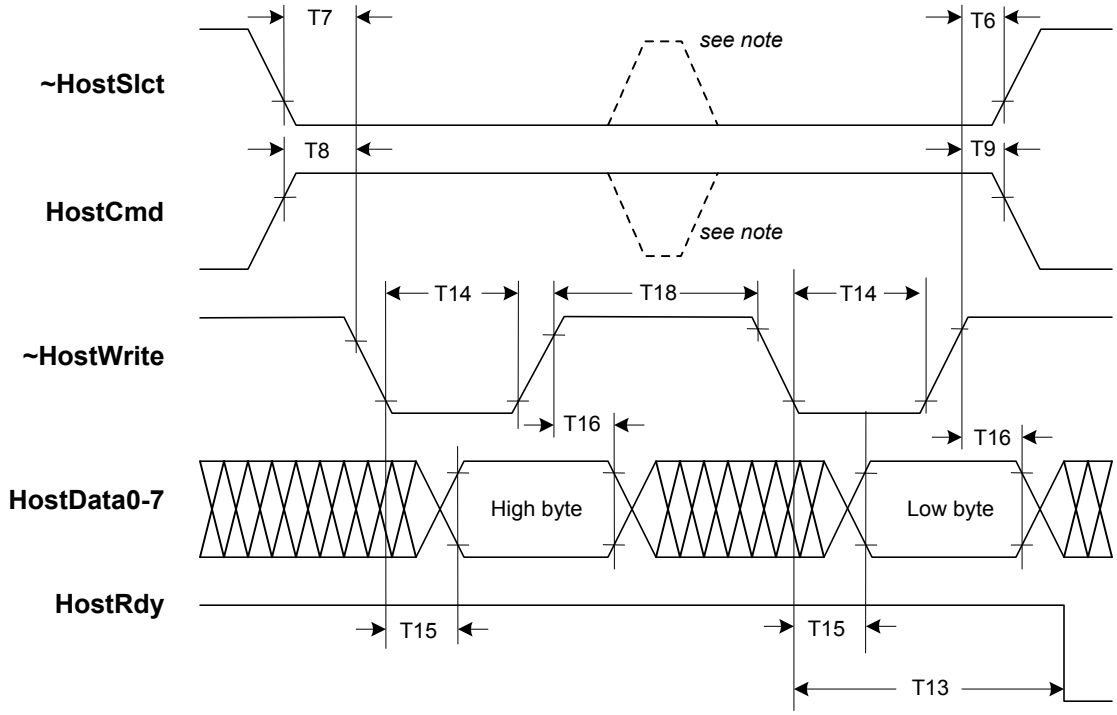


4.3 Reset



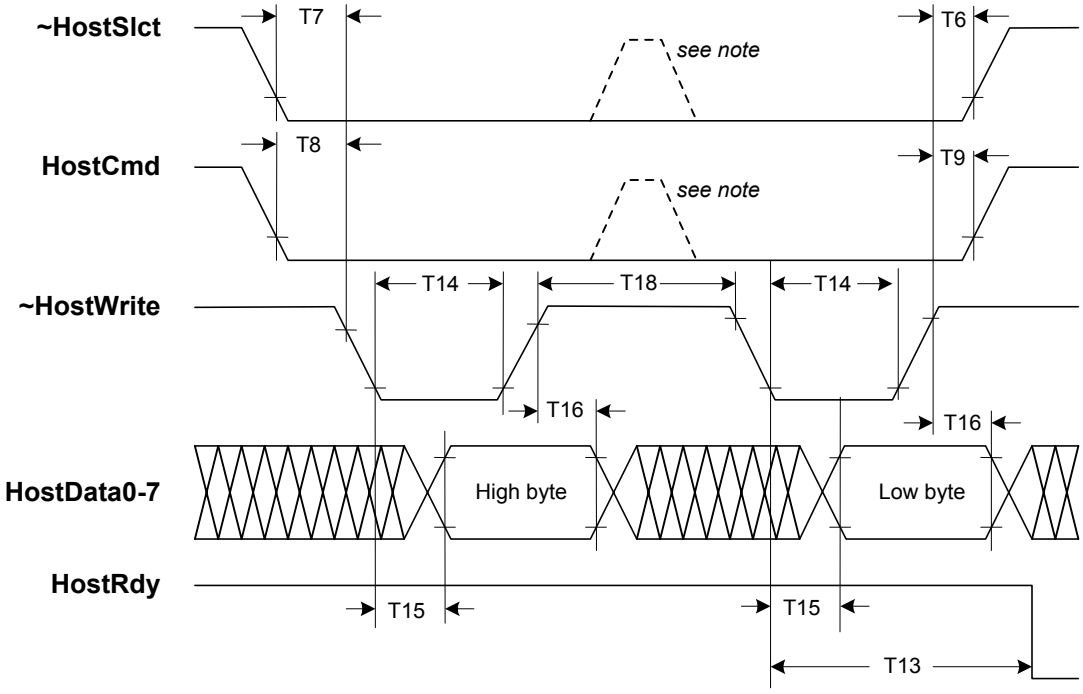
4.4 Host interface, 8/16 mode

4.4.1 Instruction write, 8/16 mode



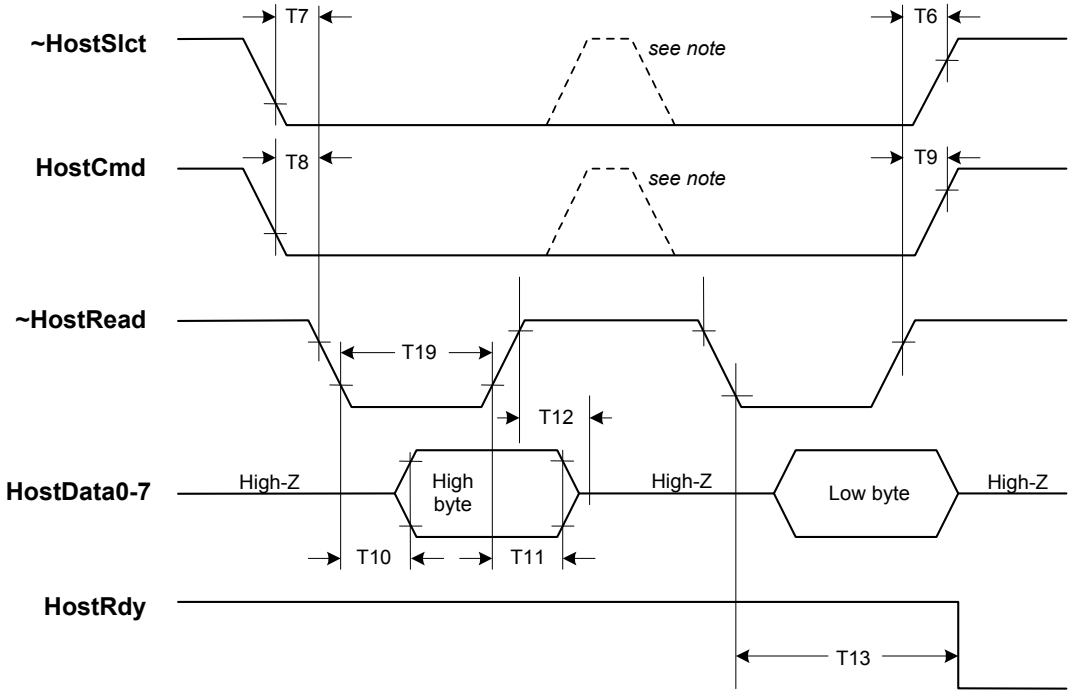
Note: If setup and hold times are met, ~HostSlct and HostCmd may be de-asserted at this point.

4.4.2 Data write, 8/16 mode



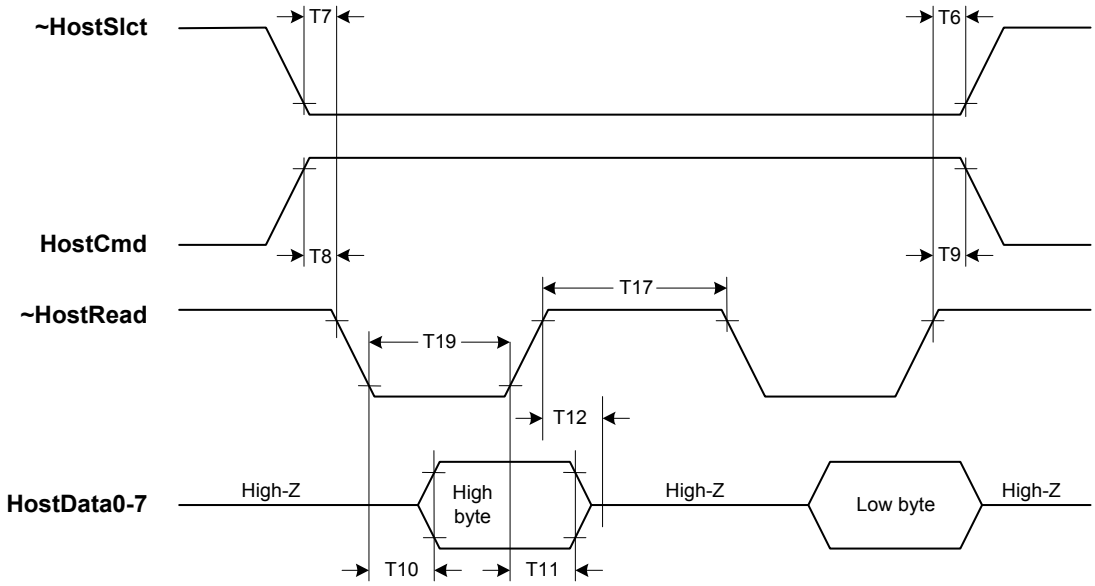
Note: If setup and hold times are met, ~HostSlct and HostCmd may be de-asserted at this point.

4.4.3 Data read, 8/16 mode



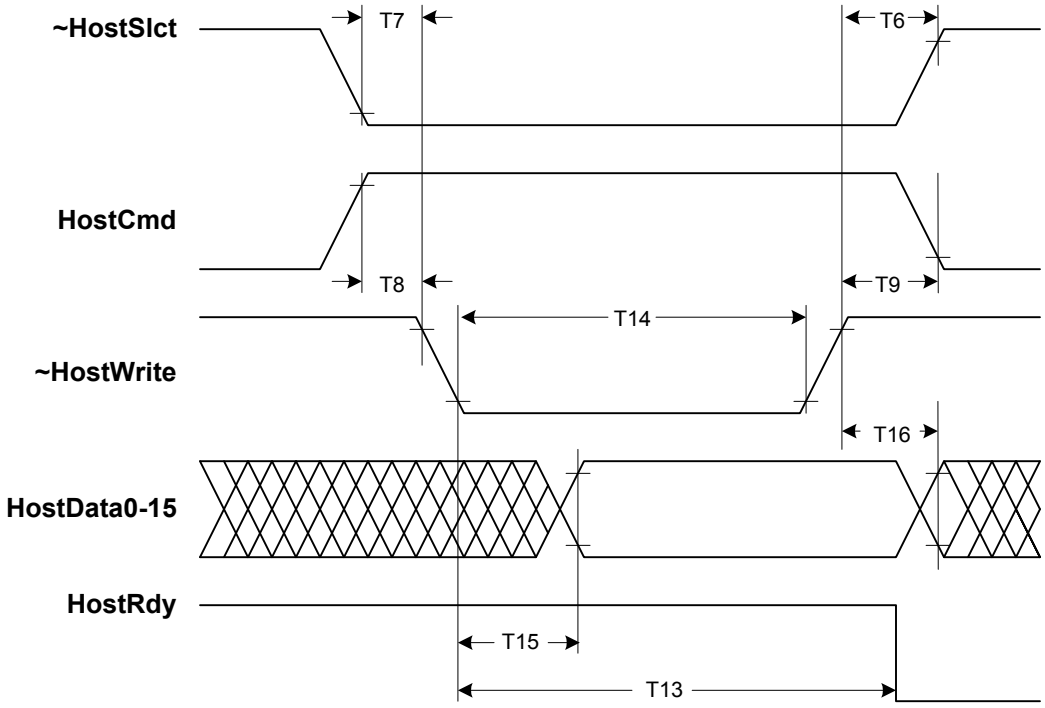
Note: If setup and hold times are met, ~HostSlct and HostCmd may be de-asserted at this point.

4.4.4 Status read, 8/16 mode

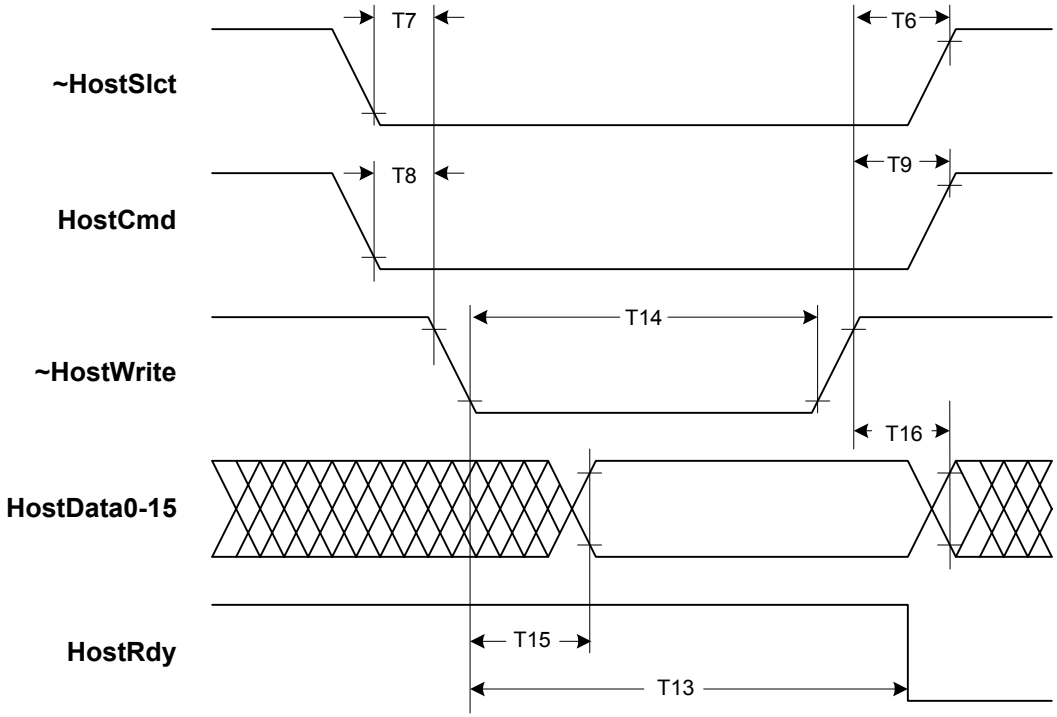


4.5 Host interface, 16/16 mode

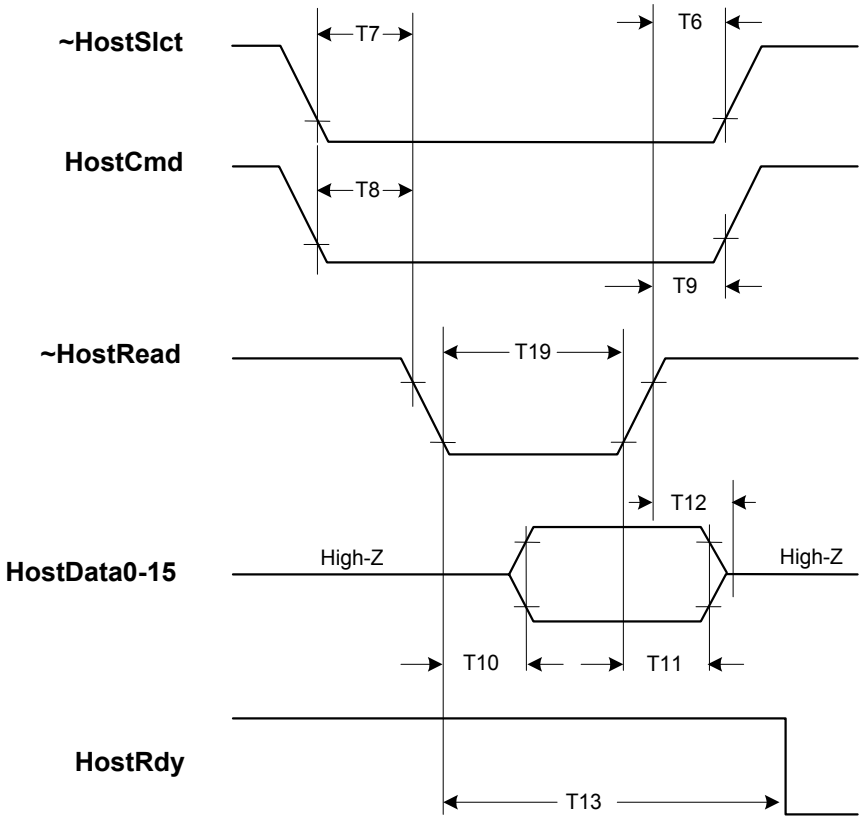
4.5.1 Instruction write, 16/16 mode



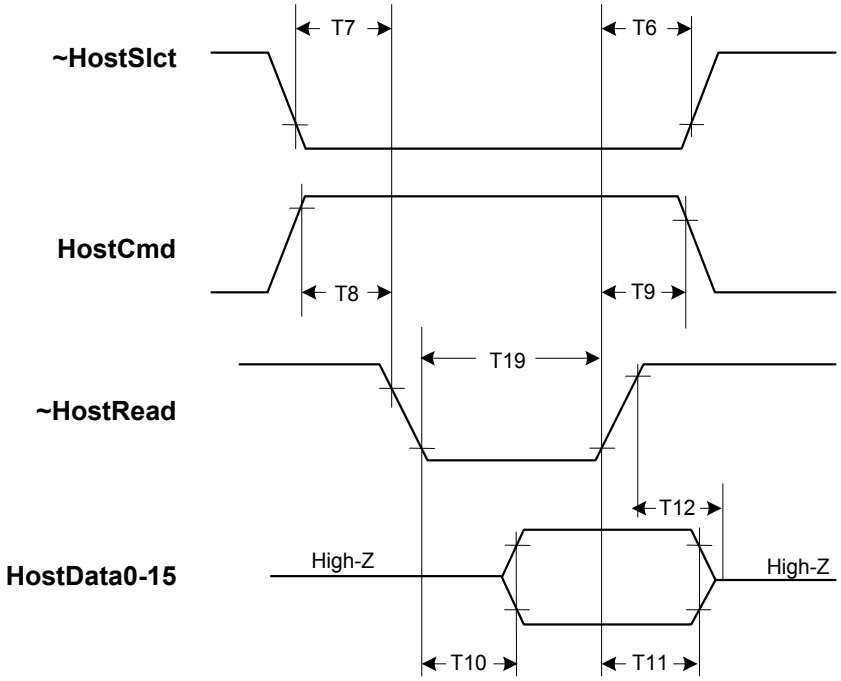
4.5.2 Data write, 16/16 mode



4.5.3 Data read, 16/16 mode



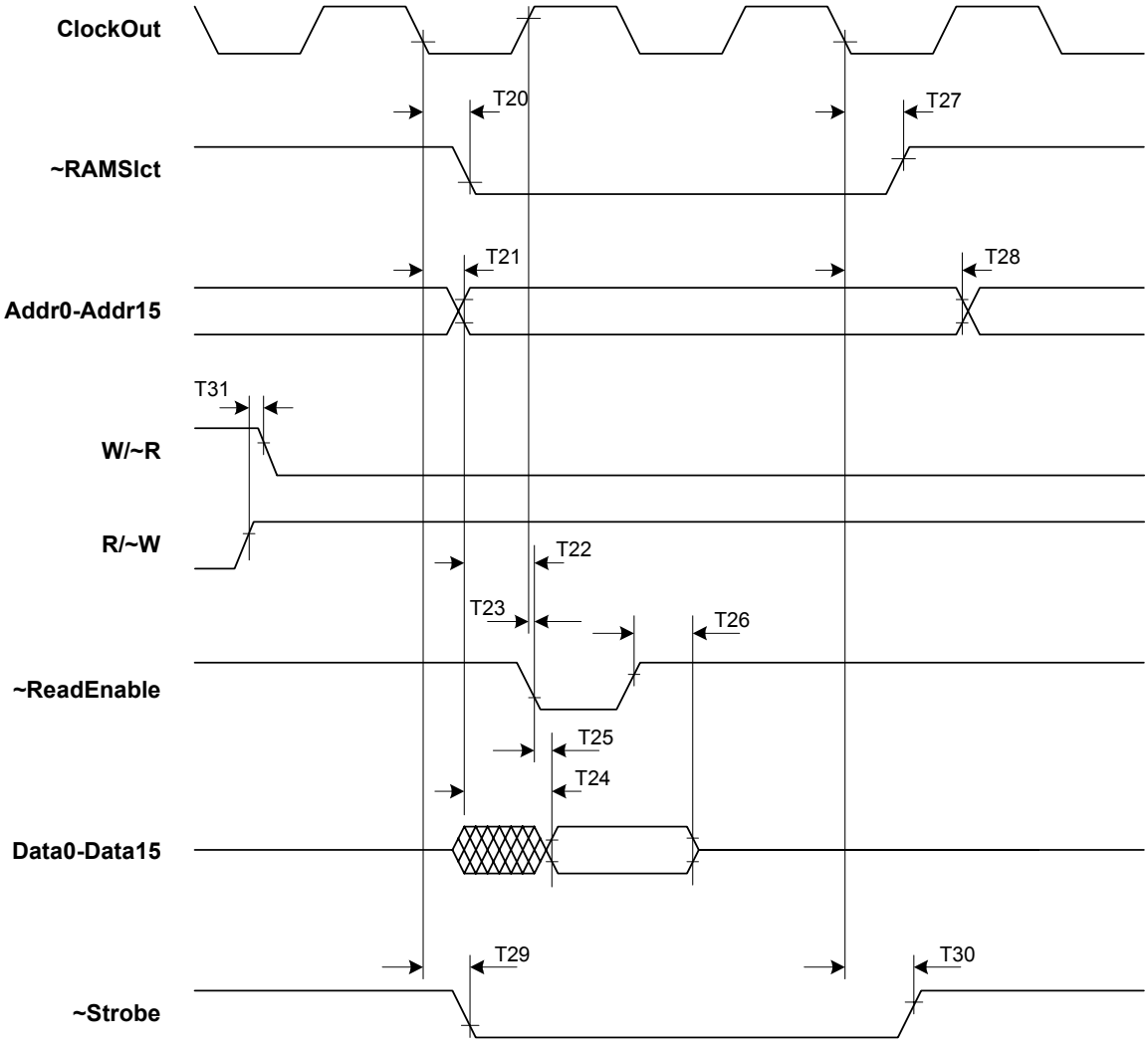
4.5.4 Status read, 16/16 mode



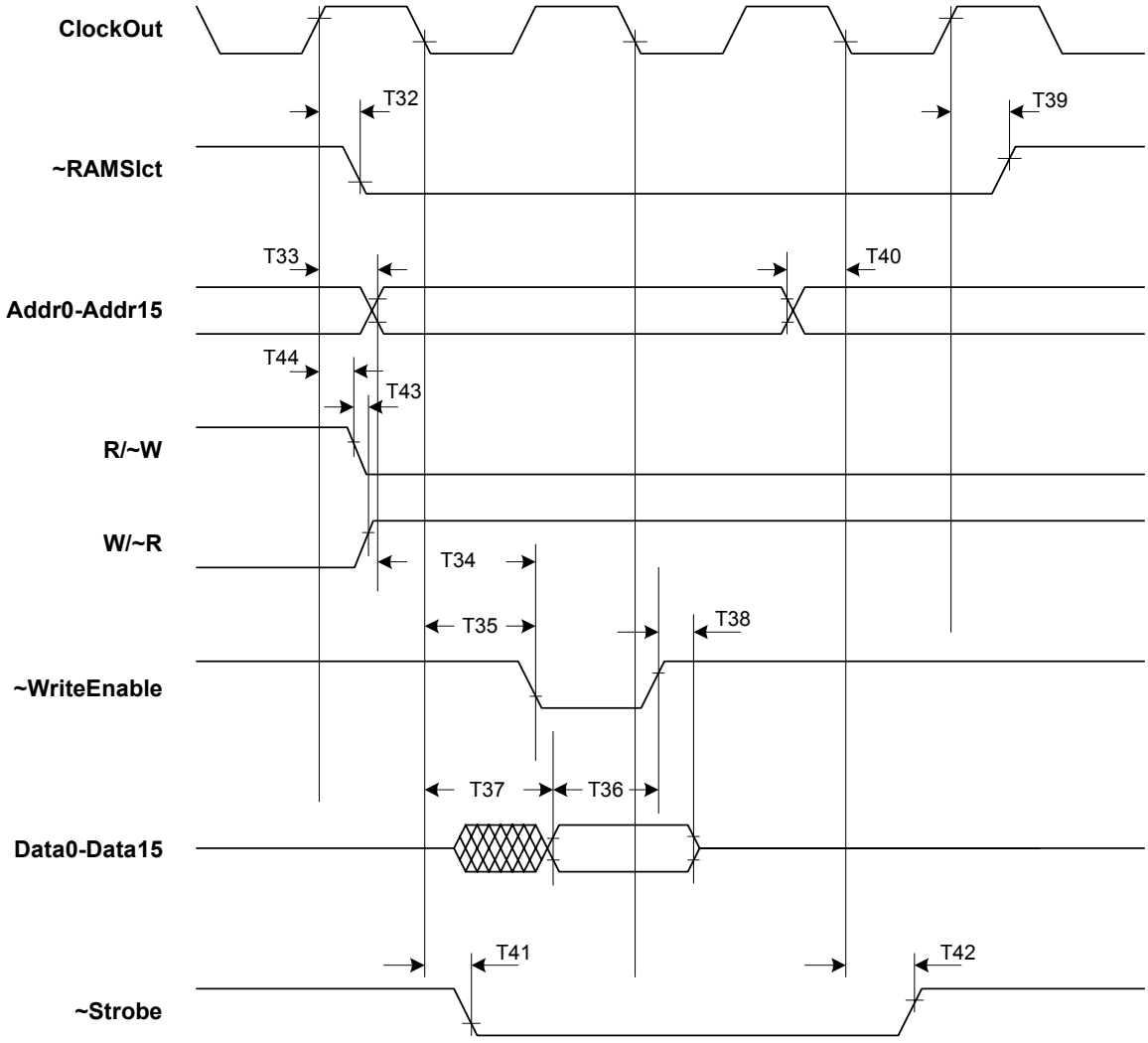
4.6 External memory timing

4.6.1 External memory read

Note: PMD recommends using memory with an access time no greater than 15 nsec.

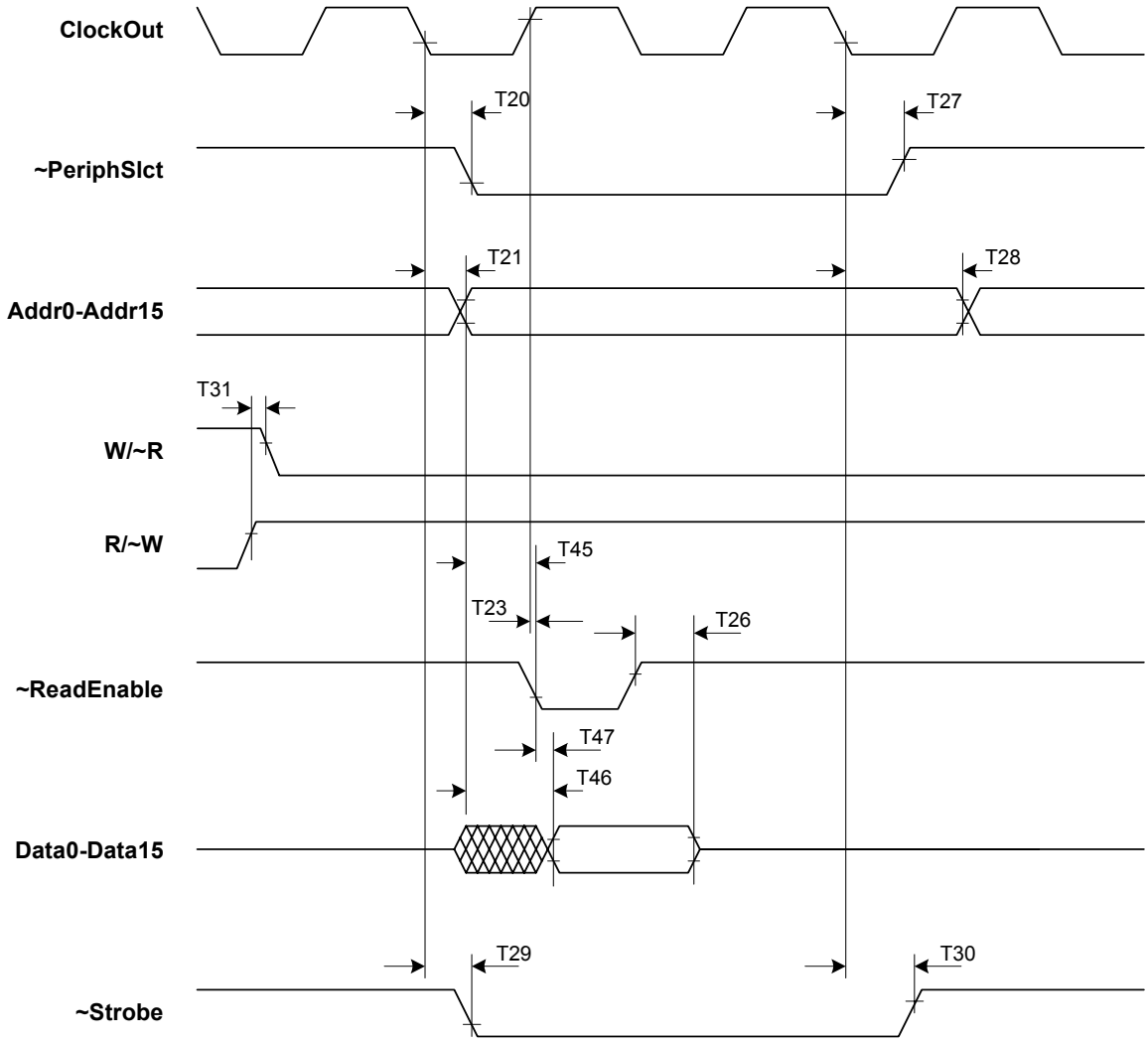


4.6.2 External memory write

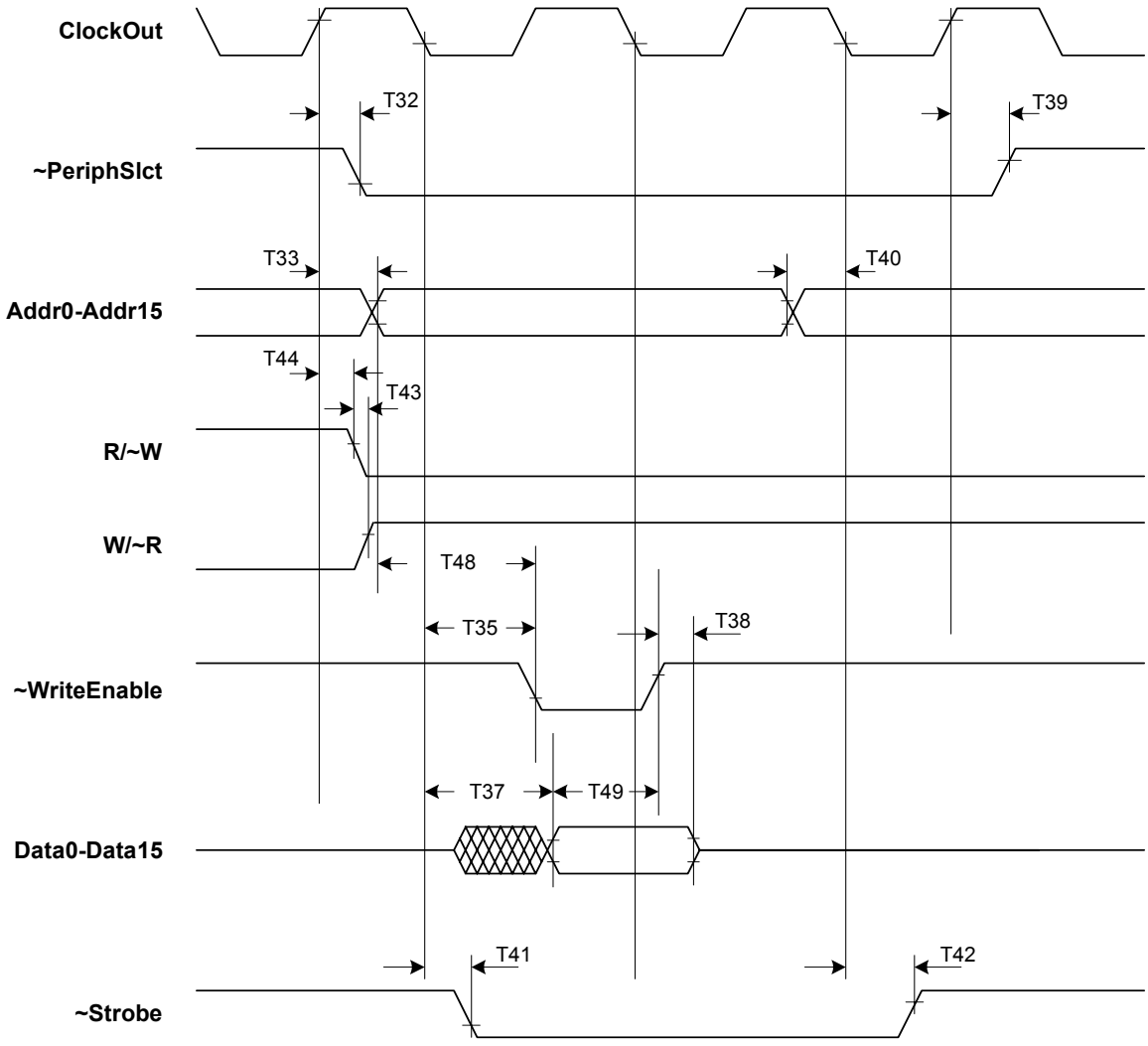


4.7 Peripheral device timing

4.7.1 Peripheral device read

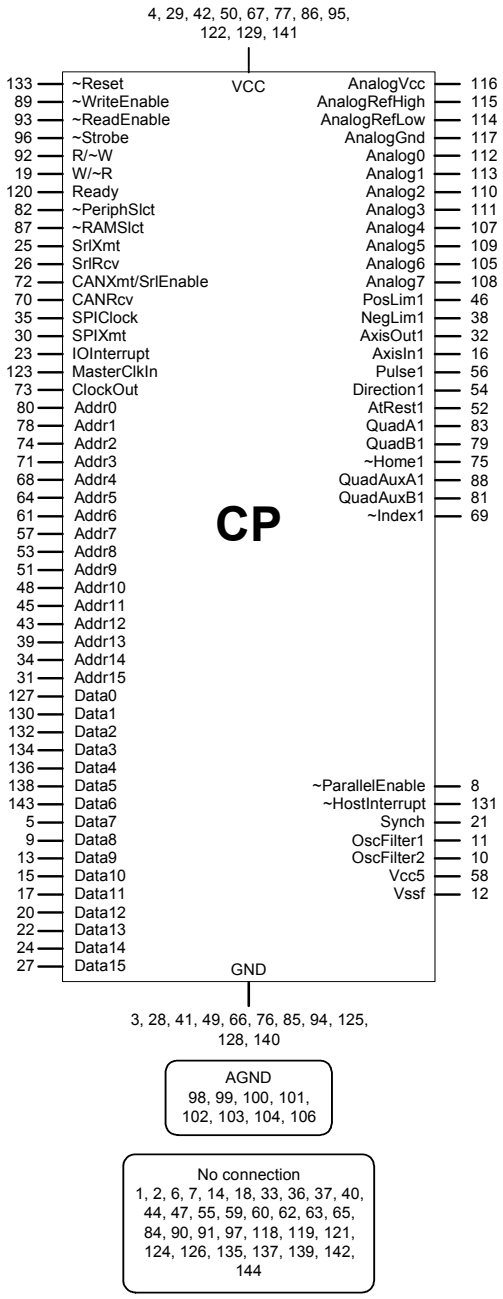


4.7.2 Peripheral device write



5 Pinouts and Pin Descriptions

5.1 Pinouts for the MC55110



5.1.1 MC55110 CP chip pin description

CP

Pin Name and number		Direction	Description
~Reset	133	input	This is the master reset signal. When brought *low*, this pin resets the chipset to its initial conditions.
~WriteEnable	89	output	This signal is the write-enable strobe. When *low*, this signal indicates that data is being written to the bus.
~ReadEnable	93	output	This signal is the read-enable strobe. When *low*, this signal indicates that data is being read from the bus.
~Strobe	96	output	This signal is *low* when the data and address are valid during CP communications. If the parallel interface is used, this pin should be connected to the PLD/FPGA IO chip signal CPStrobe.
R/~W	92	output	This signal is *high* when the CP chip is performing a read, and *low* when it is performing a write. If the parallel interface is used, this pin should be connected to the PLD/FPGA IO chip signal CPR/~W.
W/~R	19	output	This signal is the inverse of R/~W; it is *high* when R/~W is low, and vice versa. For some decode circuits and devices this is more convenient than R/~W.
Ready	120	input	Ready can be pulled low to add wait states for external accesses. Ready indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready, it pulls the Ready pin *low*. The motion processor then waits one cycle and checks Ready again. This signal can be left unconnected if it is not used.
~PeriphSlct	82	output	This signal is *low* when peripheral devices on the data bus are being addressed. If the parallel interface is used, this pin should be connected to the PLD/FPGA IO chip signal CPPeriphSlct.
~RAMSlct	87	output	This signal is *low* when external memory is being accessed.
SrlXmt	25	output	This pin outputs serial data from the asynchronous serial port.
SrlRcv	26	input	This pin inputs serial data to the asynchronous serial port.
CANXmt SrlEnable	72	output	When the CAN host interface is used, this pin transmits serial data to the CAN transceiver. When the multi-drop serial interface is used, this pin sets the serial port enable line and the CANXmt function is not available. SrlEnable is *high* during transmission for the multi-drop protocol and *low* at all other times.
CANRcv	70	output	This pin receives serial data from the CAN transceiver.
SPIClock	35	output	This pin is the clock signal used for strobing synchronous serial data to the serial DAC(s). This signal is only active when SPI data is being transmitted.
SPIXmt	30	output	This pin transmits synchronous serial data to the serial DAC(s).
IOInterrupt	23	input	This interrupt signal is used for IO to CP communication. If the parallel interface is used, this pin should be connected to the PLD/FPGA IO chip signal CPInterrupt. This signal can be left unconnected if it is not used.
MasterClkIn	123	input	This is the clock signal for the Motion Processor. It is driven at a nominal 20MHz.
ClockOut	73	output	This signal is the reference output clock. Its frequency is twice the frequency of the input clock (which is normally 20MHz) resulting in a nominal output frequency of 40MHz.

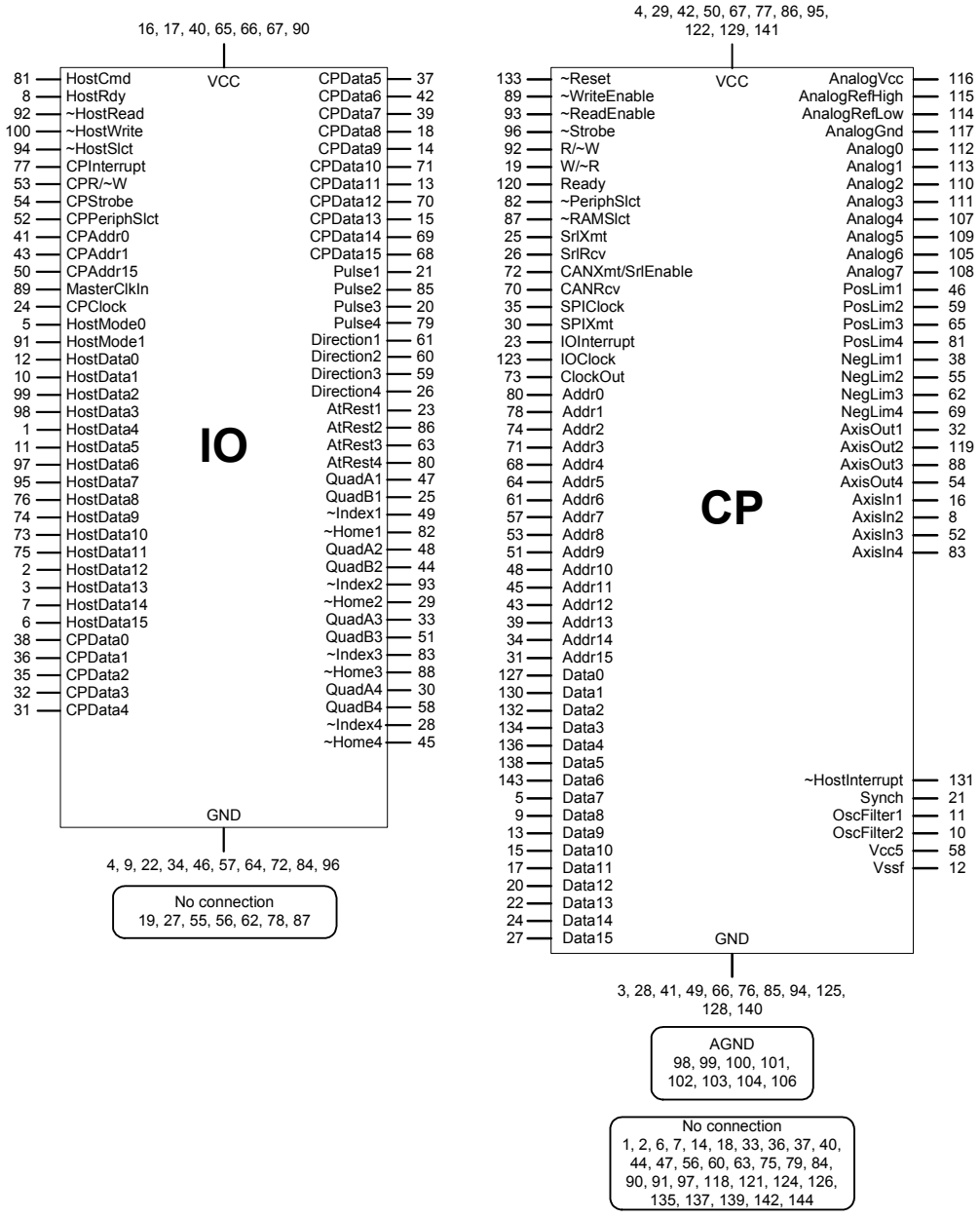
CP

Pin Name and number		Direction	Description
Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7 Addr8 Addr9 Addr10 Addr11 Addr12 Addr13 Addr14 Addr15	80 78 74 71 68 64 61 57 53 51 48 45 43 39 34 31	output	Multi-purpose address lines. These pins comprise the CP chip's external address bus, used to select devices for communication over the data bus. If the parallel interface is used, pins Addr0, Addr1, and Addr15 should be connected to the PLD/FPGA IO chip signals CPAddr0, CPAddr1 and CPAddr15. They are used to communicate between the CP and IO chips. Other address pins may be used for DAC output, parallel word input, or user-defined I/O operations. See the User's Guide for a complete memory map.
Data0 Data1 Data2 Data3 Data4 Data5 Data6 Data7 Data8 Data9 Data10 Data11 Data12 Data13 Data14 Data15	127 130 132 134 136 138 143 5 9 13 15 17 20 22 24 27	bi-directional	Multi-purpose data lines. These pins comprise the CP chip's external data bus, used for all communications with peripheral devices such as external memory or DACs. They may also be used for parallel-word input and for user-defined I/O operations. If the parallel interface is used, these pins should be connected to the PLD/FPGA IO chip signals CPData0-15.
AnalogVcc	116	input	Analog input Vcc. This pin should be connected to the analog input supply voltage, which must be in the range 3.0-3.6 V. If the analog input circuitry is not used, this pin should be tied to V_{cc}.
AnalogRefHigh	115	input	Analog high voltage reference for A/D input. The allowed range is AnalogRefLow to AnalogVcc. If the analog input circuitry is not used, this pin should be tied to V_{cc}.
AnalogRefLow	114	input	Analog low voltage reference for A/D input. The allowed range is AnalogGND to AnalogRefHigh. If the analog input circuitry is not used, this pin should be tied to GND.
AnalogGND	117	input	Analog input ground. This pin should be connected to the analog input power supply return. If the analog input circuitry is not used, this pin should be tied to GND.
Analog0 Analog1 Analog2 Analog3 Analog4 Analog5 Analog6 Analog7	112 113 110 111 107 109 105 108	input	These signals provide general-purpose analog voltage levels which are sampled by an internal A/D converter. The A/D resolution is 10 bits. The allowed signal input range is AnalogRefLow to AnalogRefHigh. Any unused pins should be tied to AnalogGND. If the analog input circuitry is not used, these pins should be tied to GND.

Pin Name and number		Direction	Description
PosLim1	46	input	This signal provides input from the positive-side (forward) travel limit switch. On power-up or after reset this signal defaults to active *low* interpretation, but the interpretation can be set to active *high* interpretation using the SetSignalSense instruction. If this pin is not used it may be left unconnected.
NegLim1	38	input	This signal provides input from the negative-side (reverse) travel limit switch. On power-up or after reset this signal defaults to active *low* interpretation, but the interpretation can be set to active *high* interpretation using the SetSignalSense instruction. If this pin is not used it may be left unconnected.
AxisOut1	32	output	This pin can be programmed to track the state of any bit in the status registers. If this pin is not used it may be left unconnected.
AxisIn1	16	input	This pin is a general-purpose input that can also be used as a breakpoint input. If this pin is not used it may be left unconnected.
Pulse1	56	output	This pin provides the pulse (step) signal to the motor. A step occurs when the signal transitions from a *high* to a *low* state. This default behavior can be changed to a *low* to *high* state transition using the command SetSignalSense. If this pin is not used it may be left unconnected.
Direction1	54	output	This pin indicates the direction of motion and works in conjunction with the pulse signal. A *high* level on this signal indicates a positive direction move and a *low* level indicates a negative direction move.
AtRest1	52	output	This signal indicates that the axis is at rest and the step motor can be switched to low power or standby mode. A *high* level on this signal indicates the axis is at rest while a *low* signal indicates the axis is in motion.
QuadA1 QuadB1	83 79	input	These pins should be connected to the A and B quadrature signals from the incremental encoder. When the axis is moving in the positive (forward) direction, signal A leads signal B by 90°. The theoretical maximum encoder pulse rate is 5.1 MHz. Actual maximum rate will vary, depending on signal noise. **NOTE**: Many encoders require a pull-up resistor on each signal to establish a proper high signal. Check your encoder's electrical specification. If these pins are not used they may be left unconnected.
~Home1	75	input	This pin provides the home signal, a general-purpose input to the position capture mechanism. A valid home signal is recognized by the motion processor when ~Home transitions from *high* to *low*. If this pin is not used it may be left unconnected.
QuadAuxA1 QuadAuxB1 ~Index1	88 81 69	input	If index capture is required, the encoder A and B signals connected to QuadA1 and QuadB1 signals must also be connected to QuadAuxA1 and QuadAuxB1. The index pin should be connected to the index signal from the incremental encoder. A valid index pulse is recognized by the motion processor when this signal transitions from *high* to *low*. If these pins are not used they may be left unconnected. **WARNING! There is no internal gating of the index signal with the encoder A and B inputs. This must be performed externally if desired. Refer to the Application Notes section at the end of this manual for an example.**

Pin Name and number		Direction	Description
ParallelEnable	8	input	This signal enables/disables the parallel communication with the host. If this signal is tied *high*, the parallel interface is enabled. If this signal is tied *low* the parallel interface is disabled. Contact PMD for more information on parallel communication. **WARNING! This signal should only be tied high if an external logic device that implements the parallel communication logic is included in the design.**
~HostInterrupt	131	output	When *low*, this signal causes an interrupt to be sent to the host processor.
Synch	21	input/output	This pin is the synchronization signal. In the disabled mode, the pin is configured as an input and is not used. In the master mode, the pin outputs a synchronization pulse that can be used by slave nodes or other devices to synchronize with the internal chip cycle of the master node. In the slave mode, the pin is configured as an input and should be connected to the Synch pin on the master node. A pulse on the pin synchronizes the internal chip cycle to the signal provided by the master node. If this pin is not used it may be left unconnected.
OscFilter1 OscFilter2	11 10		These signals connect to the external oscillator filter circuitry. Section 5.3 shows the required filter circuitry.
V_{cc5}	58		This signal can optionally be tied to a 5V logic supply, which is required for reprogramming the chipset firmware.
V_{ssf}	12		This signal must be tied to pin 28 using a bypass capacitor. A ceramic capacitor with a value between 0.1µF and 0.01µF should be used.
V_{cc}	4, 29, 42, 50, 67, 77, 86, 95, 122, 129, 141		CP digital supply voltage. All of these pins must be connected to the supply voltage. V_{cc} must be in the range 3.0 – 3.6 V.
GND	3, 28, 41, 49, 66, 76, 85, 94, 125, 128, 140		CP digital supply ground. All of these pins must be connected to the digital power supply return.
AGND	98, 99, 100, 101, 102, 103, 104, 106		These signals must be tied to AnalogGND. If the analog input circuitry is not used, these pins must be tied to GND.
No connection	1, 2, 6, 7, 14, 18, 33, 36, 37, 40, 44, 47, 55, 59, 60, 62, 63, 65, 84, 90, 91, 97, 118, 119, 121, 124, 126, 135, 137, 139, 142, 144		These signals must be left unconnected.

5.2 Pinouts for the MC55420



5.2.1 MC55020 IO chip pin description

IO

Pin Name and Number		Direction	Description
HostCmd	81	input	This signal is asserted *high* to write a host instruction to the motion processor, or to read the status of the HostRdy and HostInterrupt signals. It is asserted *low* to read or write a data word.
HostRdy	8	output	This signal is used to synchronize communication between the motion processor and the host. HostRdy (HostReady) will go *low* indicating host port busy at the end of a read or write operation according to the interface mode in use, as follows: **Interface Mode** **HostRdy goes *low*** 8/16 after the second byte of the instruction word after the second byte of each data word is transferred 16/16 after the 16-bit instruction word after each 16-bit data word HostRdy will go *high,* indicating that the host port is ready to transmit, when the last transmission has been processed. All host port communications must be made with HostRdy *high* (ready). A typical busy-to-ready cycle is 10 microseconds, but can be substantially longer, up to 50 microseconds.
~HostRead	92	input	When ~HostRead is *low*, a data word is read from the motion processor.
~HostWrite	100	input	When ~HostWrite is *low*, a data word is written to the motion processor.
~HostSlct	94	input	When ~HostSlct is *low*, the host port is selected for reading or writing operations.
CPInterrupt	77	output	IO chip to CP chip interrupt. It should be connected to CP chip pin 23, IOInterrupt.
CPR/~W	53	input	This signal is *high* when the CP chip is reading data from the IO chip, and *low* when it is writing data. It should be connected to CP chip pin 92, R/~W.
CPStrobe	54	input	This signal goes *low* when the data and address become valid during motion processor communication with peripheral devices on the data bus, such as external memory or a DAC. It should be connected to CP chip pin 96, ~Strobe.
CPPeriphSlct	52	input	This signal goes *low* when a peripheral device on the data bus is being addressed. It should be connected to CP chip pin 82, ~PeriphSlct.
CPAddr0 CPAddr1 CPAddr15	41 43 50	input	These signals are *high* when the CP chip is communicating with the IO chip (as distinguished from any other device on the data bus). They should be connected to CP chip pins 80 (Addr0), 78 (Addr1), and 31 (Addr15).
MasterClkIn	89	input	This is the master clock signal for the motion processor. It is driven at a nominal 40 MHz
CPClock	24	output	This signal provides the clock pulse for the CP chip. Its frequency is half that of MasterClkIn (pin 89), or 20 MHz nominal. It is connected directly to the CP chip IOClock signal (pin 123).
HostMode0 HostMode1	5 91	input	These two signals determine the host communications mode, as follows: **HostMode1** **HostMode0** 0 0 16/16 parallel (16-bit bus, 16-bit instruction) 0 1 *not used* 1 0 8/16 parallel (8-bit bus, 16-bit instruction) 1 1 Parallel disabled

Pin Name and Number		Direction	Description
HostData0 HostData1 HostData2 HostData3 HostData4 HostData5 HostData6 HostData7 HostData8 HostData9 HostData10 HostData11 HostData12 HostData13 HostData14 HostData15	12 10 99 98 1 11 97 95 76 74 73 75 2 3 7 6	bi-directional, tri-state	These signals transmit data between the host and the motion processor through the parallel port. Transmission is mediated by the control signals ~HostSelect, ~HostWrite, ~HostRead and HostCmd. In 16-bit mode, all 16 bits are used (HostData0-15). In 8-bit mode, only the low-order 8 bits of data are used (HostData0-7). The HostMode0 and HostMode1 signals select the communication mode this port operates in.
CPData0 CPData1 CPData2 CPData3 CPData4 CPData5 CPData6 CPData7 CPData8 CPData9 CPData10 CPData11 CPData12 CPData13 CPData14 CPData15	38 36 35 32 31 37 42 39 18 14 71 13 70 15 69 68	bi-directional	These signals transmit data between the IO chip and pins Data0-15 of the CP chip.
Pulse1 Pulse2 Pulse3 Pulse4	21 85 20 79	output	These pins provide the pulse (step) signal to the motor. This signal is always a square wave, regardless of the pulse rate. A step occurs when the signal transitions from a high state to a low state. This default behavior can be changed to a low to high state transition using the command SetSignalSense. The number of available axes determines which of these signals are valid. Invalid axis pins may be left unconnected.
Direction1 Direction2 Direction3 Direction4	61 60 59 26	output	These pins indicate the direction of motion and work in conjunction with the pulse signal. A high level on this signal indicates a positive direction move and a low level indicates a negative direction move. The number of available axes determines which of these signals are valid. Invalid axis pins may be left unconnected.
AtRest1 AtRest2 AtRest3 AtRest4	23 86 63 80	output	The AtRest signal indicates the axis is at rest and the step motor can be switched to low power or standby. A high level on this signal indicates the axis is at rest. A low signal indicates the axis is in motion. The number of available axes determines which of these signals are valid. Invalid axis pins may be left unconnected.

IO

Pin Name and Number		Direction	Description
QuadA1 QuadB1 QuadA2 QuadB2 QuadA3 QuadB3 QuadA4 QuadB4	47 25 48 44 33 51 30 58	input	These pins provide the A and B quadrature signals for the incremental encoder for each axis. When the axis is moving in the positive (forward) direction, signal A leads signal B by 90°. The theoretical maximum encoder pulse rate is 10.2 MHz. Actual maximum rate will vary, depending on signal noise. **NOTE**: Many encoders require a pull-up resistor on each signal to establish a proper high signal. Check your encoder's electrical specification. The number of available axes determines which of these signals are valid. **WARNING! If a valid axis pin is not used, its signal should be tied high.** Invalid axis pins may be left unconnected or connected to ground.
~Index1 ~Index2 ~Index3 ~Index4	49 93 83 28	input	These pins provide the Index quadrature signals for the incremental encoders. A valid index pulse is recognized by the chipset when ~Index, A, and B are all *low*. The number of available axes determines which of these signals are valid. **WARNING! If a valid axis pin is not used, its signal should be tied high.** Invalid axis pins may be left unconnected or connected to ground.
~Home1 ~Home2 ~Home3 ~Home4	82 29 88 45	input	These pins provide the Home signals, general-purpose inputs to the position-capture mechanism. A valid Home signal is recognized by the chipset when ~Home*n* goes *low*. These signals are similar to ~Index, but are not gated by the A and B encoder channels. The number of available axes determines which of these signals are valid. **WARNING! If a valid axis pin is not used, its signal should be tied high.** Invalid axis pins may be left unconnected or connected to ground.
Vcc	16, 17, 40, 65, 66, 67, 90		All of these pins must be connected to the IO chip digital supply voltage, which should be in the range 3.0 to 3.6 V.
GND	4, 9, 22, 34, 46, 57, 64, 72, 84, 96		IO chip ground. All of these pins must be connected to the digital power supply return.
Not connected	19, 27, 55, 56, 62, 78, 87		These pins must be left unconnected (floating).

5.2.2 MC55020 CP chip pin description

CP

Pin Name and number		Direction	Description
~Reset	133	input	This is the master reset signal. When brought *low*, this pin resets the chipset to its initial conditions.
~WriteEnable	89	output	This signal is the write-enable strobe. When *low*, this signal indicates that data is being written to the bus.
~ReadEnable	93	output	This signal is the read-enable strobe. When *low*, this signal indicates that data is being read from the bus.
~Strobe	96	output	This signal is *low* when the data and address are valid during CP communications. It should be connected to IO chip pin 54, CPStrobe.
R/~W	92	output	This signal is *high* when the CP chip is performing a read, and *low* when it is performing a write. It should be connected to IO chip pin 53, CPR/~W.
W/~R	19	output	This signal is the inverse of R/~W; it is *high* when R/~W is low, and vice versa. For some decode circuits and devices this is more convenient than R/~W.
Ready	120	input	Ready can be pulled low to add wait states for external accesses. Ready indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready, it pulls the Ready pin *low*. The motion processor then waits one cycle and checks Ready again. This signal can be left unconnected if it is not used.
~PeriphSlct	82	output	This signal is *low* when peripheral devices on the data bus are being addressed. It should be connected to IO chip pin 52, CPPeriphSlct.
~RAMSlct	87	output	This signal is *low* when external memory is being accessed.
SrlXmt	25	output	This pin outputs serial data from the asynchronous serial port.
SrlRcv	26	input	This pin inputs serial data to the asynchronous serial port.
CANXmt SrlEnable	72	output	When the CAN host interface is used, this pin transmits serial data to the CAN transceiver. When the multi-drop serial interface is used, this pin sets the serial port enable line and the CANXmt function is not available. SrlEnable is *high* during transmission for the multi-drop protocol and *low* at all other times.
CANRcv	70	output	This pin receives serial data from the CAN transceiver.
SPIClock	35	output	This pin is the clock signal used for strobing synchronous serial data to the serial DAC(s). This signal is only active when SPI data is being transmitted.
SPIXmt	30	output	This pin transmits synchronous serial data to the serial DAC(s).
IOInterrupt	23	input	This interrupt signal is used for IO to CP communication. It should be connected to IO chip pin 77, CPInterrupt.
IOClock	123	input	This is the CP chip clock signal. It should be connected to IO chip pin 24, CPClock.
ClockOut	73	output	This signal is the reference output clock. Its frequency is the same as the MasterClkIn signal to the IO chip, nominally 40MHz.

CP

Pin Name and number		Direction	Description
Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7 Addr8 Addr9 Addr10 Addr11 Addr12 Addr13 Addr14 Addr15	80 78 74 71 68 64 61 57 53 51 48 45 43 39 34 31	output	Multi-purpose Address lines. These pins comprise the CP chip's external address bus, used to select devices for communication over the data bus. Addr0, Addr1, and Addr15 are connected to the corresponding CPAddr pins on the IO chip, and are used to communicate between the CP and IO chips. Other address pins may be used for DAC output, parallel word input, or user-defined I/O operations. See the User's Guide for a complete memory map.
Data0 Data1 Data2 Data3 Data4 Data5 Data6 Data7 Data8 Data9 Data10 Data11 Data12 Data13 Data14 Data15	127 130 132 134 136 138 143 5 9 13 15 17 20 22 24 27	bi-directional	Multi-purpose data lines. These pins comprise the CP chip's external data bus, used for all communications with the IO chip and peripheral devices such as external memory or DACs. They may also be used for parallel-word input and for user-defined I/O operations.
AnalogVcc	116	input	Analog input Vcc. This pin should be connected to the analog input supply voltage, which must be in the range 3.0-3.6 V. If the analog input circuitry is not used, this pin should be tied to V_{cc}.
AnalogRefHigh	115	input	Analog high voltage reference for A/D input. The allowed range is AnalogRefLow to AnalogVcc. If the analog input circuitry is not used, this pin should be tied to V_{cc}.
AnalogRefLow	114	input	Analog low voltage reference for A/D input. The allowed range is AnalogGND to AnalogRefHigh. If the analog input circuitry is not used, this pin should be tied to GND.
AnalogGND	117	input	Analog input ground. This pin should be connected to the analog input power supply return. If the analog input circuitry is not used, this pin should be tied to GND.
Analog0 Analog1 Analog2 Analog3 Analog4 Analog5 Analog6 Analog7	112 113 110 111 107 109 105 108	input	These signals provide general-purpose analog voltage levels which are sampled by an internal A/D converter. The A/D resolution is 10 bits. The allowed signal input range is AnalogRefLow to AnalogRefHigh. Any unused pins should be tied to AnalogGND. If the analog input circuitry is not used, these pins should be tied to GND.

CP

Pin Name and number		Direction	Description
PosLim1 PosLim2 PosLim3 PosLim4	46 59 65 81	input	These signals provide inputs from the positive-side (forward) travel limit switches. On power-up or after reset these signals default to active *low* interpretation, but the interpretation can be set explicitly using the SetSignalSense instruction. The number of available axes determines which of these signals are valid. Invalid or unused pins may be left unconnected.
NegLim1 NegLim2 NegLim3 NegLim4	38 55 62 69	input	These signals provide inputs from the negative-side (reverse) travel limit switches. On power-up or after reset these signals default to active *low* interpretation, but the interpretation can be set explicitly using the SetSignalSense instruction. The number of available axes determines which of these signals are valid. Invalid or unused pins may be left unconnected.
AxisOut1 AxisOut2 AxisOut3 AxisOut4	32 119 88 54	output	Each of these pins can be conditioned to track the state of any bit in the Status registers associated with its axis. The number of available axes determines which of these signals are valid. Invalid or unused pins may be left unconnected.
AxisIn1 AxisIn2 AxisIn3 AxisIn4	16 8 52 83	input	These are general-purpose inputs that can also be used as a breakpoint input. The number of available axes determines which of these signals are valid. Invalid or unused pins may be left unconnected.
~HostInterrupt	131	output	When *low*, this signal causes an interrupt to be sent to the host processor.
Synch	21	input/output	This pin is the synchronization signal. In the disabled mode, the pin is configured as an input and is not used. In the master mode, the pin outputs a synchronization pulse that can be used by slave nodes or other devices to synchronize with the internal chip cycle of the master node. In the slave mode, the pin is configured as an input and should be connected to the Synch pin on the master node. A pulse on the pin synchronizes the internal chip cycle to the signal provided by the master node. If this pin is not used it may be left unconnected.
OscFilter1 OscFilter2	11 10		These signals connect to the external oscillator filter circuitry. Section 5.3 shows the required filter circuitry.
V_{cc5}	58		This signal can optionally be tied to a 5V logic supply, which is required for reprogramming the chipset firmware.
V_{ssf}	12		This signal must be tied to pin 28 using a bypass capacitor. A ceramic capacitor with a value between 0.1µF and 0.01µF should be used.
V_{cc}	4, 29, 42, 50, 67, 77, 86, 95, 122, 129, 141		CP digital supply voltage. All of these pins must be connected to the supply voltage. V_{cc} must be in the range 3.0 – 3.6 V.
GND	3, 28, 41, 49, 66, 76, 85, 94, 125, 128, 140		CP digital supply ground. All of these pins must be connected to the digital power supply return.
AGND	98, 99, 100, 101, 102, 103, 104, 106		These signals must be tied to AnalogGND. If the analog input circuitry is not used, these pins must be tied to GND.
No connection	1, 2, 6, 7, 14, 18, 33, 36, 37, 40, 44, 47, 56, 60, 63, 75, 79, 84, 90, 91, 97, 118, 121, 124, 126, 135, 137, 139, 142, 144		These signals must be left unconnected.

5.3 External oscillator filter

The following circuit shows the recommended configuration and suggested values for the filter that must be connected to the OscFilter1 and OscFilter2 pins of the CP chip. The resistor tolerance is ±5% and the capacitor tolerance is ±20%.