PLESSEY
Semiconductors

T-45-19-09

SP8755A&B

1200MHz ÷ 64

The SP8755 is a divide by 64 prescaler which operates from a standard 5V TTL supply and will drive TTL directly. The SP8755A operates over the full military temperature range (-55°C to +125°C).

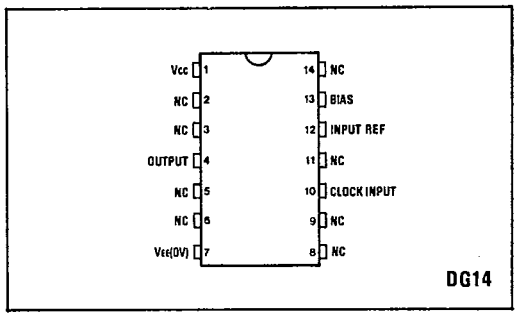


Fig.1 Pin connections - top view

FEATURES

- TTL Compatible Output
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 270mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output current	±30mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

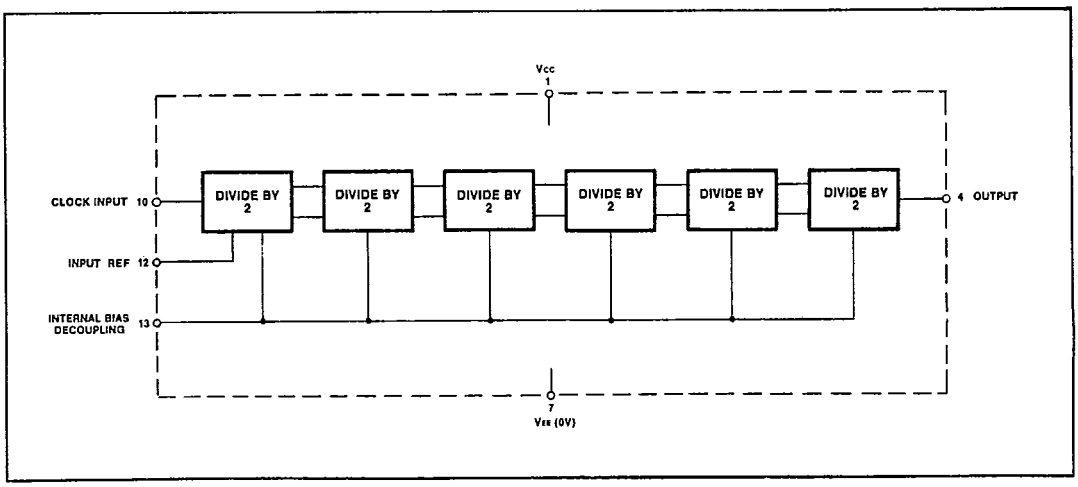


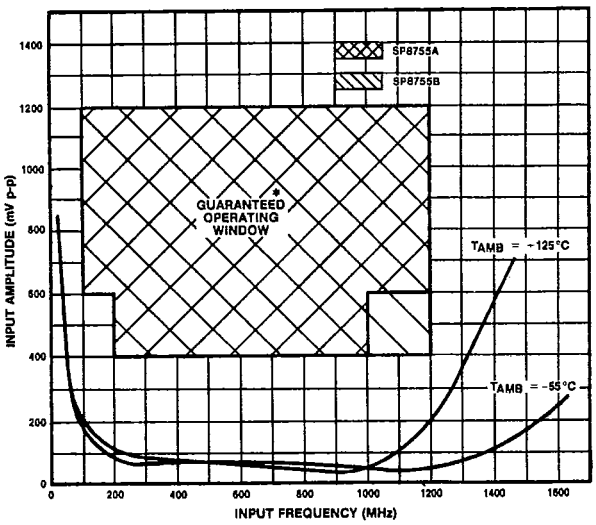
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	1.2		GHz	SP8755A	Input = 600-1200mV p-p
		1.2		GHz	SP8755B	Input = 400-1200mV p-p
Minimum frequency sinewave input	f_{min}	-	100	MHz	Both	Input = 600-1200mV p-p
Power supply current	I_{EE}		75	mA	Both	
Output high voltage	V_{OH}	2.5		V	Both	
Output low voltage	V_{OL}		0.45	V	Both	Sink current = 5mA

NOTES
1. Unless otherwise stated,the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8755A/B

OPERATING NOTES

1. The clock input is biased internally and is connected to the signal source via a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting an 18k resistor between input and V_{EE} (i.e. Pin 10 to Pin 7). This will reduce sensitivity by approximately 100mV.
3. The device will operate down to DC but input slew rate must be better than 100V/µs.
4. The output stage is a standard totem pole TTL and can therefore be interfaced directly to TTL.

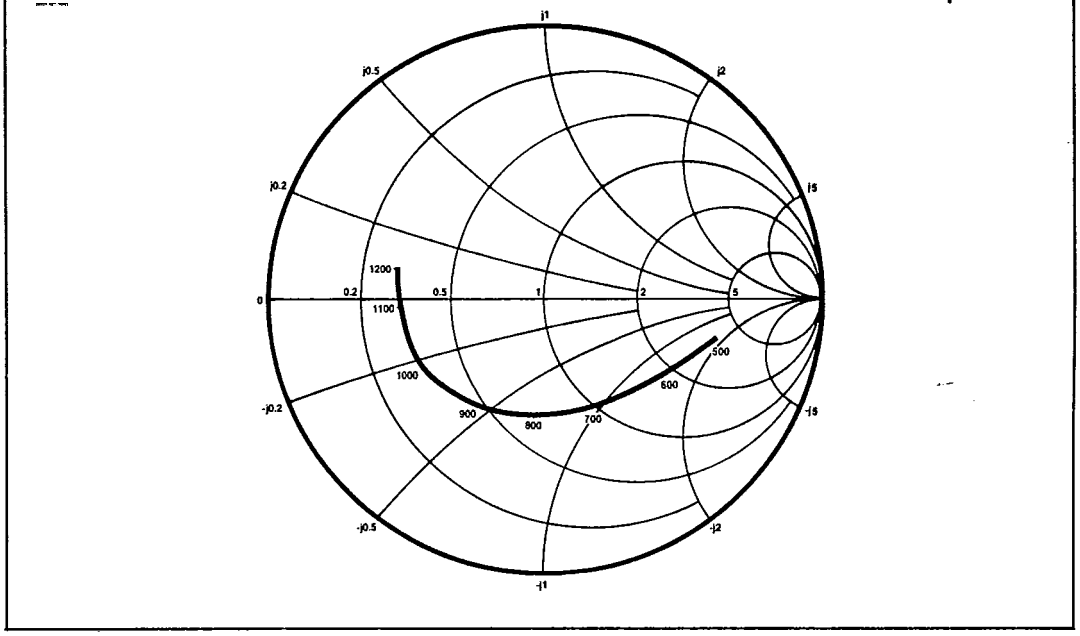


Fig.4 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

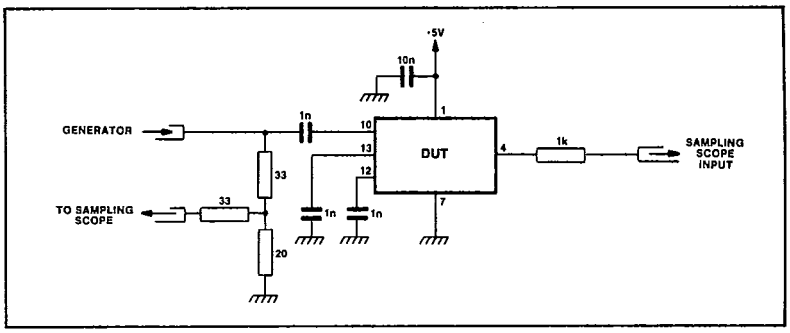


Fig.5 Test circuit

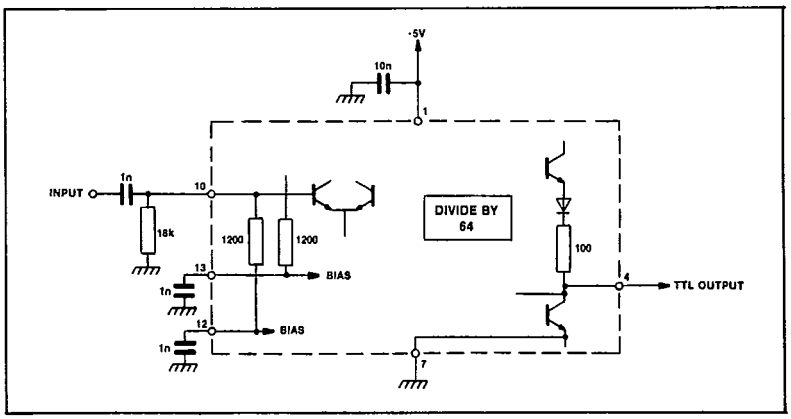


Fig.6 Typical applications circuit showing interfacing