SPL11A Programming Guide

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凌陽科技
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0 Table of Content

1 Revision History

Revision	Date	By	Remark

2 Introduction

2.1 General Description

SPL11A, a 8-bit LCD micro-controller, contains LCD-drivers, one-time programmable (OTP) ROM, SRAM, I/O, timer/counter, PLL, audio/remote control out, resistor to frequency converter (RFC) function in a single chip. The SPL11A is designed to drive LCD directly and perform efficient controller function as well as arithmetic function. With the on-chip crystal oscillator, real time clock can be easily achieved. For power savings, several power-down modes are controllable by software programming. The SPL11A is designed to be used in low-power electronic products such as remote controller, home appliance, calculator, and general LCD controller, etc.

2.2 Feature

- Built-in Sunplus 8-bit CPU (Compatible with full 6502 instruction sets)
- Working voltage: 2.4V ~ 5.5V
- Maximum CPU speed: 4MHz @ 2.4V in ROSC mode
- 8K-byte EPROM with parallel programming & verification
- 128 bytes SRAM
- 48 bytes dual-port SRAM for LCD buffers
- LCD bias: 1/2 bias, 1/3 bias, 1/4 bias
- LCD dots: 12x30 (360 dots), 11x30 (330 dots), 10x30 (300 dots), 9x32 (288 dots), 8x32 (256 dots), 5x32 (160 dots), 4x32 (128 dots), and 3x32 (96 dots)
- A 16-bit re-loadable timer/counter
- An 8-pin IOA (Input with pull-high, input with pull low, floating, output, N open drain, P open drain)
- IOB Inputs with key wakeup function & pull-low (4 inputs pins shared with LCD segments)
- Dual clock PLL/R-oscillator & 32768
- CPU Clock: PLL/2, PLL/4, PLL/8, PLL/16, 32768
- PLL clock = 32768 * 37 * 4 = 4,849,664Hz; Maximum CPU clock in PLL clock mode: 4849664/2 = 2,424,832Hz
- Four Operating modes: Operating, Wait, Halt, and Standby modes
- Interrupt sources: 37.9K/N, 32768/N, TMO, EXT0, EXT1, T2Hz, and KEYC.
- Seven wakeup sources
- Built-in RFC (Resistor to Frequency Converter) function
- Reset flags: watchdog, error address, power-on, external reset, low voltage
- Watchdog reset and error-address reset are always enabled and will reset CPU if these events

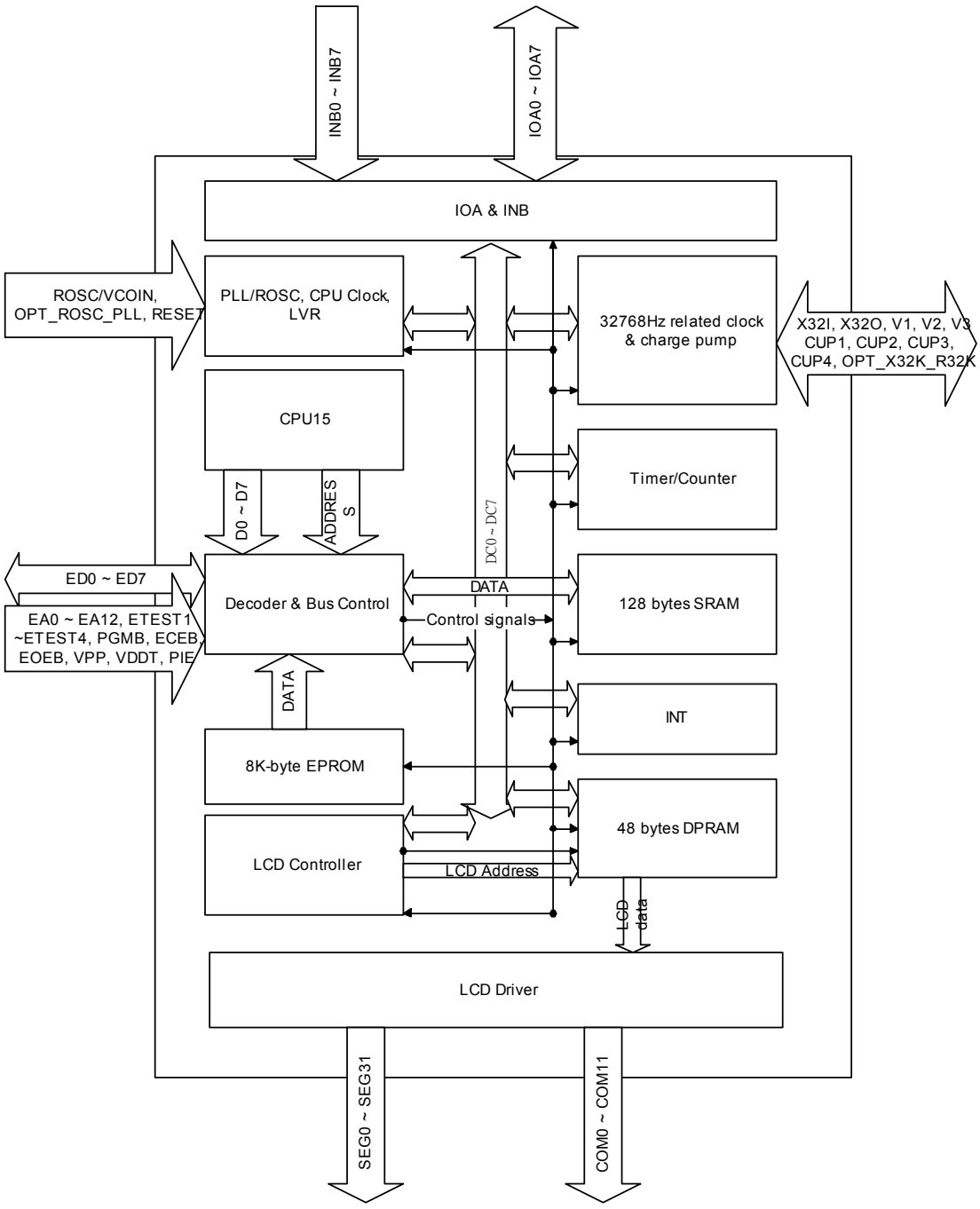
occur

- Low voltage reset can be disabled by LVROFF pin
- Wakeup start from reset or next instruction
- Low voltage reset level: 2.4V
- The pin assignment of ROM version will be the same as in OTP version, except PIE, VDDT, VPP, HCKOPT, LCKOPT, LVROFF, and TEST pins

2.3 Application

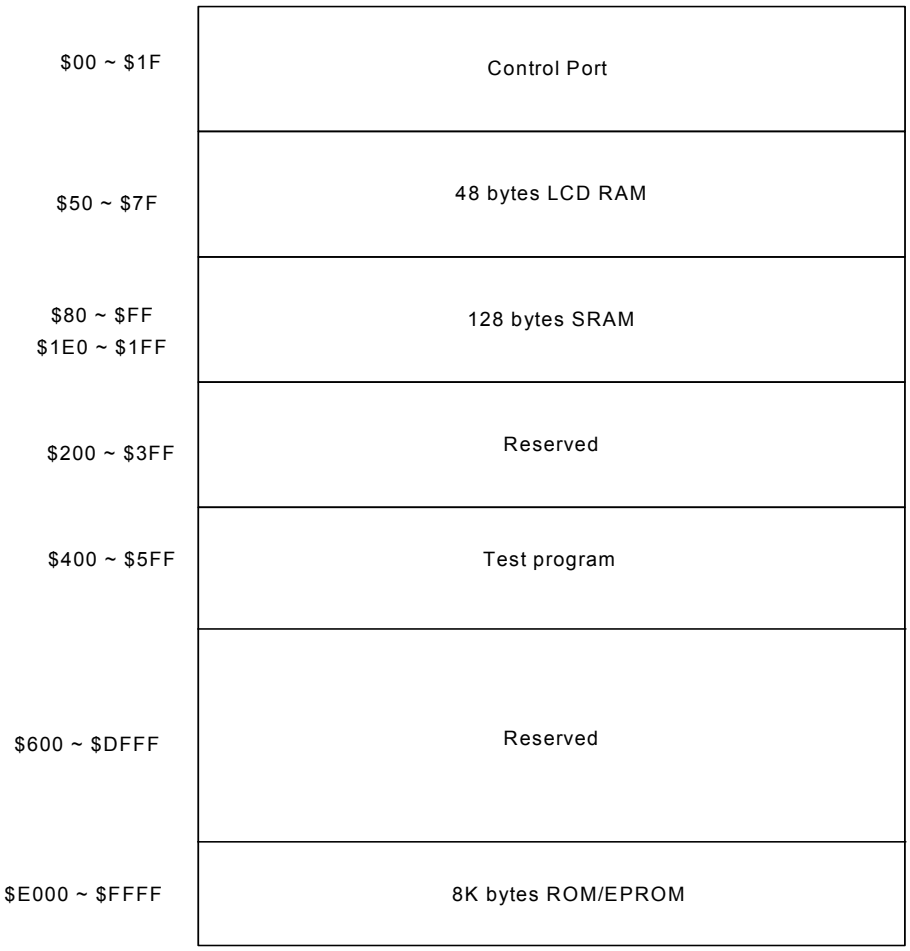
- Remote controller with LCD ability.
- LCD controller for home appliance.
- Watch, calendar, calculator, etc.

2.4 Structure Diagram



3 Memory

3.1 Memory Mapping



3.2 Memory location

- LCD RAM is a dual-port SRAM, from $50 to $7F
- $0080 ~ $00FF is CPU SRAM; $01E0 ~ $01FF maps to $E0 ~ $FF for the use of stack (maximum stack is 32 bytes).

  ** The top stacker pointer must be placed in the range of $01E0~$01FF.
- 8K-byte ROM/EPROM address is from $E000 ~ $FFFF
- 512-byte test program ROM ($400 ~ $5FF), for Sunplus use only.
- $FFF9 bit7 is for OTP security if this bit set “1” (data is not readable).

3.3 Vector

- Test program interrupt vector: $5FA~$5FF (Sunplus use only).
- User program interrupt vector: $FFFA~$FFFF.

3.4 Error-address area

Unavailable address range: $0020 ~ $004F, $0100 ~ $01DF, $0200 ~ $03FF, $0600 ~ $DFFF, and $0400 ~ $05FF. Accessing these addresses will cause the entire system to be reset and the b3 (error-address flag) in P_12H_RST_FG ($0012) will be set to “1”.

3.5 Example

$FFFA must be added to the following interrupt vectors:

```
DW      NMI
DW      RESET
DW      IRQ
```

Initial stack pointer:

```
LDX     #FFH
TXS
……..
```

4 CPU Clock Control

4.1 Clock Source Control

There are two groups of clock sources controlled by two clock option pins:

1. High-speed clock sources (HSCK): PLL / ROSC.
2. Low-speed clock sources (LSCK): 32768Hz oscillator / 32768 Crystal.

They are selected by pin option (OTP version) or mask option (ROM version). In OTP version: HSCK (High-speed clock) can be selected to PLL or Rosc via ***HCKOPT pin*** (pull-high for PLL; pull-low for ROSC (default)). In ROM version: HSCK (High-speed clock) can be selected to PLL or Rosc via ***mask option.***

In OTP version: LSCK (Low-speed clock) can be selected to X32K or R32K by ***LCKOPT pin*** (pull high for R32K; pull-low for X32K (default)). In ROM version: LSCK (Low-speed clock) can be selected to X32K or R32K via ***mask option***.

4.1.1 Clock sources combination (OTP)

	HCKOPT	LCKOPT	
ROSC/X32K	0	0	
ROSC/R32K	0	1	
PLL/X32K	1	X	Note

Note: No PLL/R32K combination, it is mapped to PLL/X32K mode

4.2 CPU Clock Control Register

4.2.1 P_05H_CPU_CLK ($0005): set CPU clock

$0005	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Name	-	-	-	-	-	CPUCK2	CPUCK1	CPUCK0
R/W	-	-	-	-	-	R/W	R/W	R/W
Default	-	-	-	-	-	0	0	0

Bit / **Mode**	**b2 (CPUCK2)**	**b1 (CPUCK1)**	**b0 (CPUCK0)**
CPUCK=HSCK/16	0	0	0
CPUCK=HSCK/8	0	0	1
CPUCK=HSCK/4	0	1	0
CPUCK=HSCK/2	0	1	1
CPUCK=LSCK(32768)	1	X	X

5 IO and RFC function

5.1 PortA(IOA) Control Register

Relevant Register: P_00H_IOA_Data($0000), P_01H_IOA_Dir($0001), P_02H_IOA_Attrib($0002)

5.1.1 P_00H_IOA_Data ($0000): Data register of PortA

Write data into register and read data back from IOA pad

$0000	b7	b6	b5	b4	b3	b2	b1	b0
Name	IOADAT7	IOADAT6	IOADAT5	IOADAT4	IOADAT3	IOADAT2	IOADAT1	IOADAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

5.1.2 P_01H_IOA_Dir ($0001): Direction Control register of PortA

$0001	b7	b6	b5	b4	b3	b2	b1	b0
Name	IOADIR7	IOADIR6	IOADIR5	IOADIR4	IOADIR3	IOADIR2	IOADIR1	IOADIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Input	0	0	0	0	0	0	0	0
Output	1	1	1	1	1	1	1	1
Default	0	0	0	0	0	0	0	0

5.1.3 P_02H_IOA_Attrib ($0002): Attribute data register of PortA

$0002	b7	b6	b5	b4	b3	b2	b1	b0
Name	IOAATT7	IOAATT6	IOAATT5	IOAATT4	IOAATT3	IOAATT2	IOAATT1	IOAATT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Configuration of IOA [7:0], where x represents IOA individual bit.

Dir ($01.x)	Attrib ($02.x)	Data ($00.x)	I/O Identity (IOAx)	Description
0	**0**	**0**	Pull Low	Input with pull-low
0	**0**	**1**	Pull High	Input with pull-high
0	**1**	**1**	LCD output (IO floating)	IOA5 => COM 8 IOA4 => COM 11 IOA3 => SEG29 IOA2 => SEG28 IOA0/IOA1/IOA6/IOA7 are input floating
0	**1**	**0**	Pass Through	IOA7 => IROUT IOA6 => TONE IOA5 => HSCK/N-TIMER IOA4 => LSCK(32768) IOA0/IOA1/IOA2/IOA3 are output Low
1	**0**	**1**	Output High	Output Data High
1	**0**	**0**	Output Low	Output Data Low
1	**1**	**X**	Float	Input with float

Note

1. IOA6/TONE: IOA6 or TONE (Timer overflow divided by 2). For timer configuration, please refer to the P_09H_TIMER_SET ($0009) in the ***Timer/Counter*** for more information.
2. To implement Open drain N-MOS (ODN) and Open drain P-MOS (ODP), do the following:

Open drain N-MOS:

Open drain P-MOS:

5.2 Resistor to Frequency Converter (RFC) Function

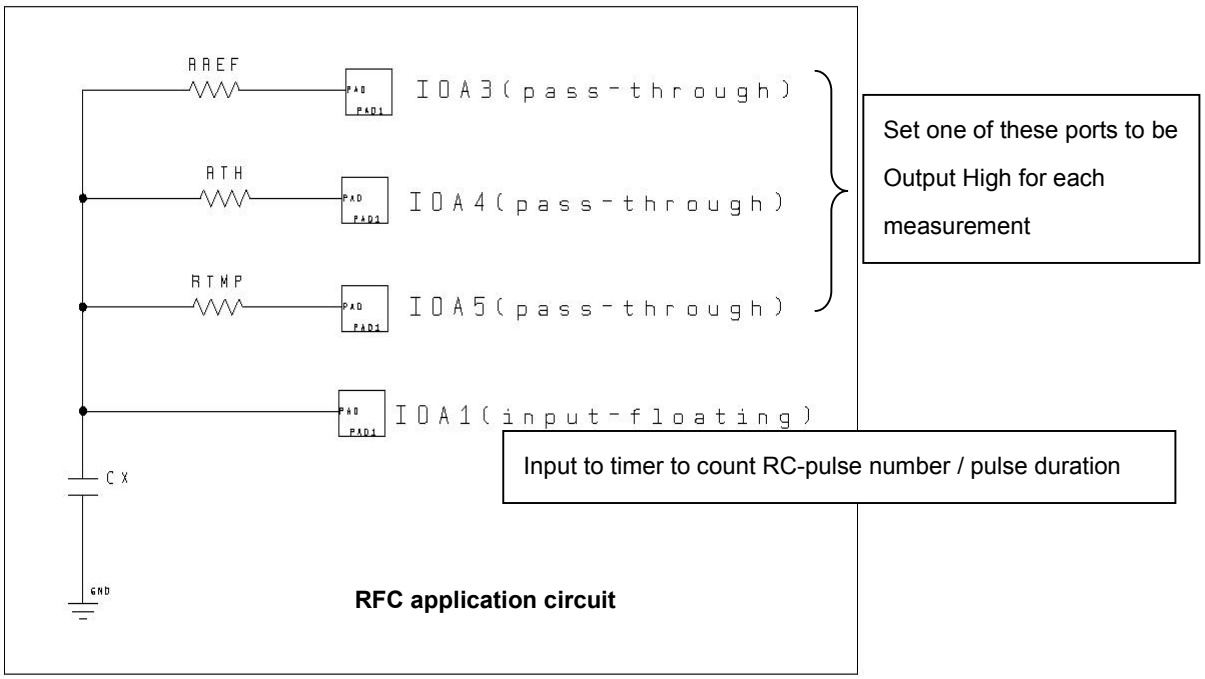
Because the heat-resistance sensor and moisture-resistance sensor will change its resistance due the change of temperature and humidity, RC time constant will also be changed. Programmers can use this identity to measure temperature or humidity.

5.2.1 P_13H_RFC_CTL ($0013): RFC Control Register

$00013	b7	b6	b5	b4	b3	b2	b1	b0
Name	-	-	-	-	-	-	-	RFCEN
R/W	-	-	-	-	-	-	-	R/W
Default	-	-	-	-	-	-	-	0

bit	Name	Description
bit0	RFCEN	0: RFC function disable 1: RFC function enable

When RFC (Resistor to Frequency Converter) function is enabled by RFCEN=1, we configure one of IOA3 (RREF), IOA4(RTH), IOA5(RTMP) to be pass-through & IOA1 (CX) to be Input-floating to make RFC function.



RFC application circuit

5.2.2 How to use RFC function

Generate RC pulse

Step 1: Set one of IOA3/IOA4/IOA5 ports to be passed-through for each measurement; the other two ports are Input-floating.

Step 2: Set IOA1 to Input floating.

Step 3: Enable RFC function ($0013 register) to generate RC-Oscillation pulse.

Measurement

Long RC time constant: use high-speed clock to sample RC-pulse in

P_09H_TIMER_SET($0009)

Step 1: GroupA timer-clock source comes from HSCK/N_TIMER (HSCK/N where N is the divisor of HSCK, selected in P_09H_TIMER_SET($0009)) .

Step 2: GroupB timer-clock source comes from EXT2 divided by 2 (EXT2CFG=1)

Step 3: Sample the number of HSCK pulses in one RC pulse.

Short RC time constant: use LSCK divided by M (where M is the divisor of LSCK, selected in P_09H_TIMER_SET($0009)) as time-base to count RC-pulse in P_09H_TIMER_SET($0009).

Step 1: GroupA timer-clock source comes from EXT2.

Step 2: GroupB timer-clock source comes from LSCK/M_TIMER (LSCK/M as time-base).

Step 3: Count the number of RC pulses in LSCK/M time-base.

5.2.3 Function description of PortA(IOA[7:0])

	Schmitt	Special Function
IOA7	-	1. I/O 2. Pass-through: IROUT
IOA6	-	1. I/O 2. Pass-through: TONE
IOA5	-	1. I/O 2. Pass-through: HSCK/N_TIMER 3. LCD output: COM8 4. Output pin for RFC application
IOA4	-	1. I/O 2. Pass-through: LSCK 3. LCD output: COM11 4. Output pin for RFC application
IOA3	-	1. I/O 2. LCD output: SEG29 3. Output pin for RFC application
IOA2	-	1. I/O 2. LCD output: SEG28
IOA1	Yes	1. I/O 2. EXT2 interrupt with P/N edge 3. Timer input 4. Input pin for RFC application
IOA0	Yes	1. I/O 2. EXT1 interrupt with P/N edge 3. Timer input

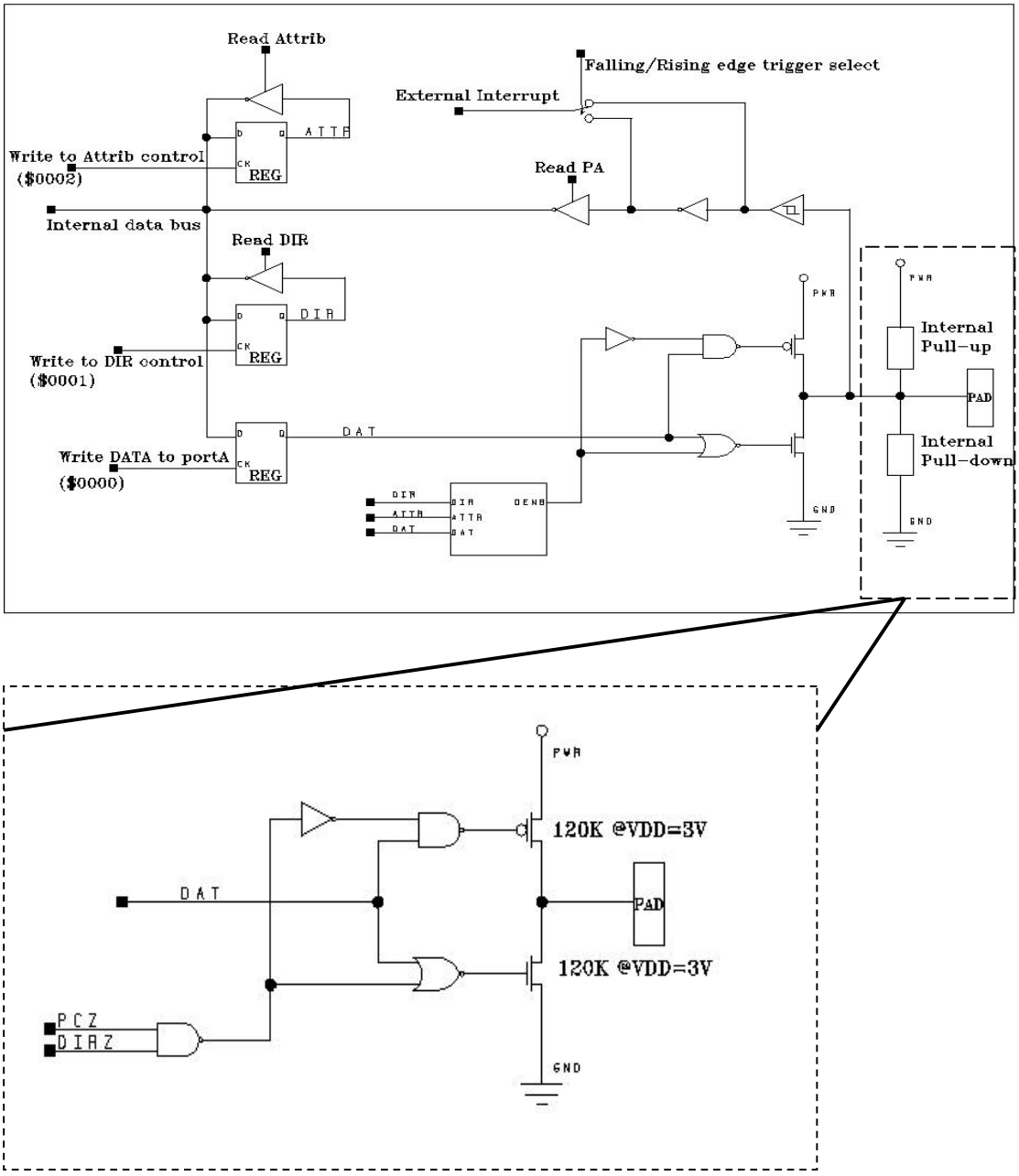
Note:

IOA[1:0] Input with Schmitt Trigger.

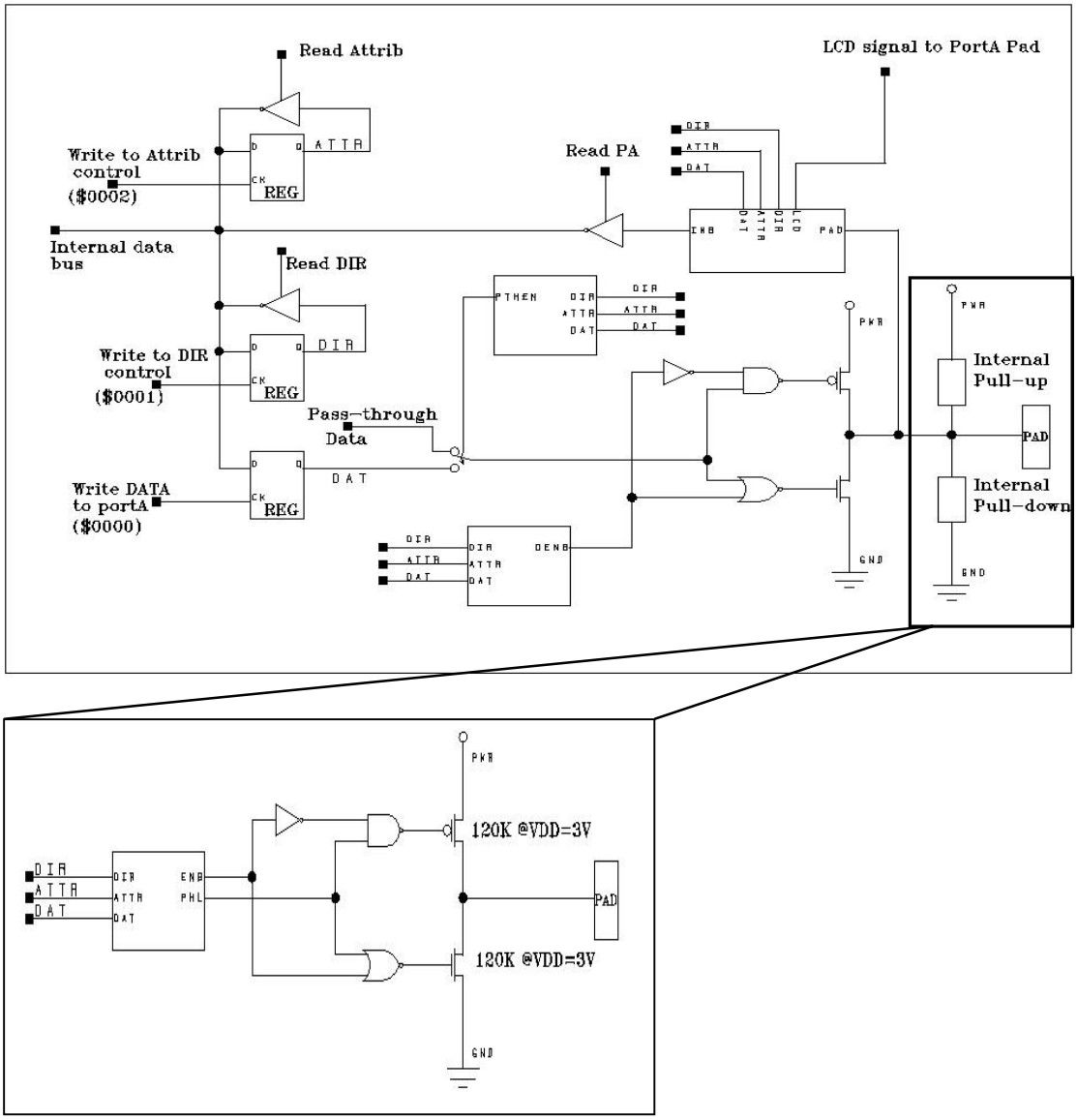
When IOA is used for COM or SEG, read operation will always return “low”. For other settings on IOA besides COM and SEG, pad status can be read back.

5.2.4 IOA Structure

IOA[1:0]



IOA[7:2]


Read Attrib
LCD signal to PortA Pad
Write to Attrib control ($0002)
Read PA
Internal data bus
Read DIR
Write to DIR control ($0001)
Pass-through Data
Write DATA to portA ($0000)
REG
ATTR
DIR
DAT
PAD
PWR
GND
Internal Pull-up
Internal Pull-down
PTHEN
DENB
ENB
PHL

PWR
120K @VDD=3V
DIR
ATTR
DAT
ENB
PHL
PAD
120K @VDD=3V
GND

5.3 PortB(INB) Control Register

INB[7:0]: Input Only with pull-low & wakeup function

Relevant Registers: P_03H_INB_Data ($0003), P_10H_IO_Config ($0010)

5.3.1 P_03H_INB_Data ($0003)

Write to latch INB data for key-change function and read data from INB pad.

$0001	b7	b6	b5	b4	b3	b2	b1	b0
Name	INBDAT7	INBDAT6	INBDAT5	INBDAT4	INBDAT3	INBDAT2	INBDAT1	INBDAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

5.3.2 P_10H_IO_Config ($0010)

Configuration register of INB & IOA

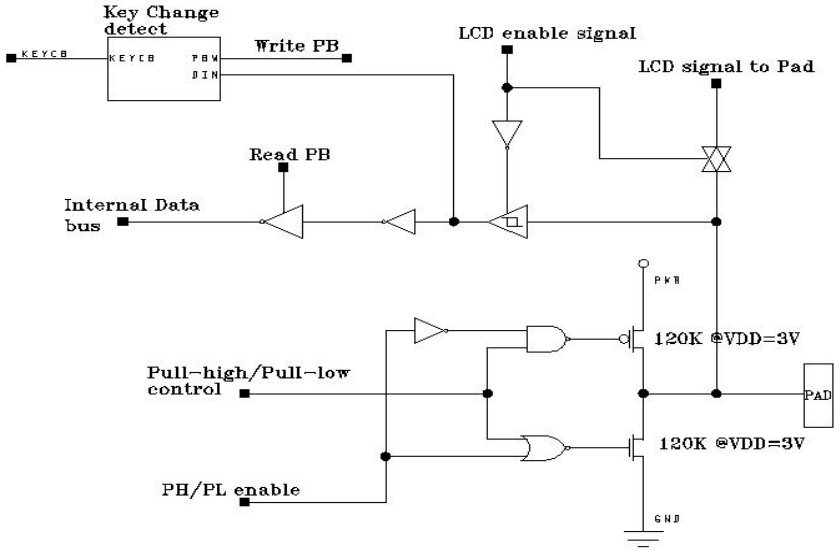
$0001	b7	b6	b5	b4	b3	b2	b1	b0
Name	EXT2EDG	EXT1EDG	INBSET5	INBSET4	INBSET3	INBSET2	INBSET1	INBSET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
b0	INBSET0	0: INB0 input with pull-low; 1: INB0 input with pull-high
b1	INBSET1	0: INB1 input with pull-low; 1: INB1 input with pull-high
b2	INBSET2	0: INB2 & INB3 input with pull-low; 1: INB2 & INB3 input with pull-high
b3	INBSET3	0: INB4 ~ INB7 input with pull-low; 1: INB4 ~ INB7 input with pull-high
b4	INBSET4	0: INB3=INB3; 1: INB3 as LCD output (SEG30/COM9)
b5	INBSET5	0: INB4=INB4, 1: INB4 as LCD output (SEG31/COM10)
b6	EXT1EDG	0: IOA0 (EXT1) falling edge interrupt; 1: IOA0 (EXT1) rising edge interrupt
b7	EXT2EDG	0: IOA1 (EXT2) falling edge interrupt; 1: IOA1 (EXT2) rising edge interrupt

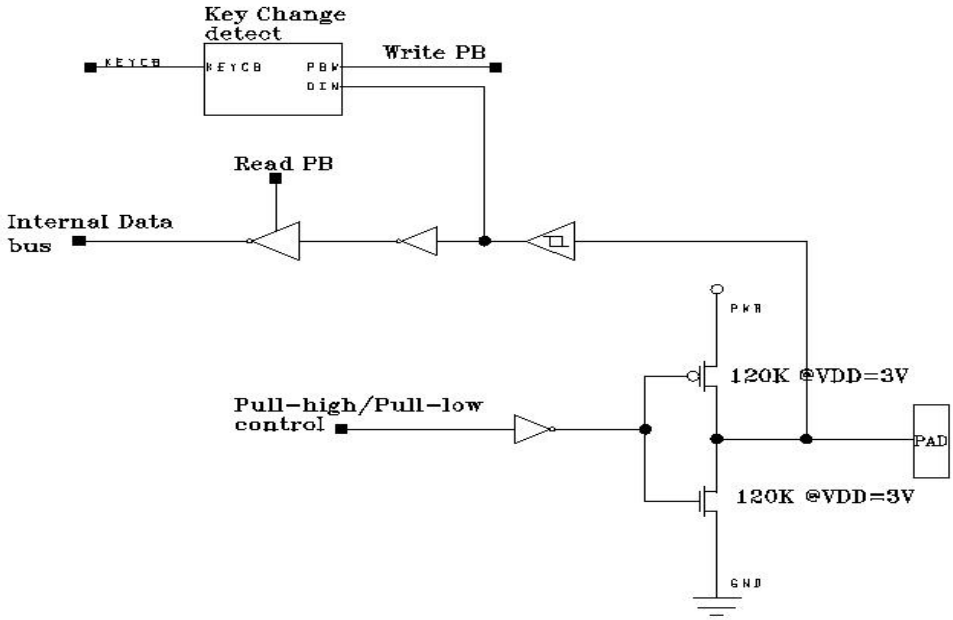
Note: When INB is used for COM or SEG, the read operation will always return “low”. For other settings on INB besides the COM and SEG, the pad status can be read back.

5.3.3 INB Structure

INB[7:3]



INB[2:0]



6 System Control

6.1 System Control

6.1.1 P_0FH_SYS_SWITCH ($000F)

Set the system operation mode, and it is a two write-operation port.

(1). First write: write $000F register with correct patterns (PAT[6:0])

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0

(2). Second write: write $000F register with Data-bit and correct patterns (PAT[6:0]) to set function-bit.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DATA	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0

Data to set function bit

FUNCTION	PATTERN	COMMENT
WAIT mode Control	1st Write: X0000001 2nd Write: D0001110 D: 0→Normal; 1→ Wait Mode	Stop CPU clock only, HSCK/LSCK sources are still ON
HSCK Control	1st Write : X0000010 2nd Write : D0001101 D : 0→Turn-ON; 1→ Turn-OFF	If CPU clock is from HSCK, STOP HSCK ➔ system enter Halt mode (LSCK is still ON)
LSCK Control	1st Write : X0000011 2nd Write : D0001100 D : 0→Turn-ON; 1→ Turn-OFF	Stop LSCK ➔ system enter Standby mode
Watchdog clear Control	1st Write: X0000100 2nd Write: D0001011 D: 0→No-Clear; 1→ Clear WDOG	
X32K mode Control	1st Write: X0000101 2nd Write: D0001010 D: 0→weak mode 1→ strong mode	
Wakeup Control	1st Write: X0000110 2nd Write: D0001001 D: 0→ Wakeup to CPU-Reset 1→ Wakeup to Next-instruction	

6.1.2 P_0FH_SYS_SWITCH ($000F)

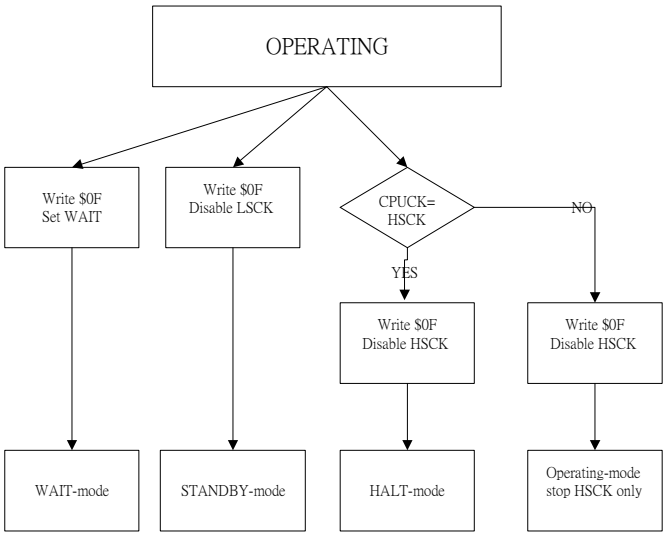
System state read back

READ FROM P_0FH_SYS_SWITCH ($000F)	
BIT	**STATUS**
b0	0:HSCk is still ON 1:HSCK is OFF
b1	0:LSCK is in weak mode 1:LSCK is in strong mode
b2	0:Wakeup to CPU-Reset 1:Wakeup to next-instruction
b3	N/A
b4	N/A
b5	N/A
b6	N/A
b7	N/A

Description:

1. The P_0FH_SYS_SWITCH ($000F) is a two-stage control port. A successful writing of the first stage makes the 2nd stage to be valid. Firmware must write to setup this port in the 2nd stage. The b7 is the data bit for the second stage writing operation.
2. The X32K crystal initially starts running at strong mode and will change to weak mode after 250ms automatically when X32K crystal is turned on (This will not change the setting in $0F weak/strong mode setting). Program will be executed after crystal oscillation is stabilized.
3. Using PLL for IR or Timer source, user's program must delay at least 8ms for the stabilization of the PLL circuit at the moment of PLL start running.
4. If no any wakeup source is configured, it is unable to enter WAIT/HALT/STANDBY mode.
5. Setting WAIT/HSCK/LSCK control bit to enter WAIT/HALT/STANDBY mode.
6. Waking up from standby mode, the **P_05H_CPU_CLK ($0005)** will be reset to the default value (HSCK/16). In wait and halt modes, the **P_05H_CPU_CLK ($0005)** will remain the same state.

Mode	Description	Action
Operating	Normal operating mode	---
WAIT	CPU OFF / all clock sources are still ON	Configure $0F register to set WAIT mode.
HALT	CPU OFF/ HSCK OFF, 32768 still ON	Configure $0F register to stop HSCk when CPU clock is HSCK.
STANDBY	CPU OFF/All clock-sources OFF	Configure $0F register to stop LSCK regardless where the CPU clock comes from HSCK or LSCK.



6.2 Reset Flags

6.2.1 P_12H_RST_FG ($0012)

$00012	b7	b6	b5	b4	b3	b2	b1	b0
Name	-	-	-	LVR	IAR	WDOG	RESETP	POR
R/W	-	-	-	R	R	R	R	R
Default	-	-	-	0	0	0	0	0

b0: Power on reset

b1: External pin reset

b2: Watchdog reset

b3: Error-address reset

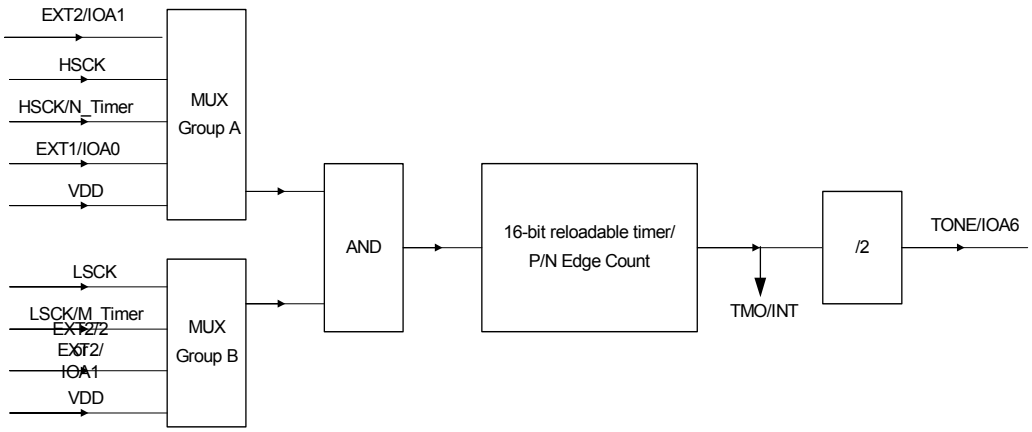
b4: Low voltage reset

Note:

1. All reset flags can be cleared by reading $12.
2. Power-on reset & external pin reset will reset low-voltage, watchdog, and error-address reset.
3. Power-on reset, external pin reset, and low voltage reset will reset entire system (all ports also are reset). Others reset functions only reset CPU (ports will not be reset).

7 Timer/Counter

7.1 Timer Structure



7.2 Timer Setup & Initialization

7.2.1 P_09H_TIMER_SET ($0009): Set the timer/counter configuration

$0009	b7	b6	b5	b4	b3	b2	b1	b0
Name	TMREN	TEDGE	EXT2CFG	TCKB1	TCKB0	TCKA2	TCKA1	TCKA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Timer-Clock setting groupA

Bit / CLK source	b2 (TCKA2)	b1 (TCKA1)	b0 (TCKA0)
HSCK	0	0	0
HSCK/N_TIMER	0	0	1
EXT1	0	1	0
VDD	0	1	1
EXT2	1	X	X

Note:

1. HSCK/N_TIMER is HSCK/N clock source set by P_0CH_Timer_INT1 ($000C).
2. EXT1: rising or falling edge interrupt from IOA0 with Glitch-Filter.

Timer-Clock setting groupB

bit / CLK source	b4 (TCKB1)	b3 (TCKB0)
LSCK	0	0
LSCK/M_TIMER	0	1
EXT2	1	0
VDD	1	1

Note:

1. LSCK/M_TIMER is LSCK/M clock source set by P_0DH_Timer_INT2 ($000D).
2. EXT2: Rising or falling edge interrupt from IOA1 with Glitch-Filter and Ext2 can be used as RC-pulse input in RFC function.

Bit	Name	Description
b5	**EXT2CFG**	0: EXT2 (as Timer-clock) 1: EXT2 divided by 2 (as Timer-clock)
b6	**TEDGE**	0: falling edge up-count 1: rising edge up-count
b7	**TMREN**	0: Disable Timer 1: Enable Timer

7.3 Timer/Interrupt Clock Sources

A. HSCK sources for timer, interrupt

7.3.1 P_0CH_TIMER_INT1 ($000C)

Set HSCK/N as the Timer/Interrupt input source

$000C	b7	b6	b5	b4	b3	b2	b1	b0
Name	-	-	-	LINT1	LINT0	LTIM2	LTIM1	LTIM0
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0

HSCK/N Clock for Timer:

bit / HSCK/N_Timer	b2 (LTIM2)	b1 (LTIM1)	b0 (LTIM0)
37.9K/16	0	0	0
37.9K/8	0	0	1

bit / HSCK/N_Timer	b2 (LTIM2)	b1 (LTIM1)	b0 (LTIM0)
37.9K/4	0	1	0
37.9K/2	0	1	1
37.9K	1	0	0
HSCK/8	1	0	1
HSCK/4	1	1	0
HSCK/2	1	1	1

HSCK/N Clock for Interrupt

bit / HSCK/N_INT	b4 (LINT1)	b3 (LINT0)
37.9K/16	0	0
37.9K/8	0	1
37.9K/4	1	0
37.9K/2	1	1

B. LSCK(32768) sources for timer, interrupt sources

7.3.2 P_0DH_TIMER_INT2 ($000D)

Set 32768Hz/M as the Timer/Interrupt input source where M is frequency divisor.

$000D	b7	b6	b5	b4	b3	b2	b1	b0
Name	-	32KINT2	32KINT1	32KINT0	RTC	32KTIM2	32KTIM1	32KTIM0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	-	0	0	0	0	0	0	0

LSCK/M clock for Timer:

LSCK/M_Timer	b2 (32KTIM2)	b1 (32KTIM1)	b0 (32KTIM0)
4 Hz	0	0	0
8 Hz	0	0	1
16 Hz	0	1	0
32 Hz	0	1	1
64 Hz	1	0	0
128 Hz	1	0	1
1024 Hz	1	1	0
4096 Hz	1	1	1

Real-Time Clock setting

Bit	Name	Description
b3	RTC	0: 2 Hz 1: 1 Hz

LSCK/M clock for Interrupt:

LSCK/M_INT	b6 (32KINT2)	b5 (32KINT1)	b4 (32KINT0)
4 Hz	0	0	0
8 Hz	0	0	1
16 Hz	0	1	0
32 Hz	0	1	1
64 Hz	1	0	0
128 Hz	1	0	1
1024 Hz	1	1	0
4096 Hz	1	1	1

7.4 Timer Data Register

7.4.1 P_0AH_TML_LATCH ($000A)

Set/load timer data into Timer b7 ~ b0 (low byte).

$000A	b7	b6	b5	b4	b3	b2	b1	b0
Name	TMLL7	TMLL6	TMLL5	TMLL4	TMLL3	TMLL2	TMLL1	TMLL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

7.4.2 P_0BH_TMH_LATCH ($000B)

Set/load timer data into Timer b15 ~ b8 (high byte).

$000B	b7	b6	b5	b4	b3	b2	b1	b0
Name	TMHL7	TMHL6	TMHL5	TMHL4	TMHL3	TMHL2	TMHL1	TMHL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Note. 1. 16-bit reloadable rising or falling edge up-count Timer/Counter

2. When preloaded value is loaded into Timer, write P_0AH_TML_Latch first and next write P_0BH_TMH_Latch to load timer data to timer.

8 LCD

8.1 LCD RAM mapping

	SEG0~SEG7	SEG8~SEG15	SEG16~SEG23	SEG24~SEG31
	b0~b7	b0~b7	b0~b7	b0~b7
COM0	$50	$51	$52	$53
COM1	$54	$55	$56	$57
COM2	$58	$59	$5A	$5B
COM3	$5C	$5D	$5E	$5F
COM4	$60	$61	$62	$63
COM5	$64	$65	$66	$67
COM6	$68	$69	$6A	$6B
COM7	$6C	$6D	$6E	$6F
COM8	$70	$71	$72	$73
COM9	$74	$75	$76	$77
COM10	$78	$79	$7A	$7B
COM11	$7C	$7D	$7E	$7F

8.2 Control registers

LCD related register: P_04H_LCD_CTL ($0004), P_11H_LCDCK_CTL ($0011)

8.2.1 Port_LCD_CTL ($0004)

LCD Control register

$0004	b7	b6	b5	b4	b3	b2	b1	b0
Name	PUMPCK	LCDMOD1	LCDMOD0	BIAS1	BIAS0	DUTY2	DUTY1	DUTY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Duty Control of LCD

BIT / Mode	b2 (DUTY2)	b1 (DUTY1)	b0 (DUTY0)
1/3 Duty	0	0	0
1/4 Duty	0	0	1
1/5 Duty	0	1	0
1/8 Duty	0	1	1
1/9 Duty	1	0	0
1/10 Duty	1	0	1
1/11 Duty	1	1	0
1/12 Duty	1	1	1

Bias Control of LCD

bit / Mode	b4 (BIAS1)	b3 (BIAS0)
1/2 Bias	0	0
1/3 Bias	0	1
1/4 Bias	1	X

Note:

1. If 1/4 bias is selected, the pins of V3_INB5, CPU3_INB6 and CPU4_INB7 will not perform as ordinary I/O functions; instead, they are used for V3, CPU3 and CPU4 for bias circuit. For 1/2 and 1/3 bias options, these pins are used for I/O purpose.
2. When duty is over 1/8, Sunplus recommends using 1/4 bias for LCD quality improvement.

LCD operating mode

BIT / Mode	b6 (LCDMOD1)	b5 (LCDMOD0)
LCD OFF	0	0
NORMAL	0	1
All dots ON	1	0
All dots OFF	1	1

Default: LCD off, meaning both common and segment are remained low.

LCD pump clock control

Bit / Mode	b7 (PUMPCK)
Pump clock = 8K	0
Pump clock = 32K	1

Note: Wait bias setting to be stabilized (a completed frame) and next turn the LCD on.

Note 2: LCD off voltage, SEG = Low (0V) & COM = Low (0V)

8.2.2 LCD clock control

Port_LCDCK_CTL ($0011): LCD clock control register; tune LCD frame-rate with smaller step.

$0011	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Name	-	-	-	-	LCK3	LCK2	LCK1	LCK0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Default	-	-	-	-	0	0	0	0

Frame-rate tuning range: approx. 40Hz ~ 100Hz with different steps for various duties

For 1/3 bias, 1/4bias, and 1/5bias:

BIT[3:0] (LCK[3:0])	Frame Rate(Hz)		
	1/3 bias	1/4 bias	1/5 bias
1111	**N/A**	**N/A**	**N/A**
1110	**N/A**	**N/A**	**N/A**
1101	**N/A**	**N/A**	**N/A**
1100	**N/A**	**N/A**	102.4
1011	**N/A**	102.3	81.9
1010	**N/A**	85.3	68.3
1001	97.5	73.1	58.5
1000	85.3	64.0	51.2
0111	75.8	56.9	45.5
0110	68.3	51.2	41.0
0101	62.1	46.6	**N/A**
0100	56.9	42.7	**N/A**
0011	52.5	39.4	**N/A**
0010	48.8	**N/A**	**N/A**
0001	45.5	**N/A**	**N/A**
0000	42.7	**N/A**	**N/A**

NA: Sunplus recommends not to give any value to the b[3:0]

For 1/8 bias~1/12 bias

BIT[3:0] (LCK[3:0])	Frame Rate(Hz)				
	1/8 bias	1/9 bias	1/10 bias	1/11 bias	1/12 bias
1111	**NA**	**NA**	**NA**	**NA**	**NA**
1110	**NA**	**NA**	**NA**	**NA**	**NA**
1101	**NA**	**NA**	**NA**	**NA**	**NA**
1100	**NA**	**NA**	102.4	93.1	85.3
1011	102.4	91.0	81.9	74.5	68.3
1010	85.3	75.9	68.3	62.1	56.9
1001	73.2	65.0	58.5	53.2	48.8
1000	64.0	56.9	51.2	46.5	42.7
0111	56.9	50.6	45.5	41.4	**NA**
0110	51.2	45.5	41.0	**NA**	**NA**
0101	46.5	41.4	**NA**	**NA**	**NA**
0100	42.7	37.9	**NA**	**NA**	**NA**
0011	39.4	**NA**	**NA**	**NA**	**NA**
0010	**NA**	**NA**	**NA**	**NA**	**NA**
0001	**NA**	**NA**	**NA**	**NA**	**NA**
0000	**NA**	**NA**	**NA**	**NA**	**NA**

NA: Sunplus recommends not to give any value to the b[3:0].

8.3 Multiple functions (I/O, segment & common sharing)

8.3.1 LCD dot & I/O

LCD dots	**IO Used**
360 dots (12 x 30)	INB0 ~ INB2, IOA0, IOA1, IOA6, IOA7
330 dots (11 x 30)	INB0 ~ INB2, IOA0, IOA1, IOA4, IOA6, IOA7
300 dots (10 x 30)	INB0~INB2, INB4, IOA0, IOA1, IOA4, IOA6, IOA7
288 dots (9 x 32)	INB0 ~ INB2, IOA0, IOA1, IOA4, IOA6, IOA7 (3 Input & 5 IO)
256 dots (8 x 32)	INB0 ~ INB2, IOA0, IOA1, IOA4 ~ IOA7 (3 Input & 6 IO)
160 dots (5 x 32)	INB0 ~ INB3, INB5 ~ INB7, IOA0 ~ IOA7 (7 Input & 8 IO)
128 dots (4 x 32)	INB0 ~ INB7, IOA0 ~ IOA7 (8 Input & 8 IO)
96 dots (3 x 32)	INB0 ~ INB7, IOA0 ~ IOA7 (8 Input & 8 IO)

8.3.2 LCD mapping with dot resolution

Dots / Signals	96 dots (3 x 32)	128 dots (4 x 32)	160 dots (5 x 32)	256 dots (8 x 32)	288 dots (9 x 32)	300 dots (10 x 30)	330 dots (11 x 30)	360 dots (12 x 30)
COM[0:2]	COM[0:2]	COM[0:2]	COM[0:2]	COM[0:2]	COM[0:2]	COM[0:2]	COM[0:2]	COM[0:2]
COM3	-	COM3	COM3	COM3	COM3	COM3	COM3	COM3
COM4	-	-	COM4_ SEG31	COM4_ SEG31	COM4_ SEG31	COM4_ SEG31	COM4_ SEG31	COM4_ SEG31
COM5	-	-	-	COM5_ SEG30	COM5_ SEG30	COM5_ SEG30	COM5_ SEG30	COM5_ SEG30
COM6	-	-	-	COM6_ SEG29	COM6_ SEG29	COM6_ SEG29	COM6_ SEG29	COM6_ SEG29
COM7	-	-	-	COM7_ SEG28	COM7_ SEG28	COM7_ SEG28	COM7_ SEG28	COM7_ SEG28
COM8	-	-	-	-	IOA5	IOA5	IOA5	IOA5
COM9	-	-	-	-	-	INB3	INB3	INB3
COM10	-	-	-	-	-	-	INB4	INB4
COM11	-	-	-	-	-	-	-	IOA4
SEG[0:27]	SEG[0:27]	SEG[0:27]	SEG[0:27]	SEG[0:27]	SEG[0:27]	SEG[0:27]	SEG[0:27]	SEG[0:27]
SEG28	COM7_ SEG28	COM7_ SEG28	COM7_ SEG28	IOA2	IOA2	IOA2	IOA2	IOA2
SEG29	COM6_ SEG29	COM6_ SEG29	COM6_ SEG29	IOA3	IOA3	IOA3	IOA3	IOA3
SEG30	COM5_ SEG30	COM5_ SEG30	COM5_ SEG30	INB3	INB3	-	-	-
SEG31	COM4_ SEG31	COM4_ SEG31	INB4	INB4	INB4	-	-	-

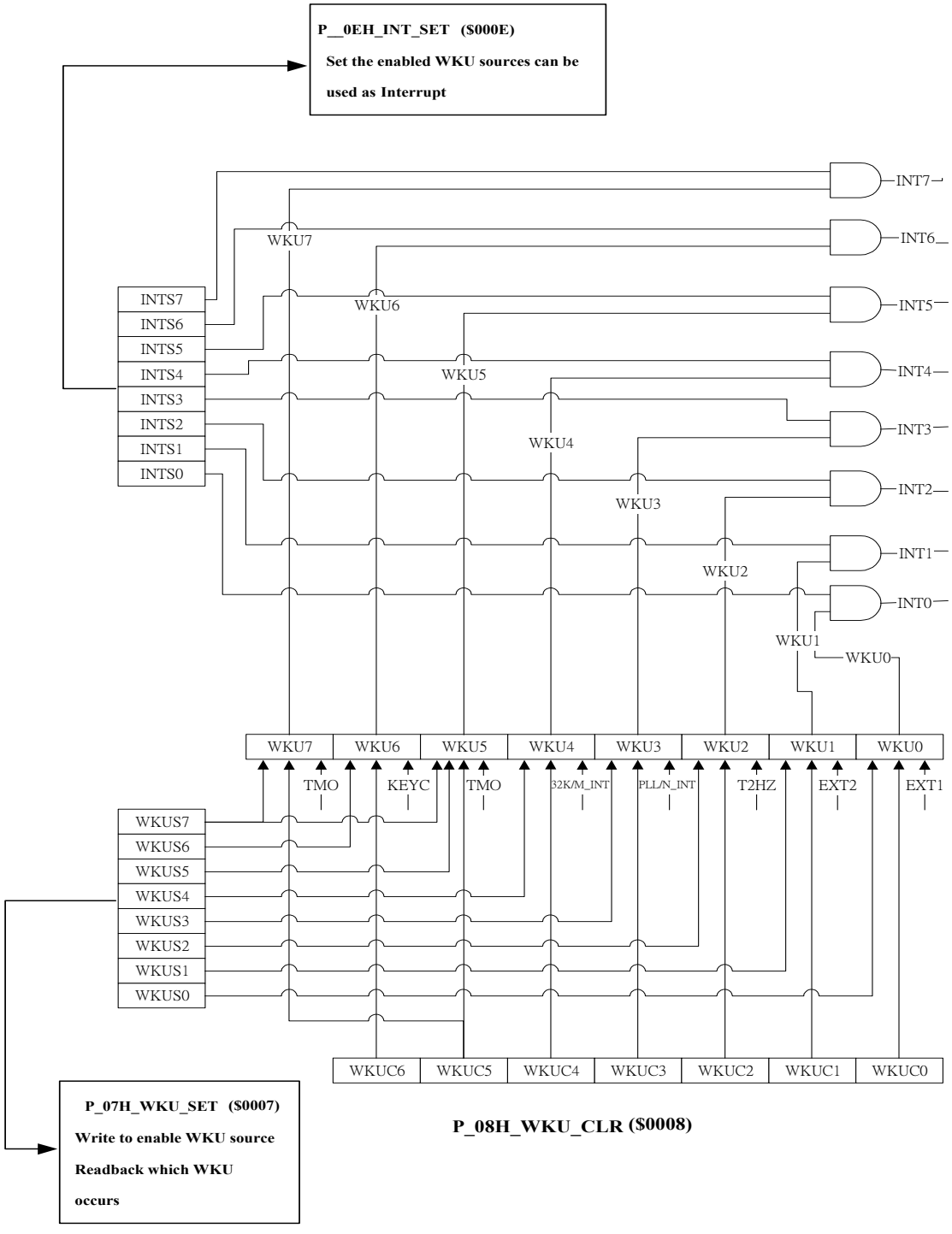
: indicates physical pin on the chip.

EX: In 96 dots matrix, the signal of SEG31 is outputted from COM4_SEG31.

EX: In 160 dots matrix, the signal of COM4 is outputted from COM4_SEG31.

9 Wakeup / Interrupt

9.1 Wakeup/Interrupt Structure Diagram



9.2 Wakeup/Interrupt Control registers

Related registers: P_07H_WKU_SET ($0007), P_08H_WKU_CLR ($0008), P_0EH_INT_SET($000E)

9.2.1 P_07H_WKU_SET ($0007)

Write register to enable/disable wakeup sources bit by bit and identify which wakeup source occurs.

$0007	b7	b6	b5	b4	b3	B2	b1	b0
Name	WKUS7	WKUS6	WKUS5	WKUS4	WKUS3	WKUS2	WKUS1	WKUS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit	Name	Description
b0	WKUS0	Wakeup source: EXT1(IOA0); 0: disabled, 1: enabled Falling (default)/Rising edge from IOA0 (set by Port_IO_Config($0010), b6)
b1	WKUS1	Wakeup source: EXT2(IOA1); 0: disabled, 1: enabled Falling (default)/Rising edge from IOA1 (set by Port_IO_Config($0010), b7)
b2	WKUS2	Wakeup source: 2Hz or 1Hz (set by P_0DH_Timer_INT2($000D), b3) 0: disabled, 1: enabled
b3	WKUS3	Wakeup source: HSCK/N_INT (37.9KHz divided by 2/4/8/16, set by P_0CH_Timer_INT1 ($000C), b[4:3]) 0: disabled, 1: enabled
b4	WKUS4	Wakeup source: LSCK/M_INT (4096/1024/128/64/32/16/8/4 Hz, set by P_0DH_Timer_INT2($000D), b[6:4]) ; 0: disabled, 1: enabled
b5	WKUS5	Wakeup source: Timer Overflow IRQ 0: disabled, 1: enabled
b6	WKUS6	Wakeup source: key change (INB[7:0]) 0: disabled, 1: enabled
b7	WKUS7	0: Timer overflow NMI disabled (timer overflow as IRQ) 1: Timer overflow NMI enabled (WKUS5 will be auto-disabled) Read for checking NMI occurrence.

Note:

1. When WKUC5 clears TMO (timer overflow), it will also clear WKU7 (NMI).
2. The WKUS7 configures TMO as IRQ (WKUS7=0) or NMI (WKUS7=1). If WKUS7 is configured TMO as NMI (WKUS7=1), WKUC5 (TMO IRQ) will be disabled automatically.

9.2.2 Port_WKU_CLR ($0008)

$0008	b7	b6	b5	b4	b3	b2	b1	b0
Name	-	WKUC6	WKUC5	WKUC4	WKUC3	WKUC2	WKUC1	WKUC0
R/W	-	W	W	W	W	W	W	W
Default	-	0	0	0	0	0	0	0

Bit	Name	Description
b0	WKUC0	Clear Wakeup source: EXT1(IOA0)
b1	WKUC1	Clear Wakeup source: EXT2(IOA1)
b2	WKUC2	Clear Wakeup source: 2Hz or 1Hz (set by P_0DH_Timer_INT2($000D), Bit3)
B3	WKUC3	Clear Wakeup source: HSCK/N_INT (37.9KHz divided by 2/4/8/16, set by P_0CH_Timer_INT1($000C), Bit[4:3])
B4	WKUC4	Clear Wakeup source: LSCK/M_INT(4096/1024/128/64/32/16/8/4 Hz, set by P_0DH_Timer_INT2($000D), Bit[6:4])
B5	WKUC5	Clear Wakeup source of Timer Overflow The clearance will also clear both TMO IRQ & NMI.
b6	WKUC6	Clear Wakeup source: Key change wakeup (INB[7:0])
b7	-	N/A

Note

1. All interrupts will wake CPU up and execute program from reset or next instruction (see PORT_SYS_SWITCH).
2. Write data into this register will clear both wakeup and interrupt flags.

9.2.3 P_0EH_INT_SET($000E)

Set wakeup sources as interrupt

$000E	b7	b6	b5	b4	b3	b2	b1	b0
Name	INTS7	INTS6	INTS5	INTS4	INTS3	INTS2	INTS1	INTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit	Name	Description
b0	INTS0	0: EXT1 is used for wakeup source only. 1: EXT1 is used for both wakeup & IRQ
b1	INTS1	0: EXT2 is used for wakeup source only. 1: EXT2 is used for both wakeup & IRQ.
b2	INTS2	0: 2Hz or 1Hz is used for wakeup source only. 1: 2Hz or 1Hz is used for both wakeup & IRQ.

b3	**INTS3**	0:HSCK/N_INT is used for wakeup source only. 1: HSCK/N_INT is used for both wakeup $ IRQ.
b4	**INTS4**	0: LSCK/M_INT is used for wakeup source only. 1: LSCK/M_INT is used for both wakeup & IRQ.
b5	**INTS5**	0: TMO is used for wakeup source only. 1: TMO is used for both wakeup & IRQ.
b6	**INTS6**	0: Key-change is used for wakeup source only. 1: Key-change is used for both wakeup and IRQ.
b7	**INTS7**	0: TMO NMI is used for wakeup source only. 1: TMO NMI is used for both wakeup & NMI.

Notice: Suppose the wakeup source is used for IRQ and also if the program executes from reset after wakeup is accepted, IRQ will not be generated till a CLI instruction is met. The reason is that CPU will set the CPU internal interrupt flag (I) when reset operation is performed.

10 Remote Control

10.1 Control registers

10.1.1 P_06H_DUTY_CTL ($0006)

IROUT control register

$0006	b7	b6	b5	b4	b3	b2	b1	b0
Name	-	-	-	IREN	IRCTL	IRDTY2	IRDTY1	IRDTY0
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Default	-	-	-	0	0	0	0	0

IROUT pulse duty control

Bit / Mode	b2 (IRDTY2)	b1 (IRDTY1)	b0 (IRDTY0)
0/8 Duty	0	0	0
1/8 Duty	0	0	1
2/8 Duty	0	1	0
3/8 Duty	0	1	1
4/8 Duty	1	0	0
5/8 Duty	1	0	1
6/8 Duty	1	1	0
7/8 Duty	1	1	1

Note: 1/8 Duty → 1/8 duty high, 7/8 duty Low

Bit	Name	Description
b3	IRCTL	0: Software control IROUT 1: Timer overflow for IROUT
b4	IREN	0: IROUT=0 1: IROUT=37.9KHz

Note:

For the initialization of using timer overflow as the IR control, setting IREN=0 first and then setting IREN=1 will generate a 37.9KHz signal at the first timer overflow occurrence. In contrast, if setting IREN=0, but not setting IREN back to “1”, the 37.9KHz will not be generated at any time.

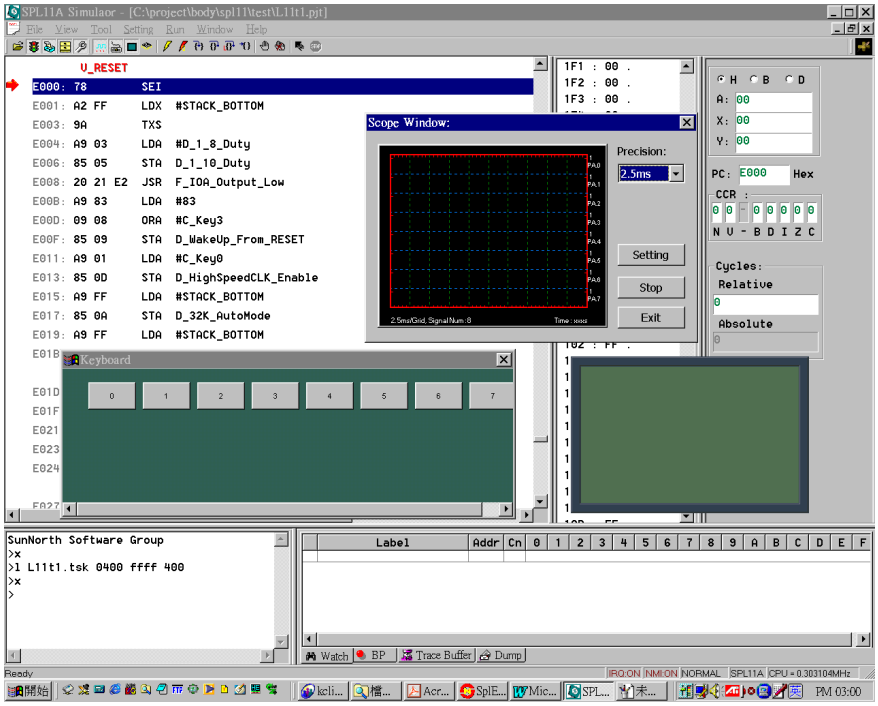
11 Development System

The SPL11A development system consists of a simulator, OTP writer with a COB/QFP package, and demo board.

11.1 SPL11A Simulator

The SPL11A development system includes a simulator (see figure below) to emulate the functionality of SPL11A, developed by programmer. For more information about how to use this simulator, please refer to ***SPL11A simulator User's Manual.***

Caution: After user's program is fully tested on the simulator, testing on SPL11A OTP demo board is also required to ensure the functionality.



11.2 OTP Writer and demo board

The SPL11A development should also include an OTP writer to program SPL11A OTP chip and a demo board to demonstrate the designed functions. For more information about how to program the SPL11A OTP and use of demo board, please refer to ***Sunplus OTP/MTP Writer User's Manual.***

12 Mask/Bonding option

12.1 Mask options for ROM version of SPL11A

- PLL or Rosc
- X32K or R32K
- Low voltage reset enable or disable

12.2 Bonding options for OTP version of SPL11A

Option / Pin Name	Bonding Low (No Bonding)	Bonding High	Description
HCKOPT	Rosc	PLL	---
LCKOPT	32K crystal	32K Rosc	---
LVROFF	Low voltage reset on	Low voltage reset off	Low voltage reset at 2.4V

12.3 Default status of pins

Pin	Default state
IOA (IOA0 ~ IOA7)	Input with pull-low
INB (IOB0 ~ IOB7)	Input with pull-low
CUP3/INB6	INB6 (determined by bias)
CUP4/INB7	INB7 (determined by bias)
V3/INB5	INB5 (determined by bias)
COM4/SEG31	SEG31 (determined by duty)
COM5/SEG30	SEG30 (determined by duty)
COM6/SEG29	SEG29 (determined by duty)
COM7/SEG28	SEG28 (determined by duty)
INB3/SEG30/COM9	INB3 (determined by duty)
INB4/SEG31/COM10	INB4 (determined by duty)
IOA4/COM11	IOA4 (determined by duty)
IOA5/COM8	IOA5 (determined by duty)
VCOIN/ROSC	ROSC (HCKOPT =Low) in OTP version
X32I/R32I	X32I (LCKOPT =Low) in OTP version.

13 Appendix

13.1 Port and Memory Map

Port Address	Description
$0000	P_00H_IOA_Data
$0001	P_01HIOA_Dir
$0002	P_02H_IOA_Attrib
$0003	P_03H_INB_Data
$0004	P_04H_LCD_CTL
$0005	P_05H_CPU_CLK
$0006	P_06H_DUTY_CTL
$0007	P_07H_WKU_SET
$0008	P_08H_WKU_CLR
$0009	P_09H_TIMER_SET
$000A	P_0AH_TML_LATCH
$000B	P_0BH_TMH_LATCH
$000C	P_0CH_TIMER_INT1
$000D	P_0DH_TIMER_INT2
$000E	P_0EH_INT_SET
$000F	P_0FH_SYS_SWITCH
$0010	P_10H_IO_CONFIG
$0011	P_11H_LCDCK_CTL
$0012	P_12H_RST_FLG
$0013	P_13H_RFC_CTL
$0020 ~ $004F	Error Address 1
$0050 ~ $007F	DPRAM for LCD display
$0080 ~ $00FF	128 Byte SRAM for data & stack
$0100 ~ $01DF	Error Address 2
$01E0 ~ $01FF	32 Byte SRAM for stack (the same SRAM in $00E0 ~ $00FF)
$0400 ~ $05FF	Testing Program for Sunplus use only. Error Address 4 in normal mode
$0600 ~ $1FFF	Error Address 3
$E000 ~ $FFFF	8K EPROM
$FFF9	Secure option (bit 7)

13.2 OTP (QFP) PIN Description

Mnemonic	PIN No.	Type	Description
SEG27 – 21 SEG20 – 6 SEG5 – 0	13 - 19 25 - 39 44 - 49	O	LCD driver segment output.
COM4_SEG31	8	O	Shared pin for LCD common4 or segment31
COM5_SEG30	9	O	Shared pin for LCD common5 or segment30
COM6_SEG29	10	O	Shared pin for LCD common6 or segment29
COM7_SEG28	11	O	Shared pin for LCD common7 or segment28
COM3 - 0	49 - 52	O	LCD driver common output
V1 V2	53 54	I	Inputs for setting LCD bias
CUP1 CUP2	55 56	I	Inputs for setting LCD bias
IOA7	72	I/O	IOA port bit7, can be used to output IR carrier
IOA6	73	I/O	IOA port bit6, can be used to output tone
IOA5	74	I/O	IOA port bit5, shared pin with LCD common8 In RFC application, used as a pass-through (output) pin and connected to sensor.
IOA4	75	I/O	IOA port bit4, shared pin with LCD common11 In RFC application, used as a pass-through (output) pin and connected to sensor
IOA3	76	I/O	IOA port bit3, shared pin with LCD segment29 In RFC application, used as a pass-through (output) pin and connected to sensor.
IOA2	77	I/O	IOA port bit2, shared pin with LCD segment28.
IOA1	78	I/O	IOA port bit1, Timer external input 2, External Interrupt input 2. In RFC application, used as input-floating pin and connected to sensor & capacitor.
IOA0	79	I/O	IOA port bit0, Timer external input 1, External Interrupt input 1
CUP3_INB7	57	I	Shared pin for (1) INB input port bit7 with key-change detection (2) Input for setting LCD bias (CUP3).
CUP4_INB6	58	I	Shared pin for (1) INB input port bit6 with key-change detection (2) Input for setting LCD bias (CUP4).
V3_INB5	65	I	Shared pin for (1) INB input port bit5 with key-change detection (2) Input for setting LCD bias (V3).
INB4	7	I/O	Shared pin for (1) INB input port bit4 with key-change detection (2) LCD segment 31 (3) LCD common 10.

Mnemonic	PIN No.	Type	Description
INB3	6	I/O	Shared pin for (1) INB input port bit3 with key-change detection (2) LCD segment 30 (3) LCD common 9.
INB2	5	I	INB input port bit2 with key-change detection
INB1	4	I	INB input port bit1 with key-change detection
INB0	3	I	INB input port bit0 with key-change detection
LVROFF	1	I	LVR (Low-voltage reset) disable pin
VDDT	23	P	EPROM testing power
VPP	24	P	EPROM programming power
PIEP	40	I	EPROM parallel interface enable
X32I	51	I	32.768KHz Crystal/R-OSC Input (option)
X32O	52	O	32.768KHz crystal output
LCKOPT	61	I	Option pin for Low-speed clock selection 0: 32768 crystal; 1: 32768 R-oscillator
HCKOPT	62	I	Option pin for high-speed clock selection 0: R-oscillator; 1: 4.85MHz PLL
RESETB	66	I	External reset input pin (Low active)
VSS	69	P	Ground input
OSCPLL	70	I	PLL Input/R-OSC Input (option)
VDD	71	P	Power input
TEST	80	I	Test input

Legend: I = Input, O = Output, P = Power