



SPN2302

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2302 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

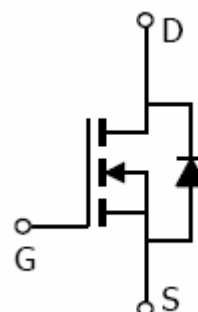
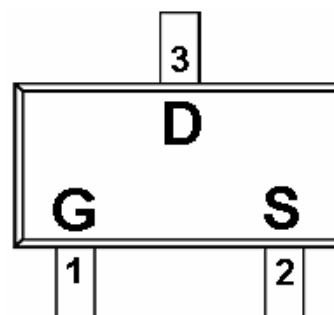
FEATURES

- ◆ 20V/3.6A, $R_{DS(ON)} = 80m\Omega @ V_{GS} = 4.5V$
- ◆ 20V/3.1A, $R_{DS(ON)} = 95m\Omega @ V_{GS} = 2.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-3L package design

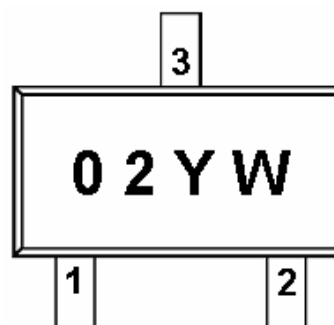
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23-3L)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2302S23RG	SOT-23-3L	02YW

Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

SPN2302S23RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25 Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	20	V
Gate –Source Voltage		V _{GSS}	±12	V
Continuous Drain Current(T _J =150)	T _A =25	I _D	2.8	A
	T _A =70		2.2	
Pulsed Drain Current		I _{DM}	10	A
Continuous Source Current(Diode Conduction)		I _S	1.6	A
Power Dissipation	T _A =25	P _D	1.25	W
	T _A =70		0.8	
Operating Junction Temperature		T _J	150	
Storage Temperature Range		T _{STG}	-55/150	
Thermal Resistance-Junction to Ambient		R _{θJA}	100	/W



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ELECTRICAL CHARACTERISTICS

(T_A=25 Unless otherwise noted)

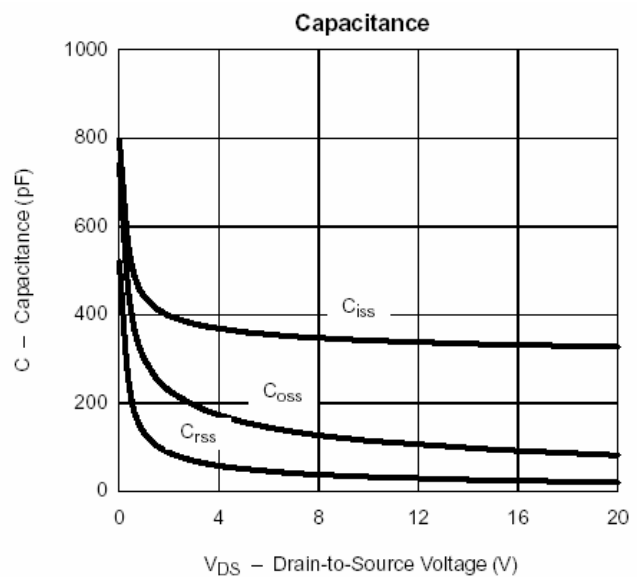
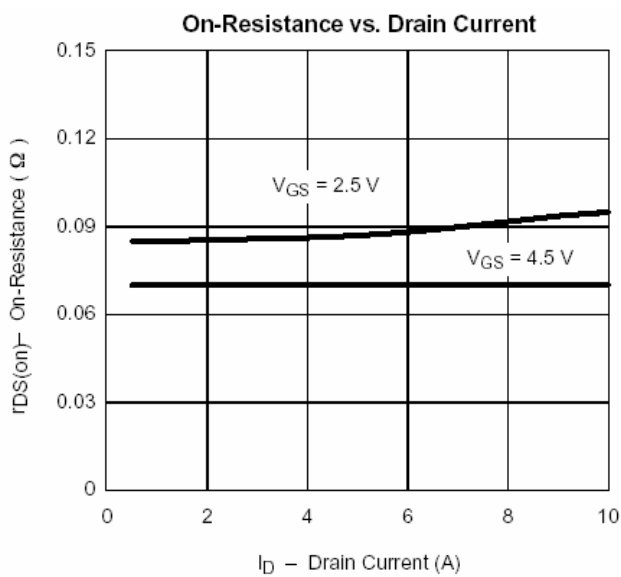
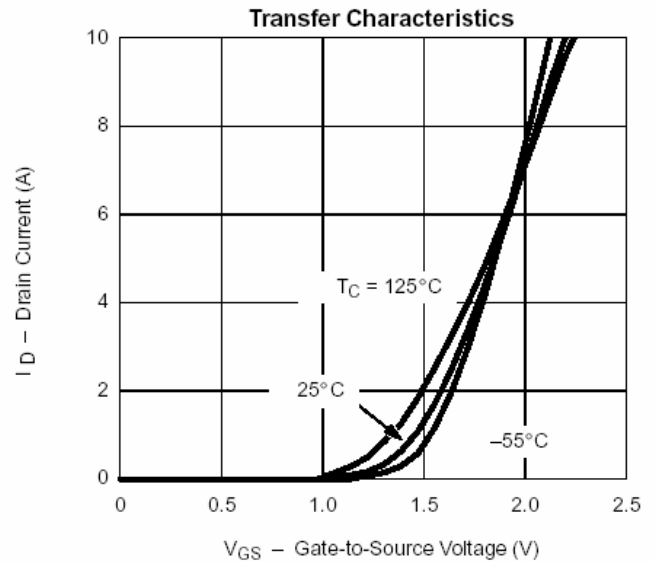
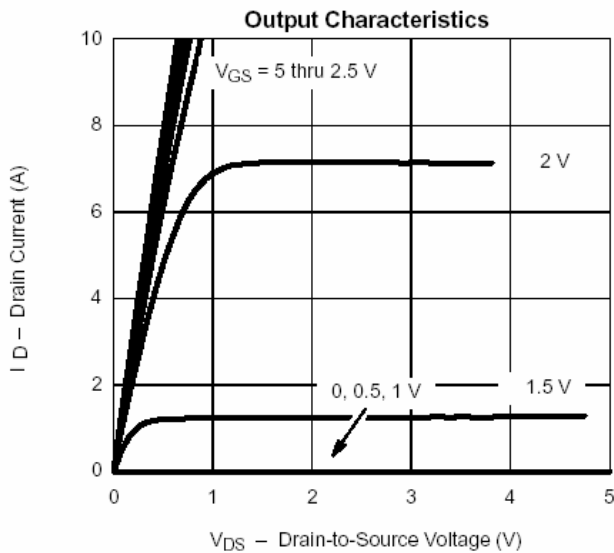
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.45		1.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	uA
		V _{DS} =20V, V _{GS} =0V T _J =55			10	
On-State Drain Current	I _{D(on)}	V _{DS} 5V, V _{GS} =4.5V	6			A
		V _{DS} 5V, V _{GS} =2.5V	4			
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =3.6A		0.050	0.080	Ω
		V _{GS} =2.5V, I _D =3.1A		0.070	0.095	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =3.6A		10		S
Diode Forward Voltage	V _{SD}	I _S =1.6A, V _{GS} =0V		0.85	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =10V, V _{GS} =4.5V I _D =3.6A		5.4	10	nC
Gate-Source Charge	Q _{gs}			0.65		
Gate-Drain Charge	Q _{gd}			1.4		
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V f=1MHz		340		pF
Output Capacitance	C _{oss}			115		
Reverse Transfer Capacitance	C _{rss}			33		
Turn-On Time	t _{d(on)}	V _{DD} =10V, R _L =5.5Ω I _D =3.6A, V _{GEN} =4.5V R _G =6Ω		12	25	ns
	t _r			36	60	
Turn-Off Time	t _{d(off)}			34	60	
	t _f			10	25	



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TYPICAL CHARACTERISTICS

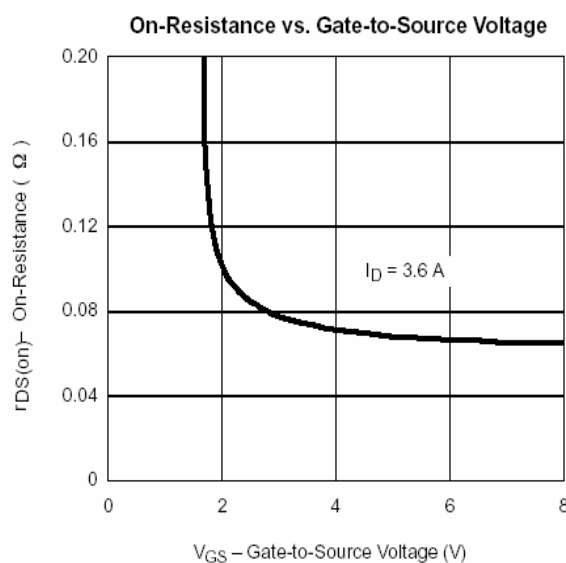
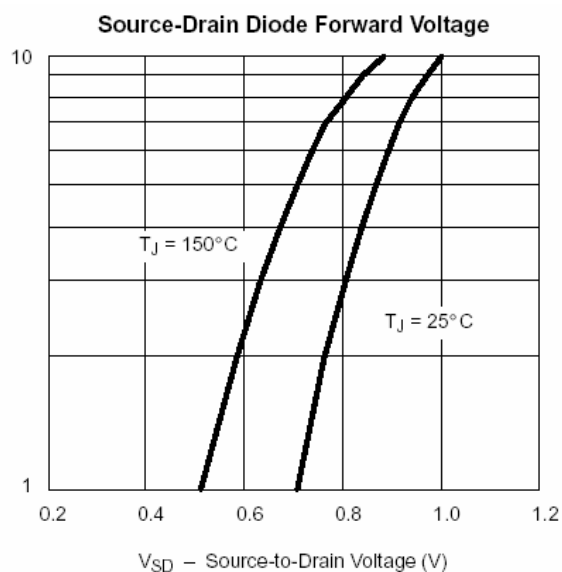
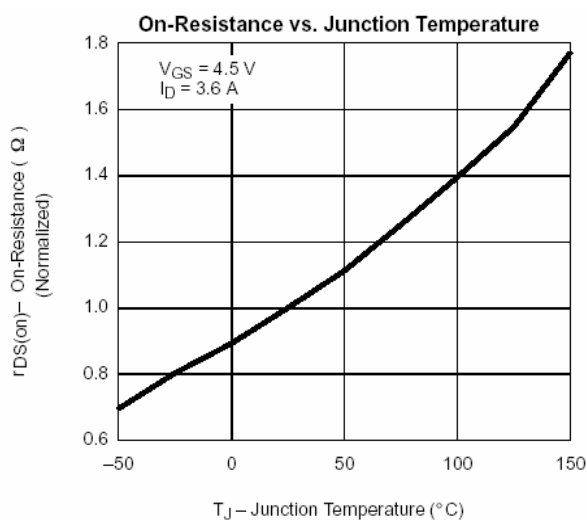
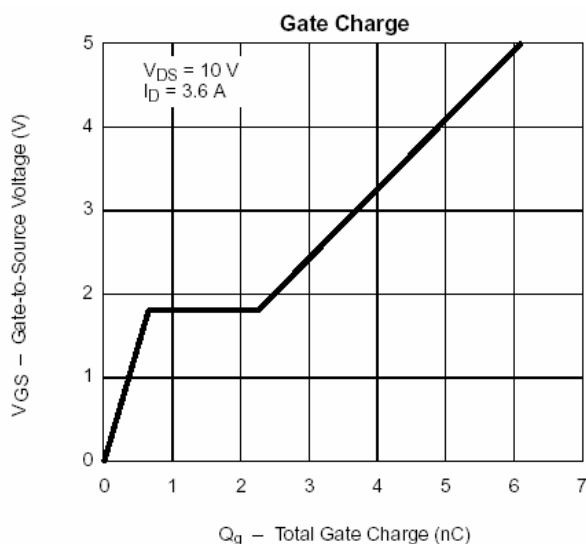




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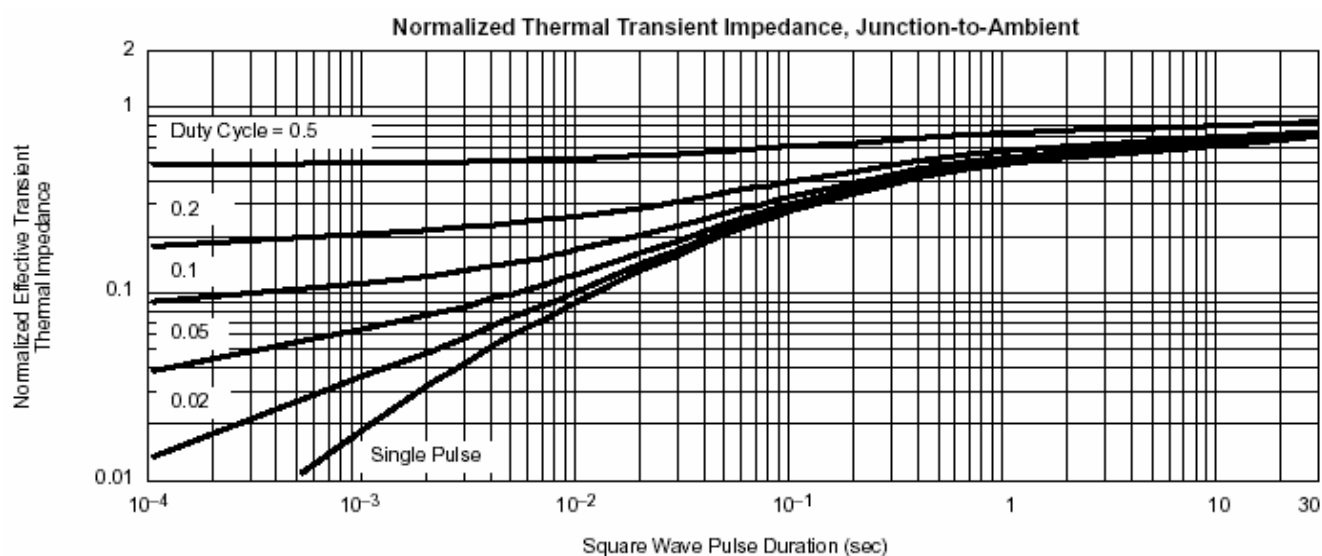
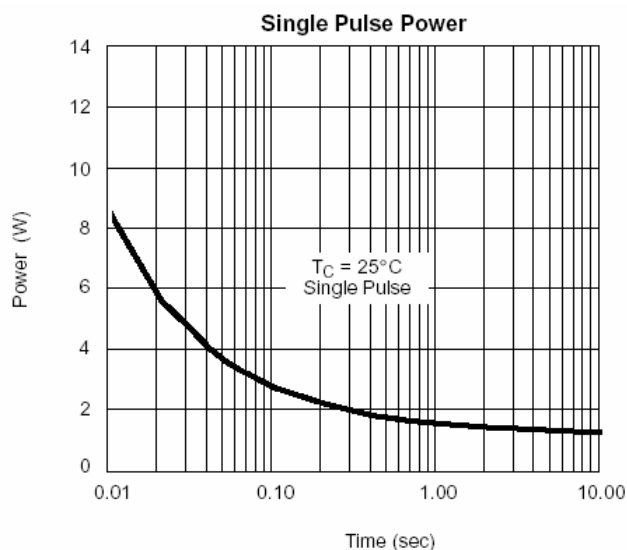
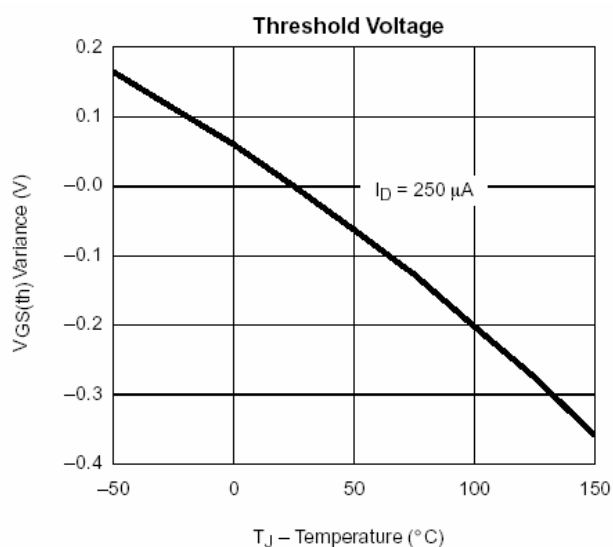




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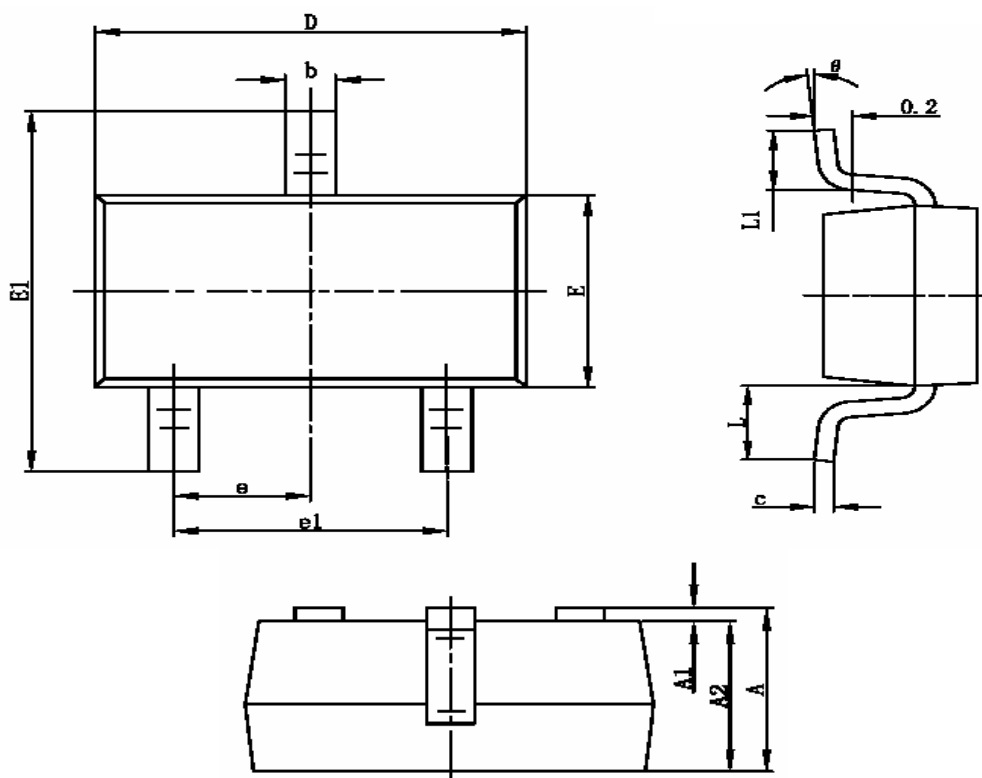




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SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



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