FEATURES

- 20 MBPS OPERATING DATA RATE
- 5.4 dB CODING GAIN @10^{-5} BER (K=7)
- MULTIPLE DEVICES CAN BE MULTIPLEXED TO GIVE UNLIMITED DATA RATES
- OPTIMIZED INTERFACE TO OPERATE WITH BPSK, QPSK, AND OQPSK DEMODULATORS
- OPERATES IN BURST AND CONTINUOUS MODES, WITH INTEGRAL TAIL-OFF
- AUTO NODE SYNC CAPABILITY
- DUAL CONTRAINT LENGTHS:
  K=6 ($G_1 = 73_8$, $G_2 = 61_8$) AND
  K=7 ($G_1 = 171_8$, $G_2 = 133_8$)
- MULTIPLE RATES:
  R = $^1/_2$, $^2/_3$*, $^3/_4$*, $^7/_8$*
  * Punctured codes
- INTERNAL PUNCTURING CAPABILITY

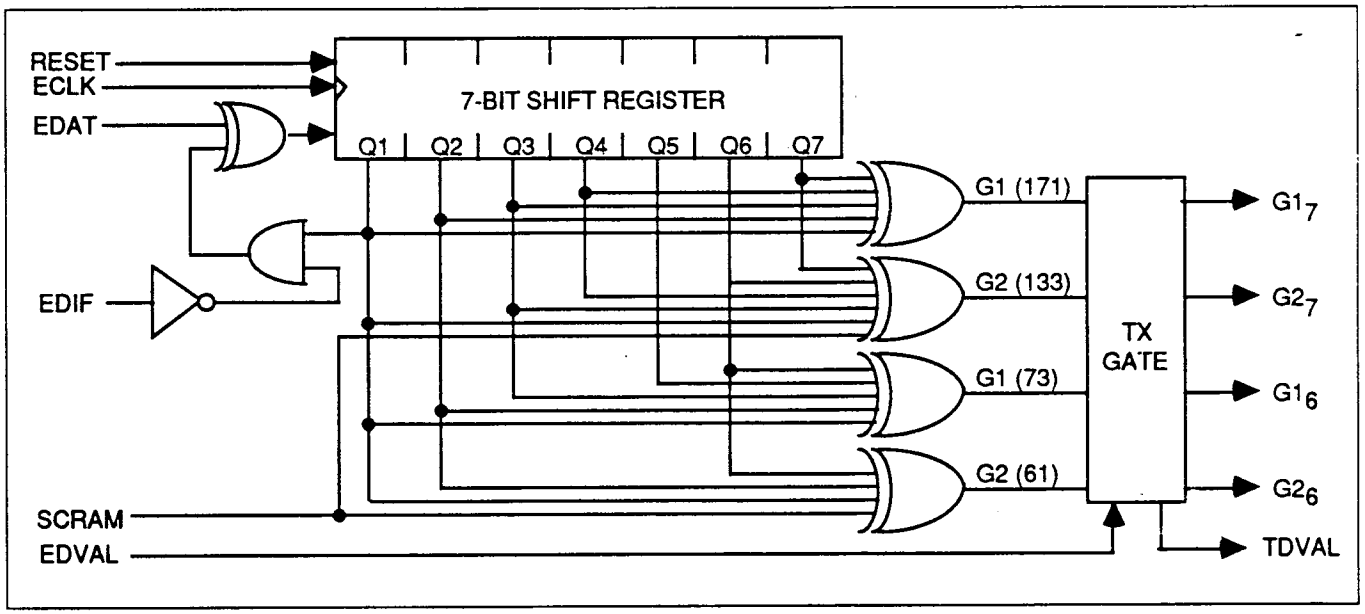
FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-2020 is a specialized product designed to perform this specific communications related function.

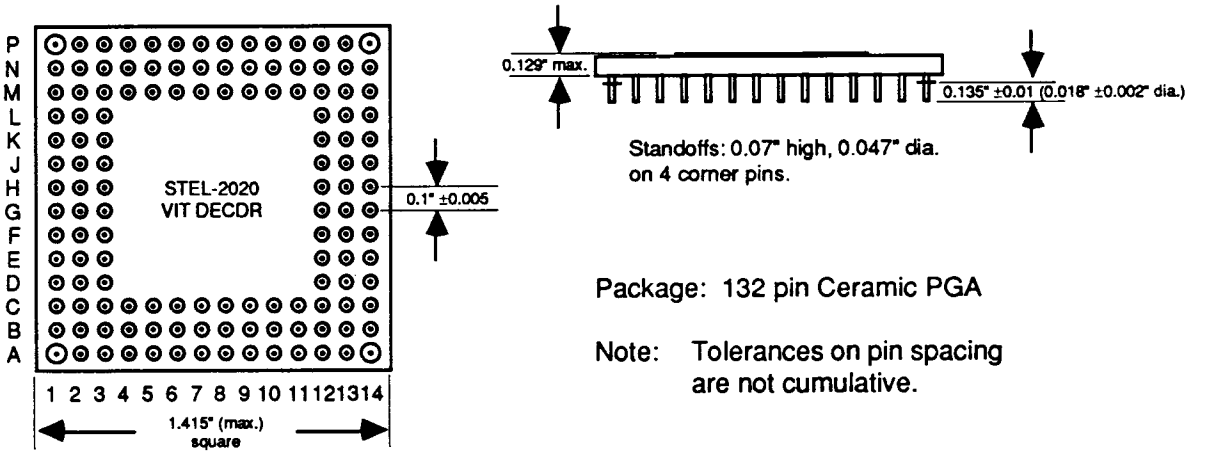
The encoder creates a stream of symbols which are transmitted at twice the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of the information despite a high symbol error rate resulting from a noisy link.

The STEL-2020 contains a convolutional encoder and Viterbi decoder (including differential, as well as direct encoding/decoding) capable of fully independent (full duplex) operation, with completely independent data clocks. At the decoder the symbol input format can be either serial, i.e., sequential symbols, (for BPSK applications) or parallel (for QPSK and OQPSK applications). The data inputs can be in offset binary or offset signed magnitude formats, with 4-bit soft decision. Auto node sync is provided for (2,1) codes, and provision for external metric assignment is also available. The unique architecture allows the device to operate with a constraint length of either 6 or 7, and punctured codes at Rates. $^2/_3$, $^3/_4$, and $^7/_8$ can be encoded and decoded as well as continuous, Rate $^1/_2$, data. The polynomials used are industry standards.

ENCODER BLOCK DIAGRAM



PIN CONFIGURATION



Package: 132 pin Ceramic PGA

Note: Tolerances on pin spacing are not cumulative.

A1	AUTO	C6	V_{SS}	H1	G_{2-0}	M10	V_{DD}
A2	THR_6	C7	V_{DD}	H2	V_{SS}	M11	I.C.
A3	THR_4	C8	NSO_6	H3	CLK	M12	V_{SS}
A4	THR_2	C9	V_{SS}	H12	V_{SS}	M13	V_{SS}
A5	THR_1	C10	SYNC	H13	V_{DD}	M14	V_{SS}
A6	NSO_7	C11	N.C.	H14	V_{DD}	N1	V_{SS}
A7	V_{DD}	C12	V_{SS}	J1	G_{2-1}	N2	XBR_7
A8	NSO_4	C13	RESET	J2	G_{2-2}	N3	XBR_5
A9	NSO_3	C14	ODVAL	J3	G_{2-3}	N4	V_{SS}
A10	NSO_1	D1	SCRAM	J12	V_{SS}	N5	XBR_0
A11	V_{SS}	D2	SEQ	J13	V_{SS}	N6	TBD
A12	V_{DD}	D3	BIN	J14	V_{SS}	N7	V_{SS}
A13	N.C.	D12	V_{SS}	K1	V_{DD}	N8	ECLK
A14	V_{DD}	D13	DATO	K2	XBR_{14}	N9	TDVAL
B1	QPSYNC	D14	DIFO	K3	XBR_{11}	N10	G_{2-7}
B2	BPSYNC	E1	RDVAL	K12	V_{SS}	N11	G_{2-6}
B3	THR_7	E2	$PNCG_2$	K13	V_{SS}	N12	I.C.
B4	THR_5	E3	$PNCG_1$	K14	V_{SS}	N13	V_{DD}
B5	THR_3	E12	V_{SS}	L1	XBR_{15}	N14	V_{SS}
B6	THR_0	E13	DIFVAL	L2	XBR_{12}	P1	XBR_8
B7	V_{DD}	E14	V_{SS}	L3	XBR_9	P2	XBR_6
B8	NSO_5	F1	G_{1-1}	L12	V_{SS}	P3	XBR_3
B9	NSO_2	F2	G_{1-0}	L13	V_{DD}	P4	XBR_2
B10	NSO_0	F3	V_{DD}	L14	V_{SS}	P5	XSEL
B11	KEQ7	F12	UCLK	M1	XBR_{13}	P6	V_{DD}
B12	I.C.	F13	GCLK	M2	XBR_{10}	P7	V_{SS}
B13	V_{SS}	F14	V_{SS}	M3	V_{DD}	P8	EDAT
B14	V_{DD}	G1	G_{1-2}	M4	XBR_4	P9	EDVAL
C1	V_{SS}	G2	G_{1-3}	M5	XBR_1	P10	V_{SS}
C2	OQSYNC	G3	V_{DD}	M6	V_{SS}	P11	G_{1-7}
C3	V_{DD}	G12	V_{DD}	M7	V_{DD}	P12	G_{1-6}
C4	OOS	G13	V_{DD}	M8	V_{DD}	P13	V_{SS}
C5	V_{DD}	G14	V_{SS}	M9	EDIF	P14	V_{SS}

ENCODER OPERATION

The convolutional coder is functionally independent from the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **ECLK**. There are four symbols generated for each data bit, two from K=6 polynomials and two from K=7 polynomials. Only two of these will normally be used at any one time, depending on which constraint length is being used. The four symbols are brought out on separate pins.

INPUT SIGNALS

RESET
Asynchronous master **Reset**. A logic low on this pin will completely reset all internal registers of the chip to an initial condition within 100 nanoseconds. This function is common to the encoder and decoder sections of the device.

ECLK
The transmit clock is the encoder system **clock**. The maximum **ECLK** frequency is 20 MHz. There is no minimum frequency.

EDAT
The encoder input **data** is connected to this input. The data is clocked in on the rising edge of the **ECLK** signal.

EDVAL
The encoder **data valid** signal is used to identify a group of transmitted bits within the same burst. This signal should be set low at the beginning of a new burst and set high at the end of the burst. The first data bit of the burst will be clocked in on the first rising edge of **ECLK** after **EDVAL** goes low. In continuous mode of operation this pin should be held low at all times.

EDIF
When the **EDIF** signal is set high it **enables** the **differential** encoder circuit. When it is set low this circuit will be disabled, and normal, non-differential data will be loaded into the convolutional encoder.

SCRAM
When this input is set high it causes the encoded data to be **scrambled** by inverting the G2 symbols after encoding. This guarantees that there will be a minimum of 1 transition in every 14 symbols in the transmitted symbol stream for Rate 1/2 encoding when the input data to the encoder contains no transitions. The G2 symbols will also be inverted before decoding when **SCRAM** is set high. When the **SCRAM** signal is set low this function will be inhibited.

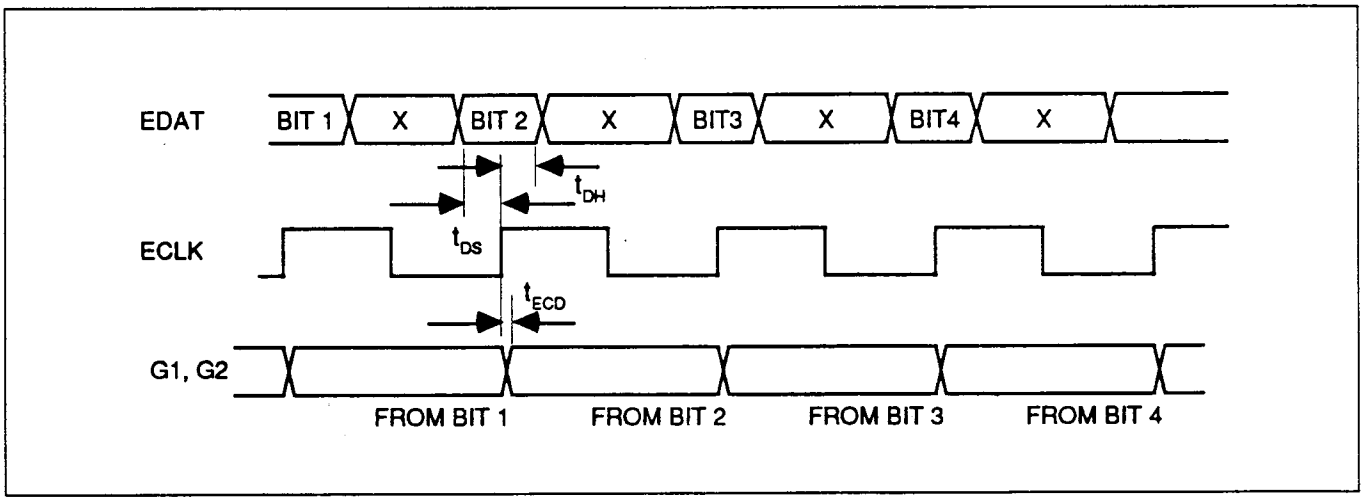
OUTPUT SIGNALS

$G1_6$, $G2_6$
The $G1_6$ and $G2_6$ signals are the two encoded symbols generated with the K=6 polynomials, $G1=73_8$ and $G2=61_8$.

$G1_7$, $G2_7$
The $G1_7$ and $G2_7$ signals are the two encoded symbols generated with the K=7 polynomials, $G1=171_8$ and $G2=133_8$.

TDVAL
This signal signifies when transmitted **data** (the output symbols) is **valid**. When it is low the symbols are valid, and when it is high they are invalid. Invalid data is generated at the end of a burst, when the signals remaining in the shift register are being flushed out.

ENCODER TIMING



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C
T_a	Operating Temperature	–40 to +85	°C (Plastic package)
		–55 to +125	°C (Ceramic package)
V_{CCmax}	Max. voltage between V_{CC} and V_{DD}	+7 to –0.7	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD}+0.7	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS}–0.7	volts

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 10%	volts
T_a	Operating Temperature (Ambient)	0 to +70	°C (Plastic package)
		–55 to +125	°C (Ceramic package)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 ±5% volts, T_a=0° to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			8.0	mA/MHz	@ 20 MHz
$V_{IH(min)}$	Min. High Level Input Voltage	2.0			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$V_{OH(min)}$	Min. High Level Output Voltage	2.4			volts	I_O = –4.0 mA
$V_{OL(max)}$	Max. Low Level Output Voltage			0.4	volts	I_O = +4.0 mA
$I_{IH(max)}$	Max. High Level Input Current			10	µA	V_{IN} = +5.0 volts
$I_{IL(max)}$	Max. Low Level Input Current			–10	µA	V_{IN} = 0 volts

ENCODER A.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 volts, V_{SS}=0 volts, T_a=25°C)

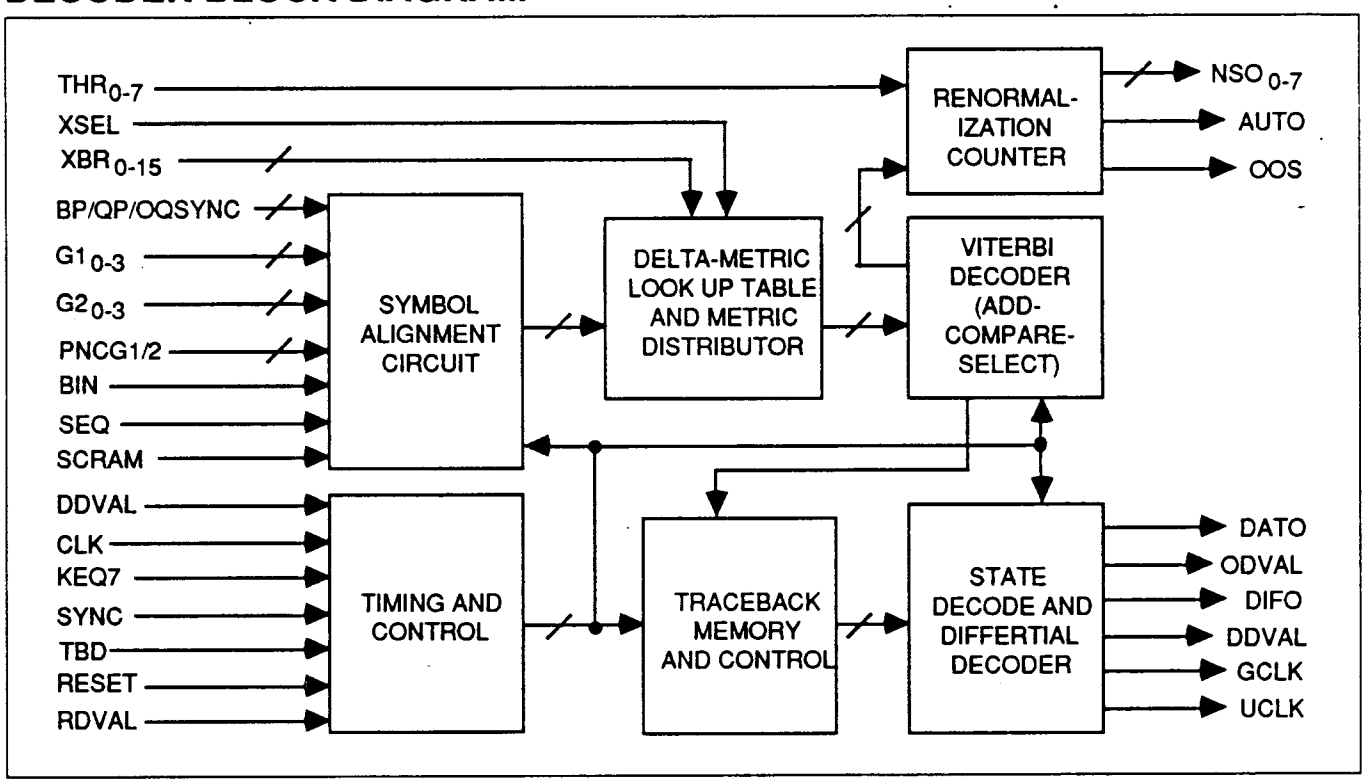
Symbol	Parameter	Min.	Max.	Units
t_{DS}	EDAT to ECLK setup	10		nsec.
t_{DH}	EDAT to ECLK hold	5		nsec.
t_{ECD}	ECLK to $G1_6$, $G1_7$, $G2_6$, or $G2_7$ stable delay		5	nsec.
f_{ECLK}	ECLK frequency		20	MHz

DECODER OPERATION

The decoder section of the STEL-2020 implements the Viterbi algorithm for decoding convolutionally encoded data. It incorporates many unique features which enhance its capabilities and flexibility. The incoming symbols can be accepted either sequentially, as would be the case in a BPSK system, or in parallel, as would be the case in a QPSK system. In addition, a special circuit takes care of symbol alignment in an offset QPSK (OQPSK) system. The signals can be in either offset binary or two's complement codes. In both cases the codes are offset from zero by half a bit, giving the same number of allowable states in both the positive and negative directions. When the encoder uses the scramble function to invert the G2 symbols these will automatically be re-inverted before being decoded.

The Viterbi decoder itself uses the add/compare/select algorithm to determine the most likely value for each bit from the received symbols. Five-bit arithmetic is used to maximize the performance with the four-bit soft-decision data inputs. The decoder contains many user controlled features which enhance its performance in different environments. The depth of the trace-back used can be set to the long mode (70 to 140 states) for optimum performance in the punctured modes ($R=^{2}/_{3}$, $^{3}/_{4}$, $^{7}/_{8}$), or to the short mode (38-76 states) in normal mode ($R=^{1}/_{2}$). (The penalty for using the longer trace-back length is the additional delay in decoding the data.) A data valid input also enhances burst mode operation by automatically setting the device into the end-of-burst mode at the correct point in time. A built-in counter estimates the probability of incorrect node synchronization from the error rate. A user selectable feedback loop allows the node synchronization to be corrected automatically.

DECODER BLOCK DIAGRAM



INPUT SIGNALS

RESET
Asynchronous master **Reset**. A logic low on this pin will completely reset all internal registers of the chip to an initial condition within 100 nanoseconds. This function is common to the encoder and decoder sections of the device.

KEQ7
The **KEQ7** signal selects the constraint length of the decoder. When it is high, K=7, and when it is low, K=6.

CLK
System **clock** to the decoder. It is the reference clock for all internal synchronous functions. It should nominally be a square wave at the same frequency as the data, with a maximum frequency of 20 MHz.

RDVAL
The **R**eceive **d**ata **val**id signal is used to identify a group of symbols associated with the same burst. This signal should be set low at the beginning of a new burst and set high at the end of the burst. The first data bit of the burst will be clocked in on the first rising edge of **CLK** after **RDVAL** goes low. When **RDVAL** is high it should remain high for at least 1 cycle of **CLK**. In continuous mode of operation, **RDVAL** should be set low at all times.

$G1_{0\text{-}3}$, $G2_{0\text{-}3}$
The $G1_{0\text{-}3}$ and $G2_{0\text{-}3}$ signals are the 4-bit soft decision input symbols to the decoder. They are presented to the decoder either sequentially or in parallel depending on the state of the **SEQ** signal. In the parallel mode (**SEQ** = 0) the symbols are clocked into the device on the rising edge of the **CLK**. In the sequential mode (**SEQ** =1) the $G2_{0\text{-}3}$ inputs are not used, both the G1 and G2 symbols are loaded via the $G1_{0\text{-}3}$ pins. The G2 symbols are then latched in on the rising edge of **CLK** and the G1 symbols are latched in on the falling edge.

SEQ
When this signal is high, the input symbols are accepted **seq**uentially by the chip, using the $G1_{0\text{-}3}$ pins for both symbols. When it is set low the inputs are accepted in parallel, using the $G1_{0\text{-}3}$ pins for the G1 symbols and the $G2_{0\text{-}3}$ pins for the G2 symbols. The sequential input is most suited for BPSK data and the parallel input is most suited for QPSK data.

BIN
The STEL-2020 can accept the soft-decision input data in either offset binary or offset 2's complement formats. When the **BIN** signal is set high the format expected will be offset **bin**ary, and when it is set low it will be offset two's complement. The meanings of the 4-bit values for these two codes is shown in the table.

Offset 2's Comp.	Offset Binary	Value
0111	1111	Most confident +
0110	1110	
0101	1101	
0100	1100	
0011	1011	
0010	1010	
0001	1001	
0000	1000	Least confident +
1111	0111	Least confident –
1110	0110	
1101	0101	
1100	0100	
1011	0011	
1010	0010	
1001	0001	
1000	0000	Most confident –

SCRAM
When this input is set high it causes the encoded data to be **scram**bled by inverting the G2 symbols after encoding. This guarantees that there will be a minimum of 1 transition in every 14 symbols when the input data to the encoder contains no transitions. The G2 symbols will also be inverted before decoding. When the **SCRAM** signal is set low, this function will be inhibited. This function is common to the encoder and decoder sections of the device.

PNCG1, PNCG2
The **PNCG1** and **PNCG2** signals are used to control the STEL-2020 when operating in punctured mode. In normal (Rate=½) operation these pins should be set low. In punctured mode the **PNCG1** signal must be set high to indicate that the G1 symbol is punctured and the **PNCG2** signal must be set high to indicate that the G2 symbol is punctured. A symbol will be punctured when the **PNCG1** or **PNCG2** signals are high during the rising edge of **CLK** and alternating least-confident ones and zeroes will be substituted for the actual data present on the $G1_{0\text{-}3}$ or $G2_{0\text{-}3}$ pins at that time.

TBD
This signal selects the Trace-Back Depth used in the decoding process. When it is set low the traceback

depth will be 70 to 140 states, and when it is set high the traceback depth will be 38 to 76 states. The longer traceback depth gives better performance, especially in the punctured modes; the shorter traceback depth gives a shorter latency.

SYNC
When the **SYNC** input is set high, the node **sync** circuit will be enabled, and when it is set low, the node sync circuit will be disabled. When it is enabled the node sync circuit will examine the renormalization count. If this count is greater than the threshold (defined by the user via the 8 input pins **THR**) for every 256 bit period, then out-of-sync condition is declared (**OOS** output signal is set high). The renormalization count for every 256 bit period is available at the 8 output pins $\mathbf{NSO_{0\text{-}7}}$. This signal can be used externally to correct the node sync. Automatic internal node sync is achieved by connecting the **AUTO** output to **BPSYNC**, **QPSYNC**, or **OQSYNC**, depending on the mode of operation.

BPSYNC, QPSYNC, and OQSYNC
The **BPSYNC**, **QPSYNC**, and **OQSYNC** signals are used to correct the node sync in the Viterbi decoder. The **BPSYNC** input should be used when the device is being used with BPSK data, the **QPSYNC** input should be used with QPSK data, and the **OQSYNC** input should be used with Offset QPSK (OQPSK) data. When these inputs are set low, no change will be made to the symbols, and when they are set high, the G1 and G2 symbols will be interchanged internally in the manner appropriate to the mode of operation. The appropriate input should be connected to the **AUTO** output to use the internal node sync circuit.

$\mathbf{THR_{0\text{-}7}}$
This 8-bit input signal defines the threshold for node synchronization. If the renormalization count is greater than this threshold value then out-of-sync condition is declared (i.e., the output pin **OOS** is switched to High).

$\mathbf{XBR_{0\text{-}15}}$
If the user wishes to use adaptive metrics, or metrics other than the ones stored internally, different branch metrics can be loaded via these 16 pins. **XSEL** must be set high to enable this function.

XSEL
When this input is set high, external branch metrics will be used. It is set low for normal operation.

OUTPUT SIGNALS

GCLK
Gated output data **clock**. The rising edge of **GCLK** can be used as a strobe for **DATO** output, which is guaranteed to be valid on this edge. When **ODVAL** is High, **GCLK** is disabled and stays Low.

UCLK
Ungated output **clock**. Same as **GCLK** except that this output clock is not gated by **ODVAL**.

DATO
Decoded **data** output. This is the output of the Viterbi decoder. The output data bits are delayed by 161 clock cycles relative to the corresponding input symbols, $\mathbf{G1_{0\text{-}3}}$ and $\mathbf{G2_{0\text{-}3}}$, when operating in the short trace-back depth mode (**TBD=1**), and 289 clock cycles when operating in the long trace-back depth mode (TBD=0).

ODVAL
Output **Data Valid**. This is a replica of **RDVAL** input, delayed by the same number of clock cycles as the decoded data bits. When **ODVAL** is low the output data **DATO** is valid. When it is high **DATO** is invalid.

DIFO
Differential decoded data output. This is the output of the Viterbi decoder after passing through the differential decoder. The **DIFO** output is delayed by one clock cycle relative to the **DATO** signal.

DIFVAL
Differential output data valid. When **DIFVAL** is low **DIFO** is valid. When it is high **DIFO** is invalid.

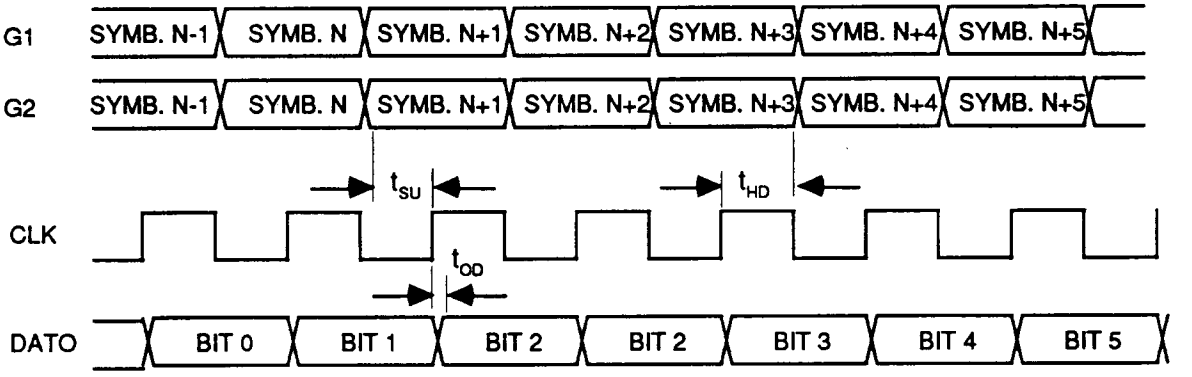
$\mathbf{NSO_{0\text{-}7}}$
These are the 8 output bits of renormalization count for every 256-bit period.

OOS
This output pin serves as a flag for the **out-of-sync** condition. When it goes high it signifies that the renormalization count in the internal node sync circuit has exceeded the threshold value set by the $\mathbf{THR_{0\text{-}7}}$ signal.

AUTO
The **AUTO** output is the feedback signal from the internal node sync correction circuit. It will toggle each time the **OOS** output goes high. It should be connected to **BPSYNC**, **QPSYNC**, or **OQSYNC**, depending on the mode of operation, when the internal node sync facility is used.

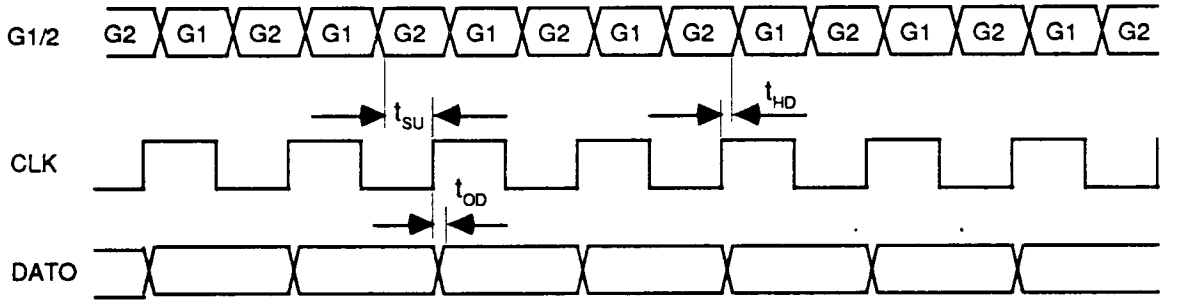
DECODER TIMING

(a) PARALLEL INPUT MODE (SEQ=0)



Note: N=157 when **TBD** =1, N=289 when **TBD** =0

(b) SEQUENTIAL INPUT MODE (SEQ=1)



DECODER A.C. CHARACTERISTICS

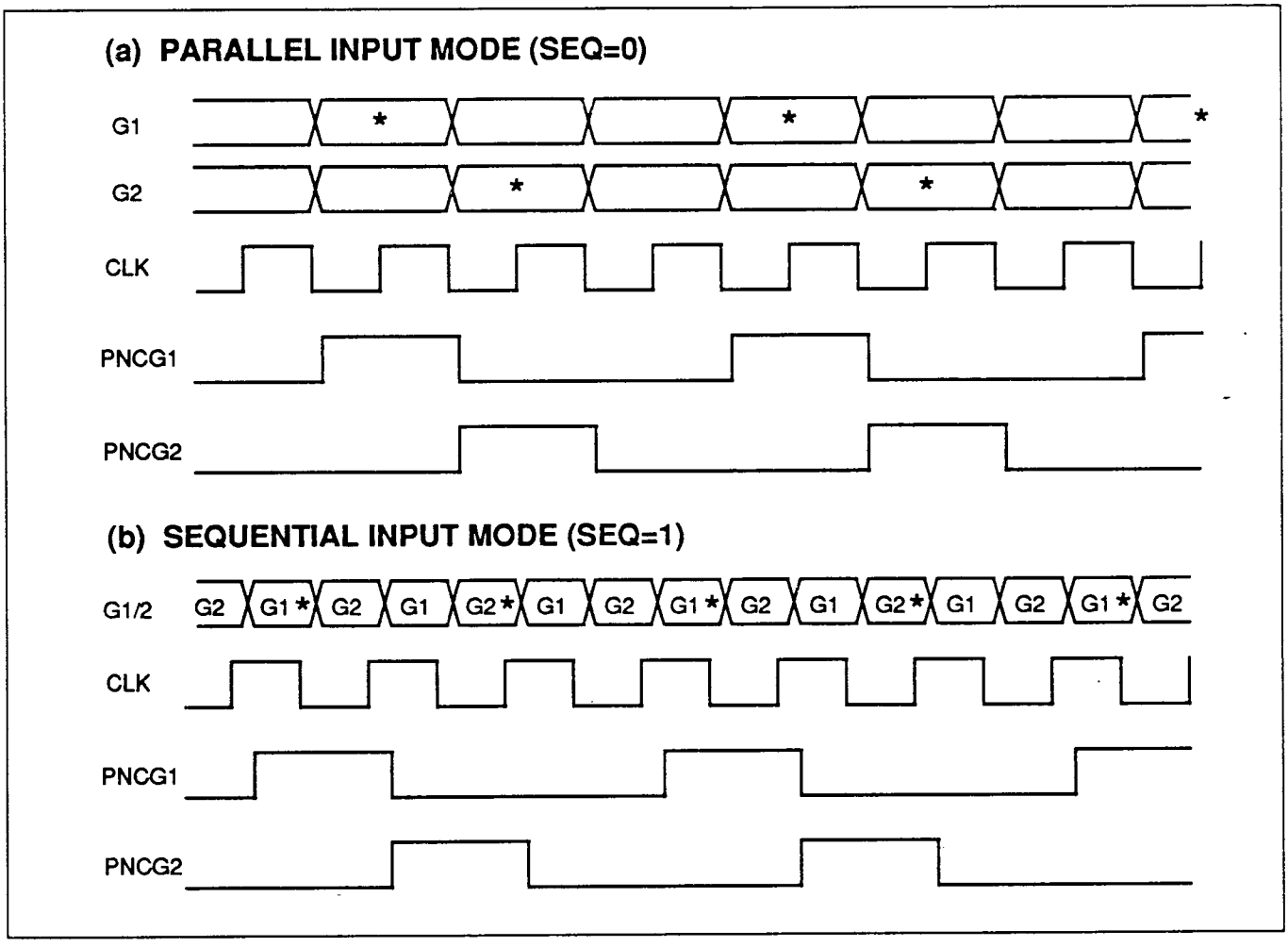
(Operating Conditions: V_{DD}=5.0 ± 5% volts, V_{SS}=0 volts, T_a=0° to 70°C)

Symbol	Parameter	Min.	Max.	Units	Conditions
f_{CLK}	CLK Frequency		20	MHz	
f_{CLK}	CLK Frequency		16	MHz	@ 125° C (ceramic only)
t_{SU}	G1 or G2 to CLK setup	10		nsecs.	
t_{HD}	G1 or G2 to CLK hold	5		nsecs.	
t_{OD}	CLK to DATO stable delay		5	nsecs.	

PUNCTURED MODE OPERATION

In punctured codes some of the symbols generated by the convolutional encoder are deleted, or punctured, from the transmitted sequence. For example, in an unpunctured Rate 1/2 sequence, four bits would be transmitted for every two data bits. If every fourth bit was punctured from the sequence then only three bits would be transmitted for every two data bits. This would result in a Rate 2/3 code. The STEL-2020 is designed to operate in punctured mode as well as normal, Rate 1/2, mode. This is easily accomplished by means of the **PNCG1** and **PNCG2** signals, which delete the symbol which would normally have been loaded into the device at the time when either of these signals is set high. The punctured symbols are replaced by alternating least confident ones and zeroes, to avoid the introduction of a bias. The Viterbi algorithm treats the least confident symbols as if they were badly corrupted signals, and zero weight is given to them in the computations relative to the other symbols. The coding gain is significantly less than that for unpunctured operation, but this is the trade-off for the reduced bandwidth required to transmit the symbols. The puncturing sequences for the various $^{(N-1)}/_{N}$ rates of punctured operation are shown in the table. The sequence shown in boldface is the basic sequence, which is then repeated. The use of the **PNCG1** and **PNCG2** signals is shown below for Rate 3/4. The sequence is G1 G2 P G2 G1 P. The punctured symbols are marked with asterisks.

Rate	Symbol sequence
2/3	**G1 G2 G1 P** G1 G2 G1 P G1 G2 G1 P G1 G1 G2 G1 P G1
3/4	**G1 G2 P G2 G1 P** G1 G2 P G2 G1 P G1 G1 G2 P G2 G1
7/8	**G1 G2 P G2 P G2 P G2 G1 P P G2 G1 P** G1 G2 P G2

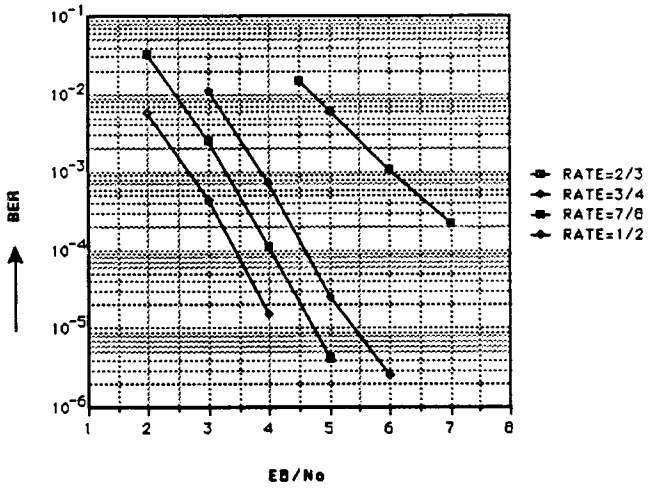


NODE SYNCHRONIZATION

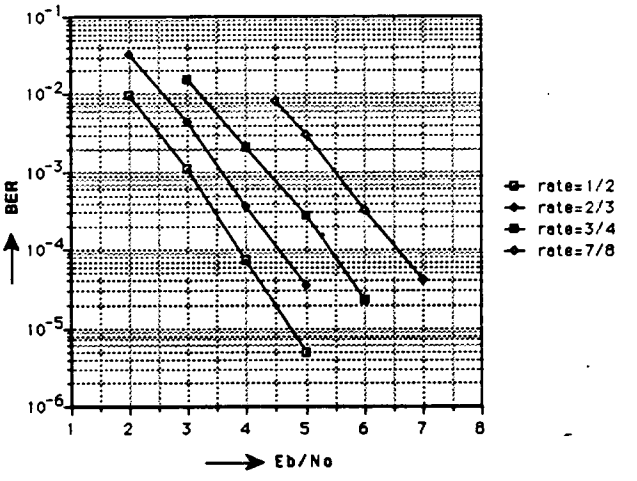
In a communication system using Viterbi decoding the decoder will only operate correctly when the symbols G1 and G2 are loaded into the decoder in the correct order. Identifying which symbol is which is referred to as node synchronization. The STEL-2020 contains a circuit designed to carry out the node synchronization function automatically. It uses the internally generated metrics of the received sequence to do this. These parameters are constantly changing and are periodically renormalized to keep them within bounds. If renormalization is required too frequently it is a good indication that the system is not converging, and the most likely reason is lack of node synchronization. The internal node sync circuit will be enabled if the **SYNC** input is set high. The renormalization rate at which the system will decide to change the node sync is determined by the threshold parameter. This is an 8-bit number which is set by the the $\mathbf{THR}_{0\text{-}7}$ inputs. When the renormalization count exceeds this value, the **OOS** output will go high and the **AUTO** output will toggle. The counter is reset every 256 clock cycles, so that the threshold must be exceeded somewhere in the 256 cycle period for resynchronization to take place. To use the internal node sync the **AUTO** output must be connected to **BPSYNC** when the data is being entered sequentially, as in a BPSK system. When the data is being entered in parallel from a QPSK system the **AUTO** output must be connected to **QPSYNC**, unless the system is supplying OQPSK data, in which case the **OQSYNC** pin should be used instead of **QPSYNC**. When this is done the symbol alignment circuit will correct the node synchronization problem. This is different for each of the three modes.

PERFORMANCE

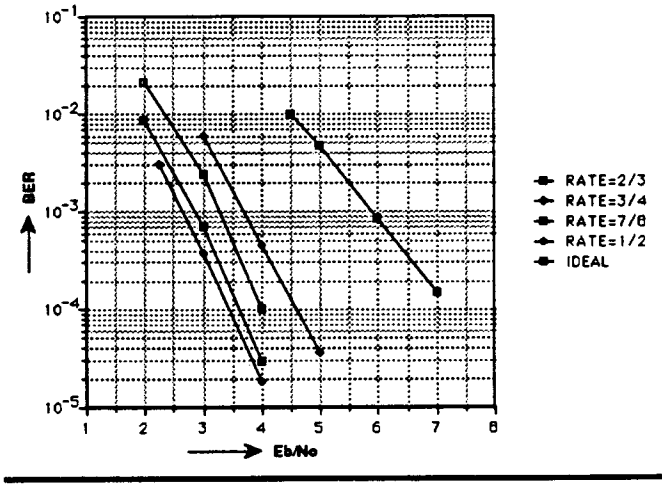
1. K=7, long burst performance.



2. K=6, long burst performance.



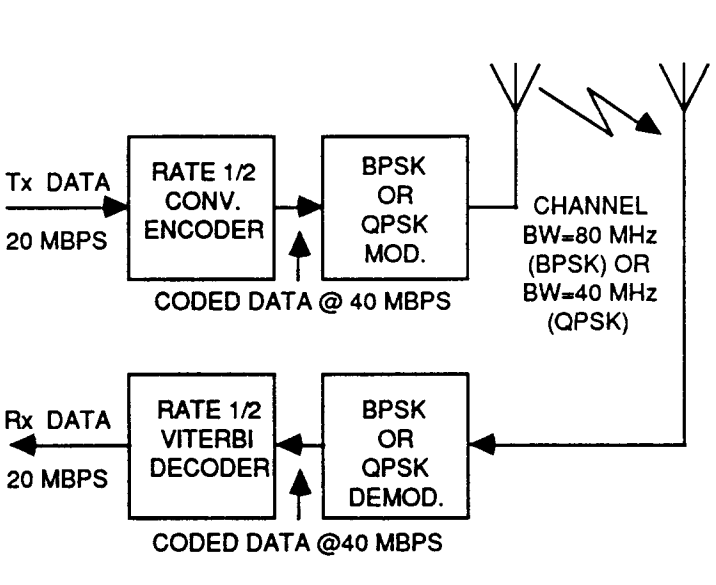
3. K=7, short burst (56 bits) performance.

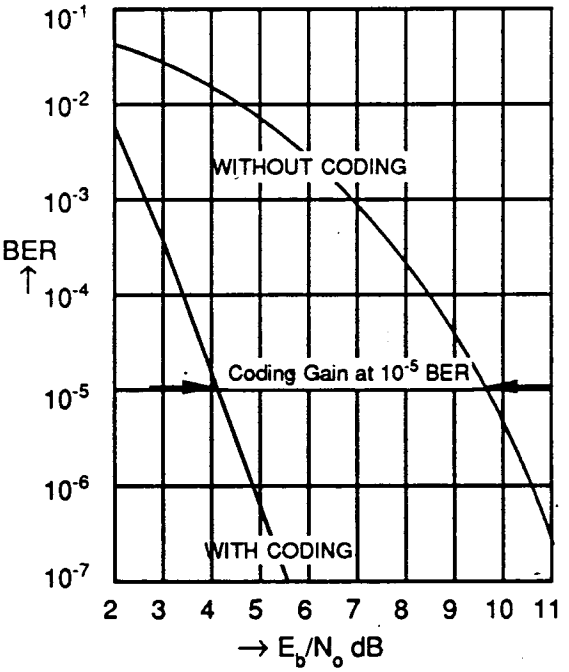


APPLICATION INFORMATION

The STEL-2020 can be used in a variety of different environments. One example is shown below. An example of a system using the convolutional coder and Viterbi decoder is illustrated here. The system modulates a data stream of rate 20 Mbps using binary PSK (BPSK) or quaternary PSK (QPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate $^1/_2$ encoding) or make use of two parallel channels (QPSK) to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder. A single data bit is clocked into the 7 bit shift register on the rising edge of **ECLK**. The decoder portion of the STEL-2020 is designed to accept symbols synchronously. **CLK** is supplied by the user to clock in the symbols. The maximum data rate is 20 Mbps, using a clock frequency of 20 MHz. This corresponds to 40 MSymbols per second at Rate $^1/_2$ with BPSK.





BPSK COMMUNICATION SYSTEM USING CONVOLUTIONAL ENCODING AND VITERBI DECODING. RATE = $^1/_2$

FOR FURTHER INFORMATION
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