GEC PLESSEY
SEMICONDUCTORS

DS2312-3·1

ULA DF SERIES

HIGH PERFORMANCE MIXED DIGITAL/ANALOG ARRAY FAMILY

(Supersedes June 1990 edition)

The DF series of arrays is designed to provide cost effective single chip solutions to high speed combined digital and analog mixed signal systems

GENERAL DESCRIPTION

For many years, GEC Plessey Semiconductors ASIC products have been successfully fulfilling the requirements for single chip systems in silicon for lower frequency applications. The DF series extends the benefits of mixed signal capability to systems operating at frequencies up to 100MHz. Integrating the complete system onto the chip saves space and assembly costs and greatly simplifies board design.

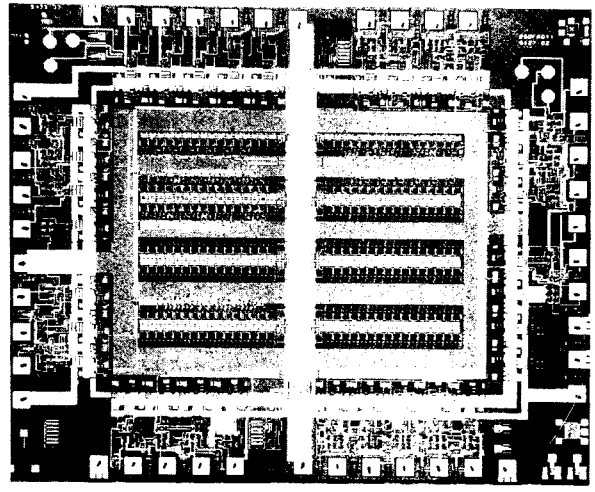


Fig. 1 A DF series array

FEATURES

- Combines High Performance Digital and Analog
- System Speeds to 100MHz
- Full Design Support, Including:
  - Digital and analog macros
  - Complete CAD suite
  - Silicon compilers
  - SPICE libraries
  - Comprehensive design element libraries
- Analog Features:
  - 100MHz analog capability
  - 24 transistors and 19 resistors per analog cell
  - Closely matched components
  - Low offsets
  - Optimised for high speed
  - Range of high performance characterised analog macros
  - Complex macros can use multiple cells
- Digital Features:
  - Gate delays to 1ns
  - Differential logic giving unprecedented speed/power performance
  - Choice of 5 different gate types
  - Selective speeding-up option
  - Excellent gate delay with high loads
- I/O Features
  - Interfaces to ECL, TTL and CMOS
- Special Features:
  - Bandgap regulator
  - High current drive transistors
- 1·5 Micron Features Using Advanced Bipolar Process
- Wide Range of Package Styles
- Full Military Temperature Range

The DF series array features enhanced high performance mixed Analog and Digital capabilities. The analog cell components are optimised for good matching, low offset and high speed.

There is a high performance logic function core on each array which is supported by a family of Design Elements offering effective gate delays to below 1ns. These delays are virtually independent of fan-out, supply voltage and clock frequency.

The supporting libraries of both Analog and Digital Design Elements and Macro functions can be combined to obtain optimum results for a specific system. Interconnection of the physical design is carried out by using the 100% autoroutable EDA (Electronic Design Automation) software.

The technology employs a 1·5 micron Advanced Bipolar process (LE2 process), which is fully supported by the silicon compiler-based CAD to provide the high performance components required by today's leading edge products.

PRODUCT RANGE

The DF array series product range is shown in Table 1, below. Actual cell utilisation can be up to 100% of the uncommitted gate count, depending on the circuit structure.

Detail	ULA Type					
	5DF	11DF	14DF	18DF	24DF[1]	30DF[1]
Core cells per arm	16	20	22	23	33	16
Arms per column	14	22	26	30	30	38
Columns	1	1	1	1	1	2
Matrix cells	224	440	572	690	960	1216
Matrix gates[2] (logic)	448	880	1144	1380	1920	2432
Analog cells	32	44	54	58	74	82
Bond pads	43	55	65	69	85	93

Table 1 Details of range of DFseries arrays

NOTES
1. Preliminary information. Please consult your local Semi-Custom Design Centre for availability.
2. A core matrix gate is defined as as a 2-input, 2-output gate. The dual output configuration of an RNOR gate allows for wire-OR, which can significantly increase the effective gate count.

CHIP ARCHITECTURE

The chip architecture of the DFseries shown in Fig. 2 comprises an inner core of matrix cells for the digital circuitry. The outer ring of analog cells is used for realising the analog functions and for interfacing.

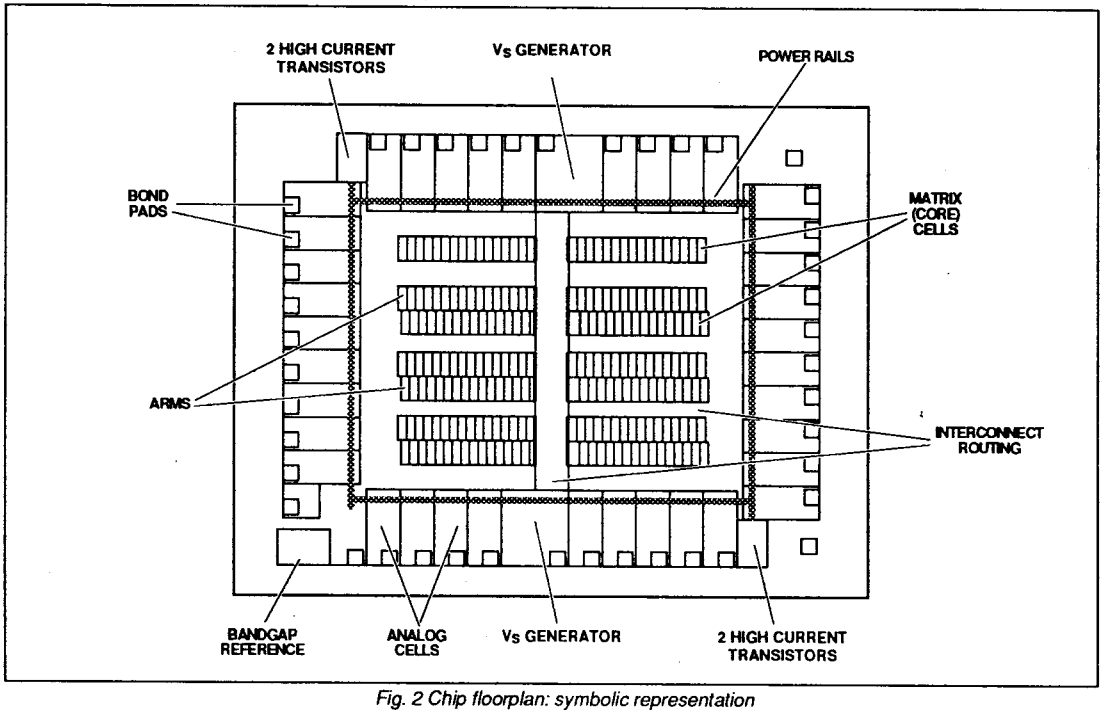


Fig. 2 Chip floorplan: symbolic representation

ANALOG CELLS

A most important aspect of the DF series of mixed signal arrays is the range of circuit functions possible with the analog cells.

The high quality of the optimally matched components used in the cells, together with the comprehensive range of values, gives the DF series the ability to implement high performance analog functions.

Each analog cell contains up to 24 transistors and 19 resistors, which can be interconnected to produce a wide variety of functions. Adjacent resistors in a cell are matched to within ±1% and similar transistors have matching V_{BE} values to within 300μV. These factors, together with the 1·1GHz f_T of the transistors, facilitate the high analog performance.

The analog cells also provide for the I/O buffering to interface to external circuitry and are therefore required to be robust and flexible. The inputs and outputs provide the designer with multiple interface options, can withstand electrostatic discharges and are not susceptible to latch-up (the process is inherently radiation-hard).

The cells can be configured to interface with all commonly used technologies such as TTL, CMOS and ECL. The ready availability of TTL compatible outputs, with the associated source and sink currents and low $R_{CE\ (SAT)}$, means that high capacitive loads can be switched at speed without the need for additional buffering. Many of these functions are available as fully characterised macros.

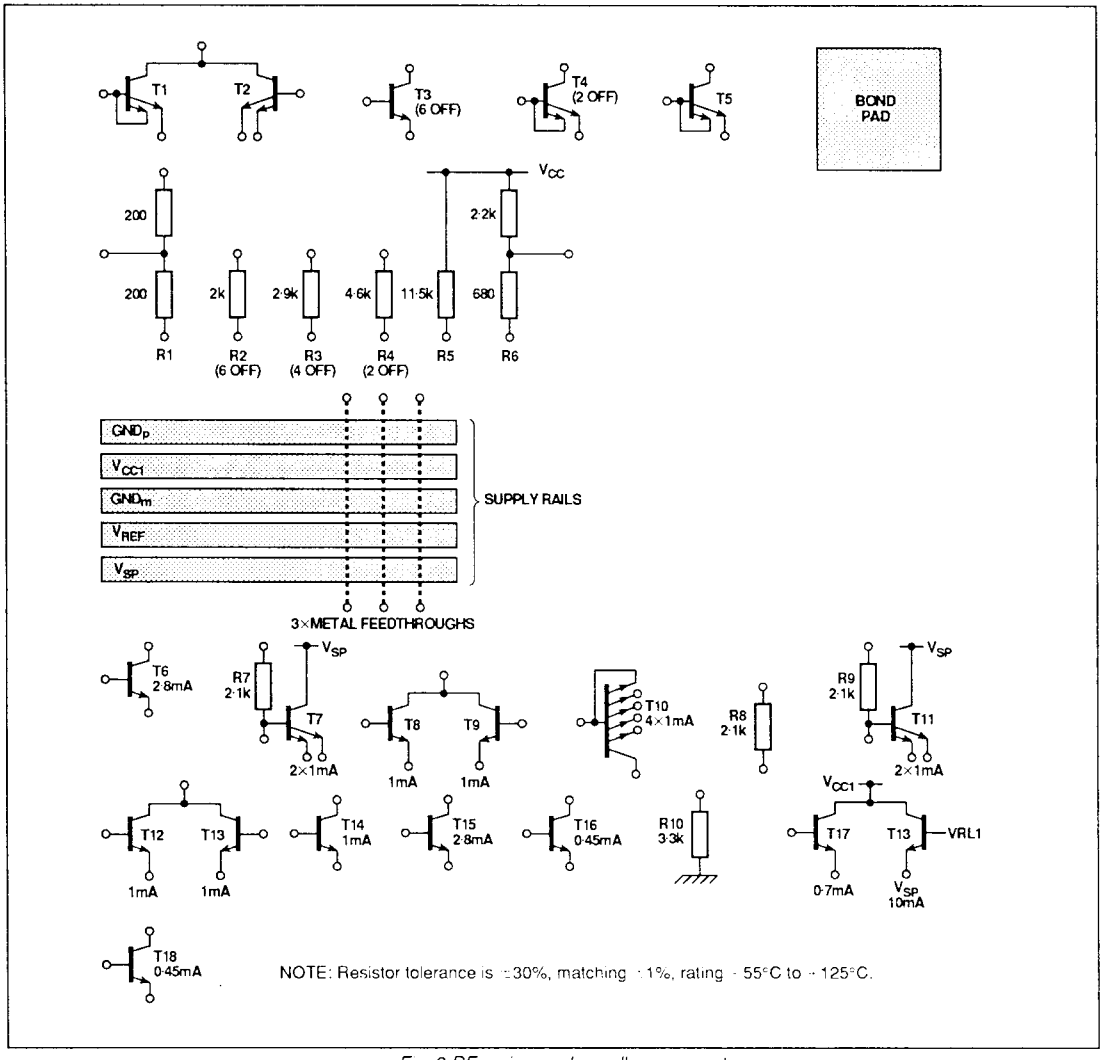


Fig. 3 DF series analog cell components

TYPICAL ANALOG PERFORMANCE CHARACTERISTICS

All parameters are for nominal V_{CC} = 5V at T_{AMB} = 25°C

Parameter	Component	Value	Units	Conditions
I_{CE}	T1	3·8	mA	
I_{CE}	T2	16·8	mA	
I_{CE}	T3	3·8	mA	
I_{CE}	T4	3·8	mA	
I_{CE}	T5	8·4	mA	
H_{FE} forward	T3	265		I_C = 100μA
H_{FE} inverse	T3	10		
V_{BE}	T3	0·775	V	I_C = 1mA
V_{BE} matching	T3	±300	μV	Between adjacent devices within one analog cell
f_T	T3	1100	MHz	I_C = 2·5mA
Resistor accuracy	All R	±30	%	
Resistor matching	R2	±1	%	Adjacent resistors within one analog cell
Resistor voltage coefficient	R2	1	%/V	

Table 2 Analog component characteristics

CORE CELLS FOR SYSTEM LOGIC

The core logic cell components can be configured into a range of logic gates and functions with differing complexities, functionality and speed/power attributes.

The core consists of rows of identical matrix cells, the rows being separated by routing channels for component or function interconnection. Power is distributed to each matrix cell by dedicated power rails between the rows of cells.

Each cell is equivalent to two 2-input gates, comprising 8 transistors and 2 resistors. Gates with effective delays to below 1ns and 1·5ns clock-to-output delay flip-flops are features of the DF matrix capability. These delays are virtually independent of fan-out, supply voltage and clock frequency.

Each matrix cell can be connected to form two basic gate structures, NOR and RNOR and two special variants, PNOR and WNOR.

The basic low power NOR gate uses current mode logic (CML) and is used whenever propagation delay is not critical. Taking the NOR gate and adding an output buffer creates an RNOR gate using an identical number of matrix cells but giving significantly faster switching times. Moreover, the delay is virtually unaffected by output loading.

The PNOR gate has been designed to drive the very high fan-outs typically found on clock lines. Table 3 shows that even when driving 50 gates the delay is below 4·5ns.

Large wire-OR nets can be realised using WNOR gates to significantly reduce complexity and overall propagation delays.

Matrix Performance

Table 3 refers to 2-input gates.

Gate type	t_{pd} (ns)	I_G (μA) (average)	Comments
NOR	2·6	55	Fanout = 2
NOR	1·6	110	Speeded-up*
RNOR	1·4	155	Buffered NOR gate, fanout = 2
RNOR	1·0	310	Speeded-up*
PNOR	4·3	330	Fan out = 50
WNOR	6·2	110	Fan out = 20

*Table 3 Gate performance. *Speed-up is achieved by the selective use of additional matrix cell components*

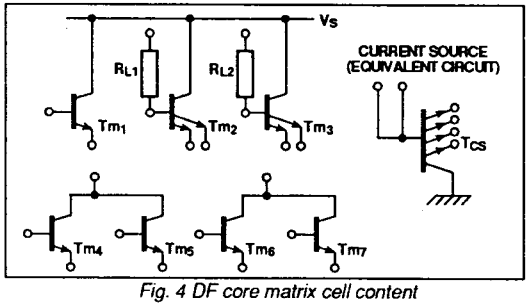


Fig. 4 DF core matrix cell content

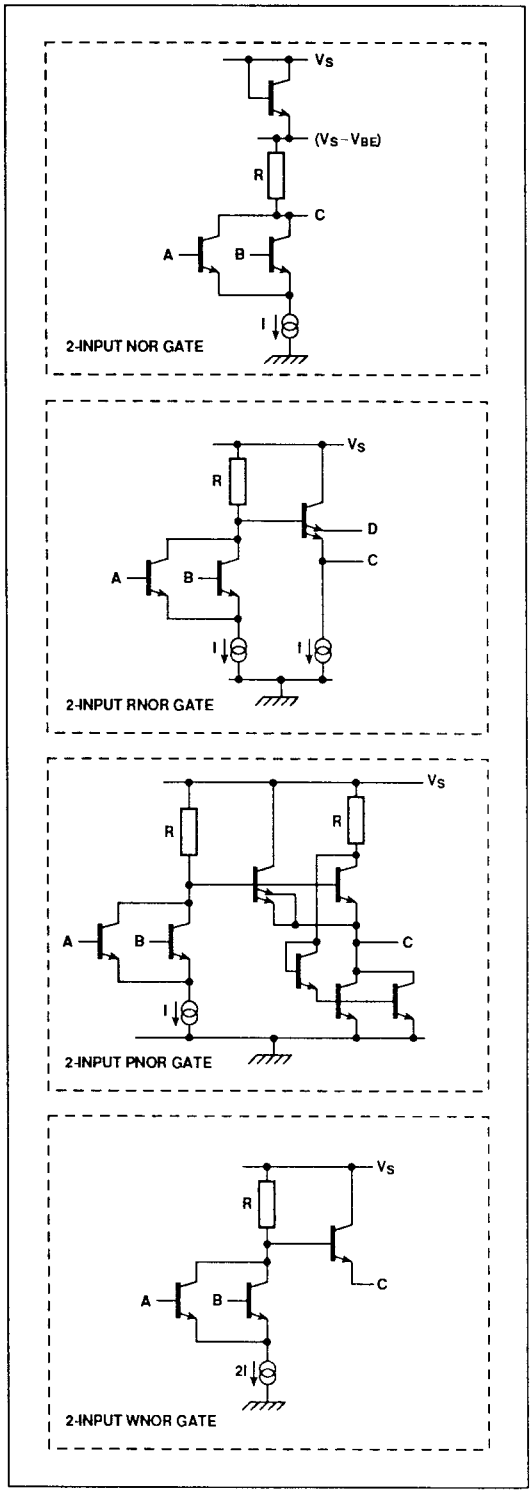


Fig. 5 DF logic gate schematic

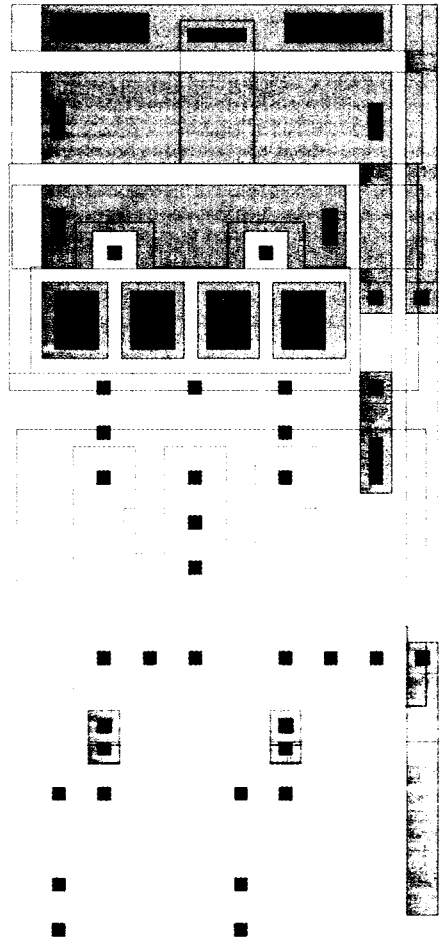


Fig. 6 DF matrix cell layout

DIFFERENTIAL LOGIC

'Differential logic' is a radical approach to logic function design. It can provide an order of magnitude improvement in speed-power product, ensuring that system power levels are kept to a minimum. It achieves a two to four times improvement in speed, with the added advantage that the standard D-type flip-flop clock to output delay is less than two equivalent gate delays.

Differential logic is based on steering current through a logic tree by means of differential pairs of transistors stacked across the supply. Many complex functions can be achieved using this technique. It eliminates the need to generate and distribute accurate temperature compensated voltage references.

A differential pair of transistors also has an extremely linear and sharp transfer characteristic, allowing the use of logic swings as low as 100mV, with excellent discrimination between logic levels.

Differential logic functions are configured from matrix components and offer sub-nanosecond equivalent delays at frugal power levels (see Table 4). Here, complete functions such as D-types are built up as ready-defined macros as shown in Fig. 7. As an illustration of the performance benefits, consider a D-type which offers a clock to output delay of 2·3ns. This performance is equivalent to a gate delay of 800ps and, moreover, the differential logic element consumes only one third the power of a conventional implementation using gates.

In asynchronous systems, the susceptibility to data errors is a major consideration. Data errors occur when latches are clocked at or near a change of input data state, which leads to 'metastability errors'. The differential logic macros include 'metastability hardened' elements offering improved data error rates for high speed asynchronous systems. They also automatically provide the true and inverse of every output and input, eliminating the need for dedicated inverters.

Differential Logic Performance

The figures given in Table 4 relate to a 2-level differential logic D-type with reset (Macro DF2DT1SRL1). The clock input and Q output are level 1, and the data input is on level 2, as shown in Fig. 7.

Parameter	Value
$t_{PD(0)}$ CLOCK to QL1	2·5ns
$t_{PD(1)}$ CLOCK to QL1	2·5ns
$t_{PD(0)}$ RESET to QL1	2·6ns
$t_{PD(1)}$ SET to QL1	2·6ns
$t_{SET\ UP(0)}$ Data input	1·6ns
$t_{SET\ UP(1)}$ Data input	1·6ns
$t_{HOLD(0)}$ Data input	0ns
$t_{HOLD(1)}$ Data input	0ns
I_G (average)	495µA

Table 4 Differential logic performance

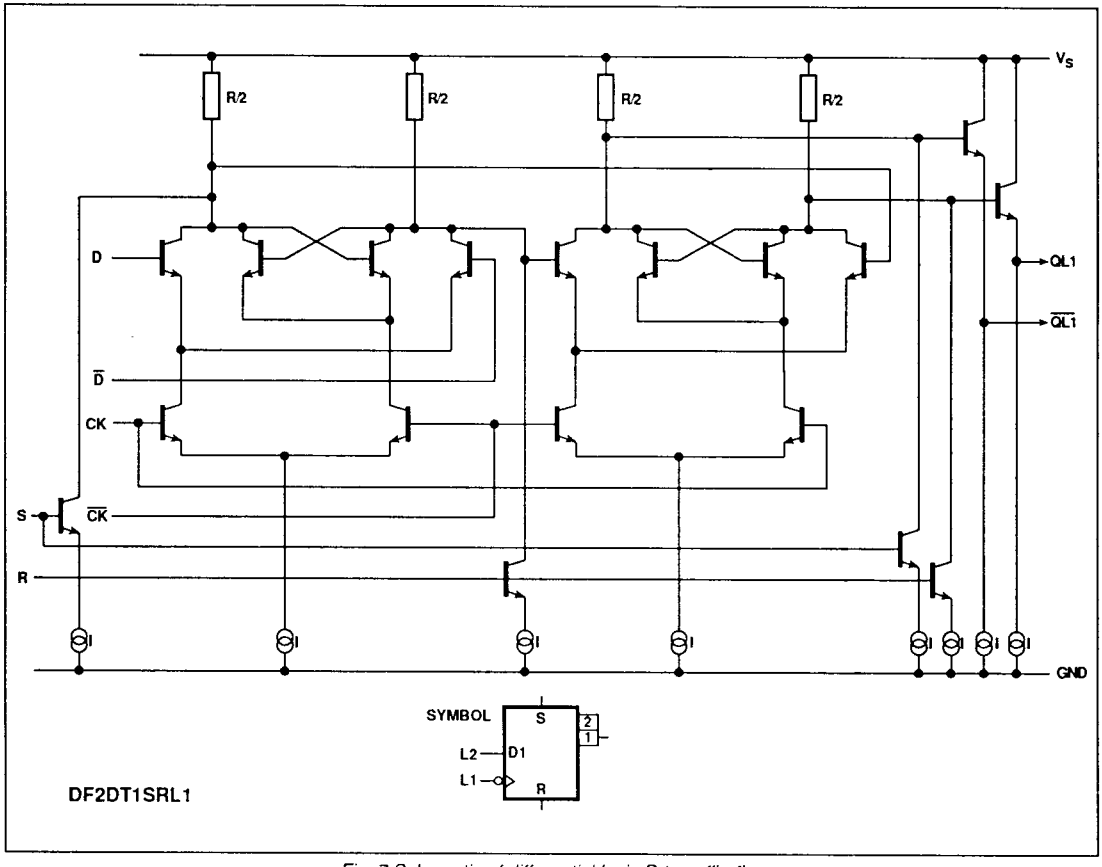


Fig. 7 Schematic of differential logic D-type flip-flop

CHARACTERISTICS

All DF series ULAs are designed to operate over the full temperature range of −55°C to +125°C, therefore embracing all the various military, industrial and commercial temperature ranges.

ABSOLUTE MAXIMUM RATINGS

Operation at Absolute Maximum Ratings is not implied. Exposure to stresses greature than those listed may affect reliability and could cause permanent damage to the device.

Supply voltage V_{CC}	−0·5V to +7·0V
Input voltage V_{IN} (at V_{CC} = 5V)	−0·5V to +5·5V
Operating temperature range T_{AMB}	−55°C to +125°C
Storage temperature range T_{STG}	−65°C to +150°C

DC CHARACTERISTICS

All parameters are for nominal V_{CC} = 5V over the temperature range.
T_{AMB} = 0°C to +70°C unless otherwise specified.

Characteristic	Macro type	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}		4·75	5·0	5·25	V	Commercial/industrial
		4·5	5·0	5·5	V	Military
High level input voltage, V_{IH}	DF2	2·0		5·5	V	High performance TTL input buffer
	DF6		4·1		V	ECL input
Low level input voltage, V_{IL}	DF2	0		0·8	V	High performance TTL input buffer
	DF6		3·3		V	ECL input
High level input current, I_{IH}	DF2	0		20	μA	High performance TTL input buffer (V_{IH}=V_{CC})
	DF6		10		μA	ECL input (V_{IH} = V_{CC})
Low level input current, I_{IL}	DF2			−0·4	mA	High performance TTL input buffer (V_{IL}=0·8V)
	DF6		10		μA	ECL input
High level output voltage, V_{OH}	DF31	2·4			V	Totem pole output (I_O = I_{OH} max.)
	DF32	2·4	3·4		V	Tristate output (I_O = I_{OH} max.)
	DF50		V_{CC}−1·0		V	ECL output (I_O = I_{OH} max.)
Low level output voltage, V_{OL}	DF31			0·5	V	Totem pole output (I_O = I_{OL} max.)
	DF32			0·5	V	Tristate output (I_O = I_{OL} max.)
	DF50		V_{CC}−1·8		V	ECL output (I_O = I_{OL} max.)
High level output current, I_{OH}	DF31			−400	μA	Totem pole output
	DF32			−400	μA	Tristate output at V_{OH} min.
Low level output current, I_{OL}	DF31			12	mA	Totem pole output (V_{OL} = 0·5V)
	DF32			12	mA	Tristate output (V_{OL} = 0·5V)
	DF38			8	mA	Open collector (V_{OL} = 0·5V)
Output leakage current, I_{OZ}	DF32			±10	μA	Tristate
	DF38			10	μA	Open collector (V_{OH} = V_{CC})

AC CHARACTERISTICS

The DF process LE2 technology library contains all the timing information for each cell in the design library. This information is accessible to the simulator, which calculates propagation delays for all signal paths in the circuit design. The EDA simulator can automatically derate timings according to various factors, such as:

Supply voltage variation (from 5V)
Chip temperature
Processing tolerance
Gate fan-out
Input transition time
Input signal polarity
Interconnection wiring

For initial assessments of feasibility, worst case estimations can be done in the following manner, at 25°C and 5V nominal. Similar calculations may be applied for any voltage and temperature relevant to the application. An additional safety factor of ±5% may be applied for conservative design.

- For temperature, a derating multiplier, K_T, of 0·4% per °C should be used.
- For supply voltage derating a factor, K_V, of −20% per volt should be used (this also includes capacitance, f_T and logic changes).
- For manufacturing variation, K_P, the tolerance is ±30%.

The maximum variation on typical delays over the commercial grade product at 4·75V and T_{AMB} = +70°C (assuming a junction temperature of +90°C) will be:

$$t_{PD\,(max.)} = K_P \times K_V \times K_T \times t_{PD\,(typ.)}$$
$$= 1{\cdot}30 \times [1+(5{\cdot}0-4{\cdot}75)0{\cdot}20] \times [1+(90-25)0{\cdot}004] \times t_{PD}$$
$$= 1{\cdot}30 \times (1+0{\cdot}05) \times (1+0{\cdot}26) \times t_{PD\,(typ.)}$$
$$= 1{\cdot}30 \times 1{\cdot}05) \times (1{\cdot}126) \times t_{PD\,(typ.)}$$
$$= 1{\cdot}72 \times t_{PD\,(typ.)}$$

By similar calculation, the minimum delay, $t_{PD\,(min.)}$, at 5·25V and 0°C will be:

$$t_{PD\,(min.)} = 0{\cdot}7 \times 0{\cdot}95 \times 0{\cdot}9 \times t_{PD\,(typ.)}$$
$$= 0{\cdot}6 \times t_{PD\,(typ.)}$$

DESIGN SUPPORT AND INTERFACES

EDA Design Software

The EDA (Electronic Design Automation) software is a complete suite for the design, simulation and implementation of ULA based products. It was developed in parallel with the ULA families to ensure complete compatibility between the design environment and the chip hardware.

Design Entry

Design Entry of DF series is by schematic capture or high level description language using compatible EDA software. It covers both the the structural and behavioural aspects of the design.

The structural aspect of the design is automatically described in the Logic Description Language and the behavioural description is the high level Test Description Language used for writing functional test schedules.

Both descriptions provide direct entry into the EDA design database.

Design Interface

DF series designs can be carried out either by GPS or the customer, using one of a number of customer entry levels, such as:

- The customer produces a verified breadboard and test schedule and GPS performs a turnkey design from this stage through to samples.
- The customer designs on her/his workstation using standard Design Elements and carries out functional and timing simulation.
- The customer designs using GPS Design Elements in a EDA Design Environment Software compatible system.

The DF Series Design Route

The overall ULA design takes place in two software environments: the Design Environment and the Physical Environment (see Fig. 8).

Design Environment

The hierarchical EDA design database contains the complete design and is central to design entry, simulation and test schedule verification.

The test schedule can range from simple truth table to a full high level specification. The test schedule is used for simulation and to generate functional programs automatically for the production test machines. The simulation software in EDA covers both logic and circuit simulation.

Physical Environment

When the ULA design has been fully verified the data from th Design Environment is transferred to the GPS Design Centre for completion of the Physical Enivronment.

The Physical Environment is a complete suite of software which handles all aspects of the physical chip design. The silicon compiler which produces the physical layout is fully automatic without the need for manual intervention.

On completion of the physical layout, the track loading information is used by the simulator to verify the dynamic performance.

The verified layout data is used to generate PG tapes for mask making. Engineering check samples are manufactured, tested and supplied to the customer, together with a complete tast record for evaluation and approval.

DESIGN REVIEWS

Design reviews are an integral part of the support provided by GEC Plessey Semiconductors during the development of a Semi-Custom integrated circuit. These reviews are scheduled meetings between the customer's representative and the allocated project engineer. They ensure that all the correct design procedures have been observed to date and that the procedures and requirements for the next phase are fully understood.

A total of four design reviews are held prior to full production. These reviews are:

- **Design Review 1** – Initial concept and system specification.
- **Design Review 2** – On completion of design and simulation.
- **Design Review 3** – On completion of layout and post-layout simulation.
- **Design Review 4** – On supply of prototypes prior to approval for full production.

At the end of the design and layout phase and when Design Review 3 has been completed, GPS manufactures prototypes. The test program is generated as part of the design process and is used to test the prototypes. This program is extended, on approval of prototypes, for finished production product.

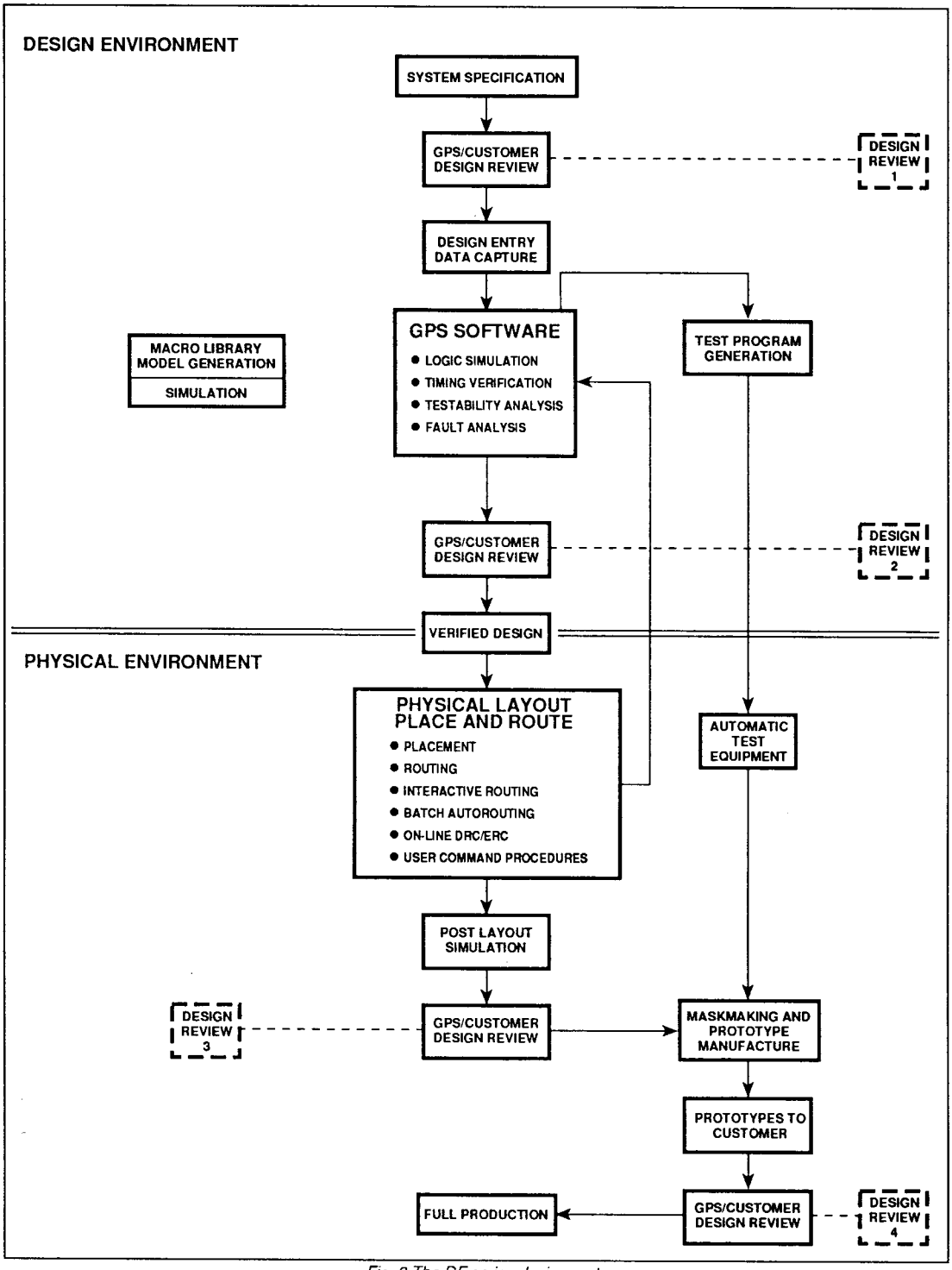


Fig. 8 The DF series design route

SPECIAL ANALOG FUNCTIONS

Each DF series array features a programmable bandgap reference and 4 high current transistors as detailed in Table 6.

Parameter	Value	Units	Conditions
Bangap			
Voltage range (buffered output)	1·3-2·6	V	Mask programmed
Output voltage temperature coefficient	±100	ppm	V_{OUT} = 1·32V
High current transistor			
I_{CC}	50	mA	V_{OUT} = 0·5V

Table 6 Special analog functions

Function	Number of peripheral cells	Number of pins
Amplifier	2	2
Comparator	2	2
Video amplifier	3	4
AGC amplifier	5	5
Zero crossing comparator	2	2
Hysteresis comparator (Schmitt trigger)	3	1
Precision monostable	2	2
VCO with fast lock	4	4

Table 7 Analog macro examples

SPECIAL FUNCTION MACRO LIBRARY

The list of circuits includes examples of the great variety of circuit configurations that are possible and that have been produced as macros on DF arrays. Examples of the analog capabilities are given in Table 7.

The special function library is being continually enlarged with many of the macros designed to solve the problems met in specific market sectors such as computer peripherals.

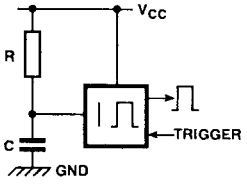
Some examples of macros and their performance characteristics, used and available from DF integrations, can be seen in Fig. 9. Full details of all macros available, as listed in the cell library on the following pages, can be found in the DF Design Manual and the DF Macro Library documents.

The analog performance attainable by the DF series is illustrated by an AGC amplifier from the macro library, shown in Fig. 9. The specification for this amplifier is given in Table 8.

Parameter	Value	Units
Differential input resistance	5·6	kΩ
Differential input bias current	5	μA
Differential input voltage range	30-400	mV
Max. Gain	80	V/V
Gain control range (min.)	18	dB
Gain control active voltage range	2·3-3·3	V
Gain input current	2	μA
3dB bandwidth	30	MHz
Max. output differential voltage swing	4	V
Output sink current	3	mA
Output resistance (max.)	20	Ω
Reference voltage V_{ACRF}	2·3-2·7	V

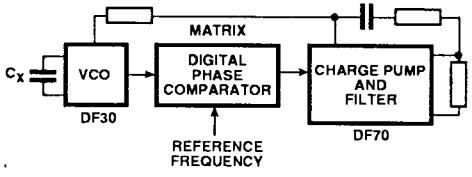
Table 8 AGC amplifier performance

NAME: DF67
FUNCTION: Precision monostable



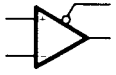
Accurate pulse width, Configurable triggering mode, t = 0·7CR, Pulse widths from 100ns to 100ms.

NAME: DF70 and DF30
FUNCTION: Full phase lock loop (PLL) VCO and charge pump/filter



VCO frequencies to 60MHz; low drift, high linearity VCO. Full phase lock loop functions available.

NAME: DF84
FUNCTION: Wideband (video) amplifier

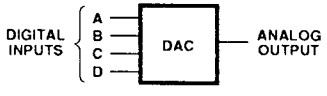


Differential I/P and O/P
Differential gain: 20dB
Bandwidth: 60MHz
Differential O/P voltage: 3Vp-p
I/P Z: 10kΩ, O/P Z: 50Ω

NAME: DF90
FUNCTION: Bandgap voltage reference

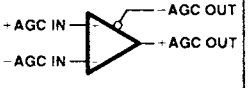
Stable voltage reference: 1·35V wrt GND, Temperature coefficient: 100ppm

NAME: DF94
FUNCTION: 4-bit D to A converter



Accuracy: ± 1/2 LSB, On-chip reference voltage, R-2R ladder network, DAC settling time: 200ns.

NAME: DF87
FUNCTION: AGC amplifier



Bandwidth: 30MHz, AGC gain control range: 18dB, Differential I/P and O/P I/P Z: 5·6kΩ, O/P Z: 20Ω

Fig. 9 Examples of DF macro functions used in integrations

CELL LIBRARY

A most comprehensive cell library is available for the DF series. The implementation of a cell has involved the silicon planning, design rule checking, automatic generation of a SPICE file for performance analysis, SPICE simulation and results extraction, generation of the EDA cell simulator and verification of the cell attributes for layout tools.

Analog and I/O Macros

The DF series has been designed to give outstanding analog performance. The Analog Macro Library encompasses a comprehensive range of analog and I/O functions. These provide a rapid, proven and fully characterised solution to a wide range of circuit requirements. The library is constantly being expanded to include more functions.

Moreover, a new design can be readily created when the exact circuit function does not already exist in library or it is required to optimise the performance of an existing macro.

This can be completed by either GPS or the customer and proven using the comprehensive SPICE parameters available for the DF series.

Input & Output Interface Function Macro Library

These macros provide interfacing to TTL, CMOS ande ECL technologies together with functions such as Schmitt trigger inputs. Also included within the library are macro variations such as ECL inputs with internal voltage reference levels or macros for use with an external source.

ANALOG MACRO LIBRARY

Monostables

DF66	Simple RC monostable
DF67	Precision RC monostable
DF72	Voltage controlled monostable
DF73	Narrow pulse monostable

Oscillators

DF65	Simple RC oscillator
DF68	Crystal oscillator
DF69	Overtone crystal oscillator
DF70	Voltage controlled oscillator
DF71	Switched voltage controlled oscillator
DF74	Precision RC oscillator

Comparators

DF80	Fast voltage comparator
DF81	Low power voltage comparator
DF82	Low offset voltage comparator
DF83	High impedance voltage comparator

Amplifiers

DF84	Video amplifier
DF85	Audio amplifier
DF86	Filter amplifier
DF87	AGC amplifier

References

DF90	1·3V voltage reference
DF91	2·6V voltage reference

Miscellaneous

DF93	Differentiator
DF94	4-bit D to A converter
DF95	Fast flip-flop

I/O MACRO LIBRARY

Inputs

DF2	TTL input
DF4	Low power TTL input
DF5	ECL input plus bias generator
DF6	ECL input
DF7	High impedance TTL input
DF8	Differential ECL input
DF10	Three state input
DF62	Precision Schmitt trigger input
DF63	Schmitt trigger input

Outputs

DF30	Charge pump output
DF31	TTL output
DF32	Tristate output
DF35	Low power TTL output
DF37	Low power tristate output
DF38	Open collector output
DF39	Low power open collector output
DF40	Open collector output with pull up
DF41	Low power open collector O/P with pull up
DF42	24 mA open collector output
DF43	Open emitter output
DF45	48 mA open collector output
DF50	ECL output
DF52	Differential ECL output

Input/Output

DF33	Tristate output/TTL input
DF34	Low power tristate output/low power TTL I/P
DF36	Open collector output/TTL input
DF51	ECL output with differential input

LOGIC CELL LIBRARY

The DF logic cell library contains a listing of all the types of Logic Design Elements available for the DF arrays. These are divided into four groups:

- **Logic Gates** – Basic logic primitives such as NOR gates, RNOR gates etc.
- **Logic Functions** – Flip-flops, Latches etc.
- **Differential Logic Elements** – High speed, low power logic gates and functions.
- **Logic Macros** – Counters, adders, registers, decoders etc.

In this brief listing, only the minimum group of letters required to indicate the generic type of each element is given, with a number of examples to show how each element name is built up. For example, for the family of single input RNOR D-type the generic name is given as DT1. A full D-type flip-flop, that is, one with SET, RESET, Q output and $\overline{Q}$ output, is invoked by the name DT1SRQN. Any unwanted terminals are omitted from the name.

Logic Gates

1- to 8-input primitive gates.

NOR1	RNOR1	PNOR1
NOR2	RNOR2	PNOR2
NOR3	RNOR3	PNOR3
NOR4	RNOR4	PNOR4
NOR5	RNOR5	
NOR6	RNOR6	
NOR7	RNOR7	
NOR8	RNOR8	
WNOR1	FPNOR1	FWNOR1
WNOR2	FPNOR2	FWNOR2
	FPNOR3	FWNOR3
	FPNOR4	FWNOR4

DT SERIES LOGIC CELL LIBRARY (Continued)

Logic Functions

These are further divided into two groups of NOR and RNOR.

(a) NOR logic functions

The prefix 'C' indicates CML

CDT1	1-input D-type flip-flop
CDT2	2-input D-type flip-flop
CDT3	3-input D-type flip-flop
CDT4	4-input D-type flip-flop
CDST1	Special D-type flip-flop
CTT1	T-type flip-flop
CDL1	Level triggered data latch
CEQV	Equivalence gate
CEXOR	Exclusive OR gate
CNMONO	Negative edge triggered narrow pulse monostable
CPMONO	Positive edge triggered narrow pulse monostable

(a) RNOR logic functions

DT1	1-input D-type flip-flop
DT2	2-input D-type flip-flop
DT3	3-input D-type flip-flop
DT4	4-input D-type flip-flop
DST1	Special D-type flip-flop
DTA1	Alternative reset D-type flip-flop
TT1	T-type flip-flop
DL1	Level triggered data latch
REQV	Equivalence gate
REXOR	Exclusive-OR gate
NMONO	Negative edge triggered narrow pulse monostable
PMONO	Positive edge triggered narrow pulse monostable

Differential Logic Elements (2-Level)

DF2L1	CML to DCML, level 1 output
DF2L2	CML to DCML, level 2 output
DF2L12	CML to DCML, level 1 and 2 output
DF2ANDL1	2-input AND gate, level 1 output
DF2ANDL2	2-input AND gate, level 2 output
DF2ANDL12	2-input AND gate, level 1 and 2 output
DF2DL1L1	Data latch, level 1 output
DF2DL1L2	Data latch, level 2 output
DF2DL1L12	Data latch, level 1 and 2 output
DF2DT1L1	D-type flip-flop, level 1 output
DF2DT1L2	D-type flip-flop, level 2 output
DF2DT1L12	D-type flip-flop, level 1 and 2 output
DF2DT1RL1	D-type flip-flop with Reset, level 1 output
DF2DT1RL2	D-type flip-flop with Reset, level 2 output
DF2DT1RL12	D-type flip-flop with Reset, level 1 and 2 output
DF2DT1SRL1	D-type flip-flop with Set/Reset, level 1 output
DF2DT1SRL2	D-type flip-flop with Set/Reset, level 2 output
DF2DT1SRL12	D-type flip-flop with Set/Reset, level 1 and 2 output
DF2EXORL1	Exclusive-OR gate, level 1 output
DF2EXORL2	Exclusive-OR gate, level 2 output
DF2EXORL12	Exclusive-OR gate, level 1 and 2 output
DF2CMLT	DCML to CML, True output
DF2CMLW	DCML to CML, Wire-OR output
DF2CMLTW	DCML to CML, True and Wire-OR output
DF2SELL1	2-1 Selector, level 1 output
DF2SELL2	2-1 Selector, level 2 output
DF2SELL12	2-1 Selector, level 1 and 2 output
DF2DTS1RL1	Special D-type flip-flop, level 1 output
DF2DTS1RL2	Special D-type flip-flop, level 2 output
DF2DTS1RL12	Special D-type flip-flop, level 1 and 2 output
DF2LRL2	Level 1 to level 2
DF2DELL1	Delay, level 1 output
DF2DELL2	Delay, level 2 output
DF2LSL1	Level 2 to level 1
DF2DL1RL1	Data latch with Reset, level 1 output
DF2DL1RL2	Data latch with Reset, level 2 output
DF2DL1RL12	Data latch with Reset, level 1 and 2 output
DF2MDL1L2	Metastable resistant Latch, level 2 output
DF2MDL1RL2	Metastable resistant Latch with Reset, level 2 output
DF2ANDCML	2-input AND gate, CML output
DF2DL1CML	Data Latch, CML output
DF2DL1RCML	Data Latch with Reset, CML output
DF2DT1CML	D-type flip-flop, CML output
DF2DT1RCML	D-type flip-flop with Reset, CML output
DF2DT1SRCML	D-type flip-flop with Set/Reset, CML output
DF2DTS1RCML	Special D-type flip-flop, CML output
DF2EXORCML	Exclusive-OR gate, CML output
DF2SELCML	2-1Selector, CML output
DF2DELPER	Delay, level 2 output to peripheral
DF2ANDPER	2-input AND gate, level 2 output to peripheral
DF2DL1PER	Data Latch, level 2 output to peripheral
DF2DL1RPER	Data Latch with Reset, level 2 output to peripheral
DF2DT1PER	D-type flip-flop, level 2 output to peripheral
DF2DT1RPER	D-type flip-flop with Reset, level 2 output to peripheral
DF2DT1SRPER	D-type flip-flop with Set/Reset, level 2 output to peripheral
DF2DTS1RPER	Special D-type flip-flop, level 2 output to peripheral
DF2EXORPER	Exclusive-OR gate, level 2 output to peripheral
DF2SELPER	2-1Selector, level 2 output to peripheral
DF2LRPER	Level 1 to level 2 peripheral
DF2L2PER	CML to level 2 peripheral

Logic Macro Functions

The Logic Macro Function Library comprises a set of commonly used logic functions which can be used in conjunction with all other Logic Design Elements or Logic Cells.

The same notation is used here as with the Logic Function Library in that each example is of the full element complete with SET and RESET where applicable. Functions which are available in both NOR and RNOR logic are prefixed (C).

(a) Gates

NAND2	2-input NAND gate
NAND3	3-input NAND gate
NAND4	4-input NAND gate
(C)OA22	2-input, 2-wide OR-NAND
(C)OA23	2-input, 3-wide OR-NAND
(C)OA24	2-input, 4-wide OR-NAND
(C)OA32	3-input, 2-wide OR-NAND
OA33	3-input, 3-wide OR-NAND
(C)OA34	3-input, 4-wide OR-NAND
(C)OA232	2, 3-input, 2-wide OR-NAND

(b) Flip-flops

(C)SR	S-R flip-flop
WDT	D-type flip-flop with wired-OR outputs, e.g. WDTSR
(C)MDT	D-type flip-flop with multiplexed data input, e.g. (C)MDTSR
(C)JK	J-K flip-flop, e.g. (C)JKSR
(C)JNK	JNK flip-flop, e.g. (C)JNKSR
(C)TE	Toggle enable D-type flip-flop, e.g. (C)TESR

(c) Multiplexers

(C)MPX2	2- to 1-line multiplexer
(C)MPX4	4- to 1-line multiplexer
(C)MPX8	8- to 1-line multiplexer
(C)MPX16	16- to 1-line multiplexer

(d) Data selectors

(C)DSL2	1- to 2-line data selector
(C)DSL4	1- to 4-line data selector
(C)DSL8	1- to 8-line data selector
(C)DSL16	1- to 16-line data selector

(e) Decoders

(C)DEC4	2- to 4-line decoder
(C)DEC8	3- to 8-line decoder
(C)DEC16	4- to 16-line decoder

(f) Comparators

(C)EQCOM4	4-bit equality comparator
(C)MCOM4	4-bit magnitude comparator

(g) Adders

(C)HA	Half adder
(C)GFA	Gated full adder

(h) Registers

(C)DR4	4-bit clocked data register, e.g. (C)DR4R
(C)DR6	6-bit clocked data register, e.g. (C)DR6R
(C)DR8	8-bit clocked data register, e.g. (C)DR8R
(C)TDL4	4-bit transparent data latch, e.g. (C)TDL4R
(C)TDL6	6-bit transparent data latch, e.g. (C)TDL6R
(C)TDL8	8-bit transparent data latch, e.g. (C)TDL8R

(i) Counters

(C)A4BRC	4-bit ripple counter, e.g. (C)A4BRC
(C)A6BRC	6-bit ripple counter, e.g. (C)A6BRC
(C)A8BRC	8-bit ripple counter, e.g. (C)A8BRC
(C)SD3C	Synchronous ÷3 counter, e.g. (C)SD3CR
(C)SD5C	Synchronous ÷5counter, e.g. (C)SD5CR
(C)AD6C	Asynchronous ÷6counter, e.g. (C)AD6CR
(C)AD7C	Asynchronous ÷7counter, e.g. (C)AD7CR

(j) Synchronous binary counters

(C)SBUC4	4-bit binary up counter, e.g. (C)SBUC4R
(C)SBDC4	4-bit binary down counter, e.g. (C)SBDC4R
(C)SBUDC4	4-bit binary up/down counter, e.g. (C)SBUDC4R
(C)SPBUC4	Presettable binary up counter
(C)SPBUC4RC	Presettable binary up counter with carry-out and reset
(C)SPBDC4	Presettable binary down counter
(C)SPBDC4SC	Presettable binary down counter with carry-out and set

(j) Synchronous decade counters

(C)SDUC4	4-bit decade up counter, e.g. (C)SDUC4R
(C)SDDC4	4-bit decade down counter, e.g. (C)SDDC4R
(C)SDUDC4	4-bit decade up/down counter, e.g. (C)SDUDC4R
(C)SPDUC4	Presettable decade up counter
(C)SPDUC4RC	Presettable decade up counter with carry-out and reset
(C)SPDDC4	Presettable decade down counter
(C)SPDDC4SC	Presettable decade down counter with carry-out and set

(k) Shift registers

(C)PISO	4-bit synchronous PISO, e.g. (C)PISOR

PACKAGING

A wide variety of ceramic and plastic package styles are available. Packages in clude dual-in-line, flatpacks, chip carriers, small outline (SO) packages and pin grid arrays.

The selection of a suitable package for a given application is determined by a number of factors:

- Number of input and output pins
- Number of power supply connections
- Application environment and temperature range
- Array die size relative to package island size
- Power dissipation
- Method of mounting package to PCB

Production quantities of the DF series ULAs are available in industry-standard ceramic and plastic packages as shown below in Table 9. Prototype samples are normally supplied in ceramic only. Where plastic production packages are requested, ceramic prototypes will be supplied in the nearest equivalent and tested to the final test specification.

QUALITY AND RELIABILITY

At GEC Plessey Semiconductors, quality and reliability are built into the product by rigorous control of all processing operations and by minimising random uncontrolled effects in all manufacturing operations. Process management involves full documentation of all procedures, recording of batch-by-batch data, using traceability procedures and the provision of appropriate equipment and facilities to perform sample screens and conformance testing on finished product.

A common management system is used to control the manufacturing of GPS processes. All products benefit from the use of an integrated monitoring system throughout manufacturing, which leads to high quality standards for all technologies.

Further information is contained in the Quality Brochure, available from GEC Plessey Semiconductors Sales Offices.

Package code	Package type	Through board	Surface mount	Description
DC	DILMON	✓		Dual-in-line, multilayer ceramic. Brazed leads. Metal sealed lid.
DG	CERDIP	✓		Dual-in-line, ceramic body. Alloy leadframe. Glass sealed.
DP	PLASDIP	✓		Dual-in-line, plastic moulded. Copper or alloy leadframe.
AC	PGA	✓		Pin Grid Array, multilayer ceramic. Metal sealed lid.
MP	Small Outline		✓	Dual-in-line, plastic moulded. 'Gullwing' formed leads.
LC	LCC		✓	Leadless Chip Carrier, multilayer ceramic. Metal sealed lid.
HC	Leaded Chip Carrier		✓	Quad multilayer ceramic. Brazed 'J'-formed leads. Metal sealed lid.
GC	Leaded Chip Carrier		✓	Quad multilayer ceramic. Brazed 'Gullwing' leads. Metal sealed lid.
HG	Quad CERPAC		✓	Quad ceramic body. 'J'-formed leads. Glass sealed.
GG	Quad CERPAC		✓	Quad ceramic body. 'Gullwing'-formed leads. Glass sealed.
HP	PLCC		✓	Quad leaded plastic chip carrier. 'J'-formed leads.
GP	PQFP		✓	Quad plastic flatpack. 'Gullwing'-formed leads.

Table 9 Available package types