

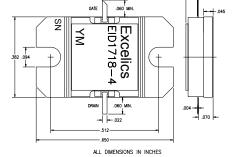
EID1718-4

17.30-18.10 GHz 4-Watt Internally-Matched Power FET

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FEATURES

- 17.30-18.10 GHz Bandwidth
- **Input/Output Impedance Matched to 50 Ohms**
- +36.0 dBm Output Power at 1dB Compression
- 6.0 dB Power Gain at 1dB Compression
- 25% Power Added Efficiency
- **Hermetic Metal Flange Package**



ELECTRICAL CHARACTERISTICS ($T_a = 25^{\circ}C$)

OVMDOL	DADAMETERO TEST SONDITIONS	BAINI	TVD	BAAV	LINUTO
SYMBOL	PARAMETERS/TEST CONDITIONS ¹	MIN	TYP	MAX	UNITS
P _{1dB}	Output Power at 1dB Compression $f = 17.30-18.10GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 1200\text{mA}$	35.5	36.0		dBm
G _{1dB}	Gain at 1dB Compression $f = 17.30-18.10GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 1200\text{mA}$	5.0	6.0		dB
ΔG	Gain Flatness $f = 17.30-18.10GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 1200\text{mA}$			±0.6	dB
PAE	Power Added Efficiency at 1dB Compression $V_{DS} = 10 \text{ V}, I_{DSQ} \approx 1200 \text{mA}$ f = 17.30-18.10GHz		25		%
Id _{1dB}	Drain Current at 1dB Compression f = 17.30-18.10GHz		1300	1800	mA
IM3	Output 3rd Order Intermodulation Distortion Δf = 5 MHz 2-Tone Test; Pout = 30.0 dBm S.C.L ² V_{DS} = 10 V, I_{DSQ} ≈ 65% I_{DSS} f =18.10GHz	-29.0	-34.0		dBc
I _{DSS}	Saturated Drain Current $V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}$		2080	2880	mA
V_P	Pinch-off Voltage $V_{DS} = 3 \text{ V}, I_{DS} = 20 \text{ mA}$		-2.5	-4.0	V
R _{TH}	Thermal Resistance ³		4.5	5.5	°C/W

- Tested with 100 Ohm gate resistor.
- S.C.L. = Single Carrier Level.
- Overall Rth depends on case mounting.

ABSOLUTE MAXIMUM RATINGS FOR CONTINUOUS OPERATION1,2

SYMBOL	CHARACTERISTIC	VALUE	
V_{DS}	Drain to Source Voltage	10 V	
V_{GS}	Gate to Source Voltage	-4.5 V	
I _{DS}	Drain Current	IDSS	
I _{GSF}	Forward Gate Current	40 mA	
P _{IN}	Input Power	@ 3dB compression	
P_T	Total Power Dissipation	23.0 W	
T _{CH}	Channel Temperature	150°C	
T_{STG}	Storage Temperature	-65/+150°C	

Operating the device beyond any of the above ratings may result in permanent damage or reduction of MTTF. Bias conditions must also satisfy the following equation $P_T < (T_{CH} - T_{PKG})/R_{TH}$, where $T_{PKG} =$ temperature of package, and $P_T = (V_{DS} * I_{DS}) - (P_{OUT} - P_{IN}).$

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