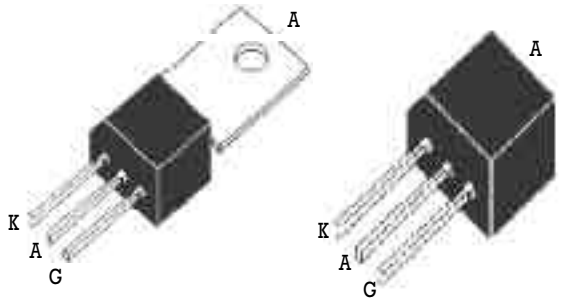
SENSITIVE GATE SCR

TO202-1 (E) TO202-3 (F)



On-State Current
8 Amp

Gate Trigger Current
< 200 µA

Off-State Voltage
200 V ÷ 600 V

These series of **S**ilicon **C**ontrolled **R**ectifier use a high performance PNPN technology.

These parts are intended for general purpose applications where high gate sensitivity is required.

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, T_c = 110 °C		8	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, Θ = 180 °, T_C = 110 °C		5	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz		73	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz		70	A
I^2t	Fusing Current	t_p = 10ms, Half Cycle		24.5	A^2s
V_{GRM}	Peak Reverse Gate Voltage	I_{GR} = 10 µA		8	V
I_{GM}	Peak Gate Current	20 µs max.		4	A
P_{GM}	Peak Gate Dissipation	20 µs max.		5	W
$P_{G(AV)}$	Gate Dissipation	20ms max.		1	W
T_j	Operating Temperature		-40	+125	°C
T_{stg}	Storage Temperature		-40	+150	°C
T_{sld}	Soldering Temperature	10s max.		260	°C

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			B	D	M	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	R_{GK} = 1 KΩ	200	400	600	V

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		SENSITIVITY	Unit
				02	
I_{GT}	Gate Trigger Current	V_D = 12 V_{DC} , R_L = 140Ω. T_j = 25 °C	MIN MAX	 200	µA
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}$, R_{GK} = 220Ω T_j = 125 °C $V_R = V_{RRM}$, T_j = 25 °C	MAX MAX	1 5	mA µA
V_{TM}	On-state Voltage	at I_T = 16 Amp, tp = 380 µs, T_j = 25 °C	MAX	1.6	V
V_{GT}	Gate Trigger Voltage	V_D = 12 V_{DC} , R_L = 140Ω, T_j = 25 °C	MAX	0.8	V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}$, R_L = 3.3KΩ, R_{GK} = 220Ω T_j = 125 °C	MIN	0.1	V
I_H	Holding Current	I_T = 50 mA , R_{GK} =1KΩ T_j = 25 °C	MAX	5	mA
I_L	Latching Current	I_G = 1 mA R_{GK} =1KΩ	MAX	6	mA
dv / dt	Critical Rate of Voltage Rise	V_D = 0.67 x V_{DRM} , R_{GK} = 220Ω T_j = 125 °C	MIN	5	V/µs
di / dt	Critical Rate of Current Rise	I_G = 2 x I_{GT} Tr ≤ 100 ns, T_j = 125 °C	MIN	50	A/µs
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC			20	°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC			100	°C/W
V_{t0}	Threshold Voltage	T_j = 125 °C	MAX	0.85	V
R_d	Dynamic resistance	T_j = 125 °C	MAX	46	mΩ

PART NUMBER INFORMATION

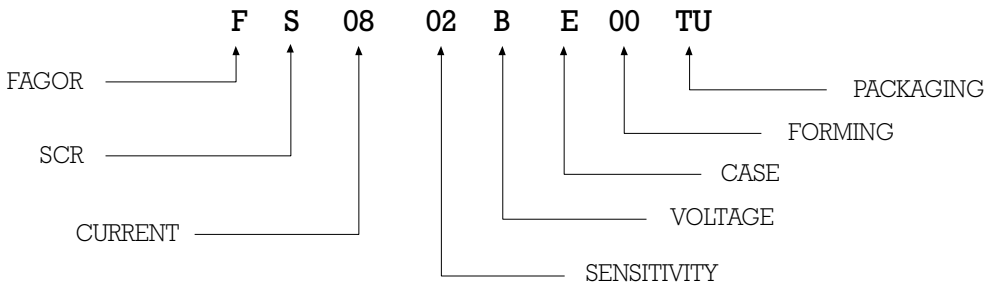


Fig. 1: Maximum average power dissipation versus average on-state current.

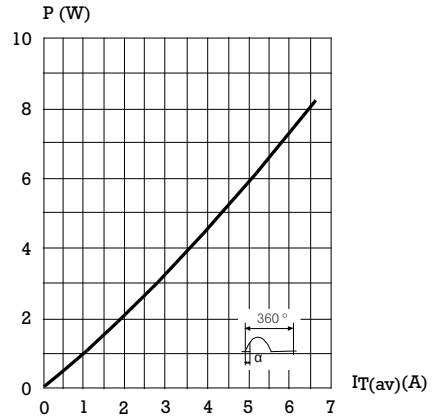


Fig. 2: Average and D.C. on-state current versus case temperature.

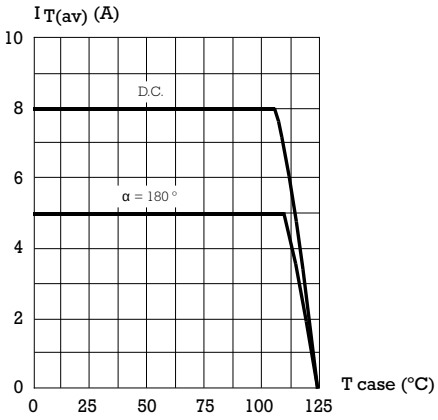


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration.

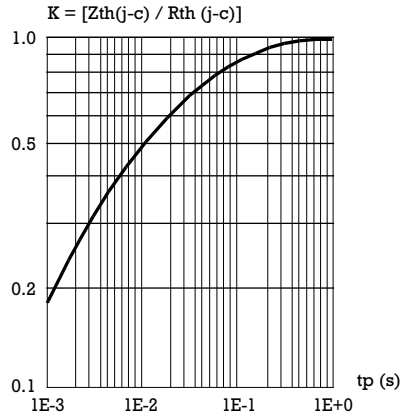


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

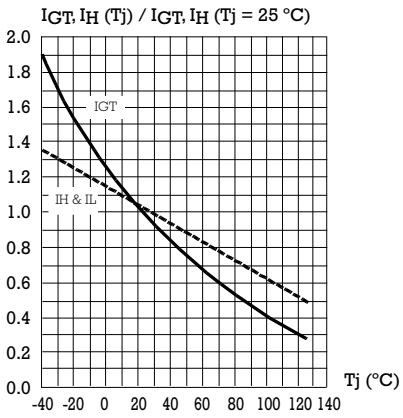


Fig. 5: Non repetitive surge peak on-state current versus number of cycles.

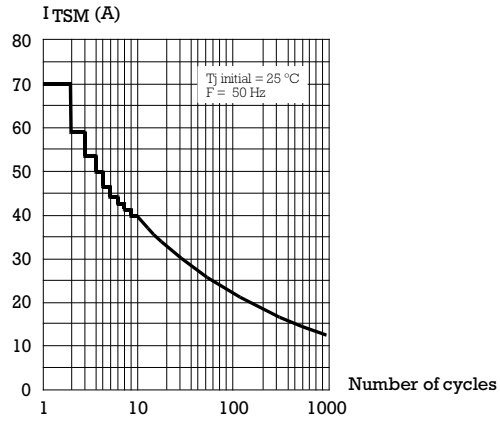


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I^2t.

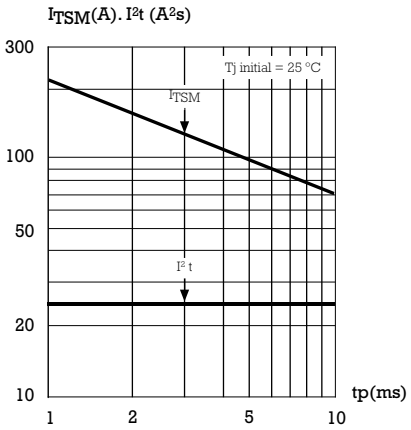
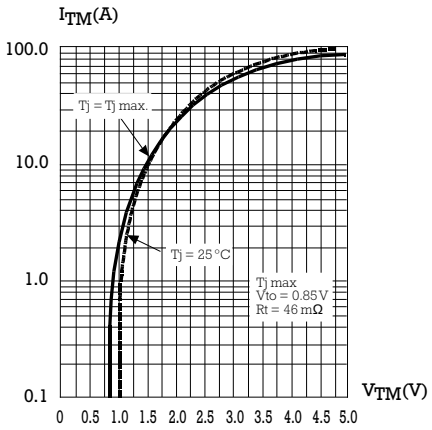
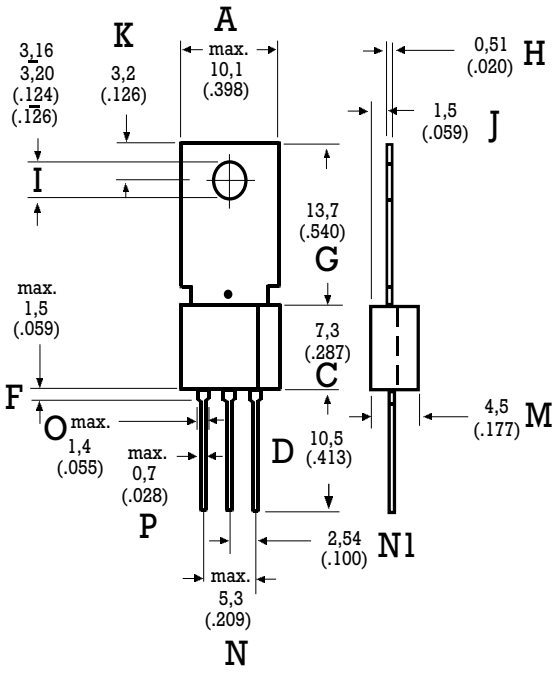


Fig. 9: On-state characteristics (maximum values).



PACKAGE MECHANICAL DATA TO 202-1 TO 202-3

TO 202-1



TO 202-3