FAIRCHILD
SEMICONDUCTOR®

AN7820/24
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- 20 and 40 MSPS Conversion Rate
- On-Board Clock Drivers
- Data Output and Strobe Signal
- User Selectable Capture Clock
- On-Board Reference Drivers

APPLICATIONS

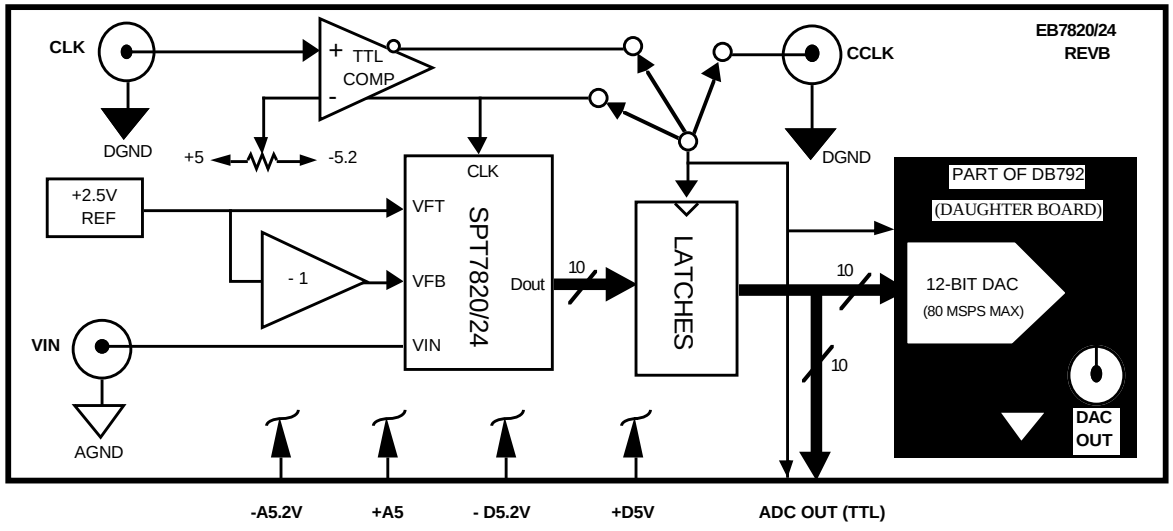
- Evaluation of SPT7820 and SPT7824
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Guide for System Layout

GENERAL DESCRIPTION

The EB7820/24 evaluation board demonstrates the performance of the SPT7820 and SPT7824, monolithic high speed analog-to-digital converters (ADCs). This document can used as an application note and as supplemental information to the existing data sheets (SPT7820 or SPT7824). Both the SPT7820 and SPT7824 have analog input ranges of ±2 V.

The SPT7820 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 20 MSPS, while the SPT7824 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 40 MSPS. Both devices are pin-compatible. All input/output logic is TTL-compatible.

Figure 1: EB7820/24 Block Diagram. (The full detail schematic is shown in figure 17.)



The EB7820/24 (≈ 4" X 7.5") consists of five separate sections:

- Reference circuits
- Clock circuits
- SPT7820 or SPT7824, 10-bit ADC (not included with the board)
- Output latches available through 26-pin female ribbon connector
- The DB792 DAC reconstruction board is a separate daughter board (≈ 2.5" X 3.0") that directly interfaces with the EB7820/24

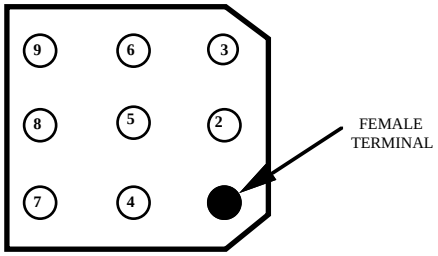
POWER SUPPLIES

EB7820/24 requires four power supply sources: analog -5.2 V (-A5.2 V), analog +5 V (+A5 V), digital - 5.2 V (- D5.2 V), and digital +5 V (+D5 V) . P1 is the power connector. (See figure 2.) The recommended operating voltage range is shown in table 1.

Table 1 - Recommended Power Supply Operating Range

PS	Min	Typ	Max	Typ Current
-A5.2 V	-4.95 V	-5.20 V	- 5.45 V	60 mA
+A5 V	+4.75 V	+5.00 V	+5.25 V	240 mA
-D5.2 V	-4.95 V	-5.20 V	- 5.45 V	15 mA
+D5 V	+4.75 V	+5.00 V	+5.25 V	60 mA

Figure 2 - P1, Power Supply Connector's Pin Assignment



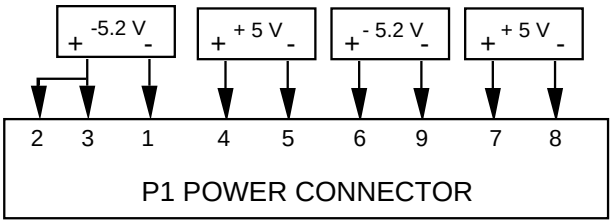
P1 (top view)

PIN#	PIN ASSIGNMENT
1	ANALOG - 5.2 V
2	ANALOG - 5.2 V RETURN # 1 (AGND)
3	ANALOG - 5.2 V RETURN # 2 (AGND)
4	ANALOG + 5V
5	ANALOG + 5 V RETURN (AGND)
6	DIGITAL - 5.2 V RETURN (DGND)
7	DIGITAL + 5 V
8	DIGITAL + 5 V RETURN (DGND)
9	DIGITAL - 5.2 V

The total power dissipation is typically 1.89 watts, including the SPT7820 or SPT7824 (1.1 W typ).

POWER SUPPLY HOOK-UPS

Figure 3 - P1 Connector/Hook-Up



POWER SUPPLIES AND GROUNDING

The SPT7820/24 requires two analog supply voltages: -A5.2 V and +A5 V. The +A5 V supply is common to analog VCC (pin 18 &25) and digital DVCC (pin 14 and 28). A ferrite bead in series with each supply (RF1 and RF2) reduces the transient noise injected into VCC. The bead (RF1 or RF2) to SPT7820/24 connections should not be shared with any other device. Bypass each power supply pin as closely as possible to the device (0.1 μF to AGND for each VEE and VCC pin and 0.01 μF to DGND for the DVCC pin).

AGND and DGND are isolated on the SPT7820 and SPT7824. Both -A5.2 V and +A5 V are the analog supply sources. As in most very high speed ADCs, grounding is critical. Therefore, the ground plane technique is the most desirable for the SPT7820/24. To accomplish this, split and tie together the AGND and DGND ground planesonly at the device (SPT7820/24) through an RF bead. The EB7820/24 is a four-layer printed circuit board: the top signal, ground (AGND & DGND) plane, power plane and the bottom signal. The two ground planes are connected together at the device through a ferrite bead (RF3). All three ferrite beads (RF1-3) are located close to the ADC.

The analog input (pin 21) is physically sandwiched between the reference taps. Carefully plan printed circuit board layout to minimize any pick-up from VIN (high frequency) into the references (VFT or VFB).

REFERENCE CIRCUIT

The SPT7820/24 requires the use of two voltage references: VFT and VFB. VFT is the force for the top of the voltage reference ladder (+2.5 V typ), and VFB (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 900 Ω. In addition, there are three reference ladder taps: VST, VRM and VSB. VST is the top of the reference ladder tap (+2 V), VRM is the middle point (0.0 V typ), and VSB is the bottom of the reference ladder tap (-2 V). The voltages seen at VST and VSB are the expected full scale input voltages of the device when VFT and VFB are driven to the recommended voltages (+2.5 V and -2.5 V respectively). Use VST and VSB to monitor the actual full scale input voltages (±2 V) by adjusting VFT and VFB. These adjustments have some interaction; repeat a few times as needed until VST and VSB settle at the desired voltages. Do not drive VRM as is commonly done with a standard flash ADC converter. When not being used (VST, VRM & VSB), decouple with a 0.01 μF chip capacitor (surface mounted) to AGND from each tap to minimize high frequency noise injection.

Referring to figure 17, U2 is the + 2.5 V reference with ±150 mV of adjustable range (R1 potentiometer). U3 (OP--07) is an inverting amplifier. Its tolerance is 5% with ±300 mV of adjustable range (R2 potentiometer). Fairchild recom-

mends that these references (VFT & VFB) be operated to within ± 2% (or ± 2.5 V ± 50 mV) to maintain accuracy within the specified limit. Before each EB7820/24 board is shipped, the references are adjusted for VFT and VFB of ±2.5 V ±5 mV respectively. For each new SPT7820 or SPT7824, VST and VSB need to be readjusted. All measurement must be referenced to AGND test point (provided).

REFERENCE MONITORING

Table 2 - Recommended Operating Voltage Range

Ref	Monitoring Point	Min	Typ	Max	Adjust
VST	U1, PIN 20	+1.95 V	+2.00 V	+2.05 V	R1
VSB	U1, PIN 23	- 2.05 V	- 2.00 V	- 1.95 V	R2

Note that the SPT7820 and SPT7824 (especially reference taps VFT VFB, VST and VRM) are sensitive to electrostatic discharge (ESD).

Figure 4A shows one type of reference driver. Figure 4B is another way to drive the reference circuits using force and sense. The alternate circuit provides better control of plus full scale (+FS) and minus full scale (-FS) errors by sensing VST and VSB to ± 2.0 V respectively. However, the reference pins VST and VSB are not low impedance nodes that require additional precaution when routing (PCB layout).

Figure 4A - Reference Driver

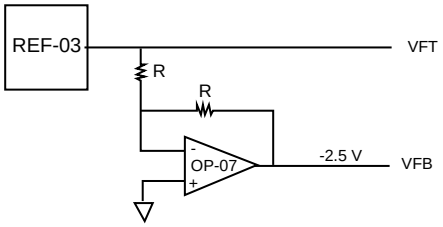
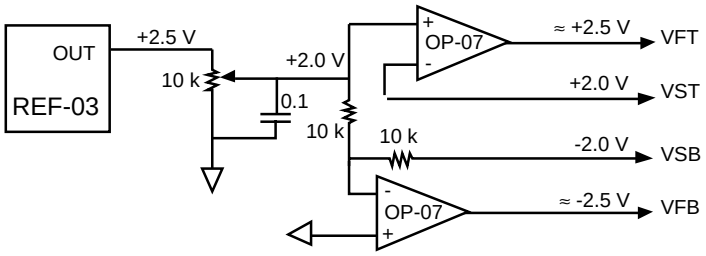


Figure 4B - Alternative Reference Driver



SPT7820 OR SPT7824, 10-BIT ADC

The SPT7820 integrated circuit is a 10-bit analog-to-digital converter capable of digitizing an input signal with a minimum update rate of 20 mega-samples per second (MSPS). The SPT7824, on the other hand is pin compatible with the SPT7820 except that it is faster: 40 MSPS for the sampling frequency. On both devices, the expected full scale analog input range is from VST to VSB. The analog input is latched at the leading edge of the CLK. There are 11 digital TTL outputs. D0 - D9 are the parallel TTL-output bits, with D0 the LSB, D9 the MSB and D10 the overrange bit. The data outputs are latched at the rising edge of the CLK, with a propagation delay of typically 14 nsec. There is one clock latency between CLK and valid output data (see figure 5 for more detail). The output code is a straight binary:

Table 3: SPT7820/24 Output Coding

(Ø Indicates the Flickering Bit Between Logic 0 and 1)

Analog Input	D12 (Overrange Bit)	Data Output Code
<- 2.0 V	0	00 0000 0000
- 2.0 V +1 LSB	0	00 0000 000Ø
0 V	0	ØØ ØØØØ ØØØØ
+ 2.0 V - 1 LSB	0	11 1111 111Ø
> + 2.0 V + 1/2 LSB	1	11 1111 1111

Pin 21 is the analog input pin. Selecting the analog input driver for the SPT7820/24 is less of an issue than with most Flash ADCs because the input impedance and input capacitance are typically 300 kΩ and 5 pF, respectively. For example, at 10 MHz and 4 V_{P-P} sinewave input, the input driver source only requires 0.648 mA of peak output current (4 πFC).

The analog input is directly fed from a BNC (VIN). R10 (51 Ω), analog input source termination is mounted on a socket as a user-selectable termination. The analog input pin has no circuit protection. Its maximum rating is from VFT to VFB (±2.5 V). In an application in which the analog input range is greater than ±2.5 V, protect the input pin from permanent damage with a voltage limiter.

INPUT CLOCK DRIVER

CLK is the single-ended input clock to the EB7820/24 (evaluation board), CLK IN is the input clock to the SPT7820 or SPT7824, and CCLK is the capture clock used for the output latches (U7 & U8).

The clock input of the SPT7820/24 requires a TTL-logic level of 6 nsec or faster to improve the noise. TTL-logic family (74FXX) is good for driving the SPT7820/24. Finding a TTL-square wave generator up to 40 MHz with fast slew rate and low jitter is harder than a sine wave, low jitter generator. U5 (MAX9686, TTL-voltage comparator) provides most of the above requirements to drive the SPT7820 or SPT7824 (except the low jitter generator). The CLK signal can be a sine wave signal with the amplitude not to exceed ± 3 V (input common mode limitation of U5). R11 (51 Ω) is the CLK source termination. Use R3 to adjust the duty cycle of the CLK IN. CLK IN is in phase with CLK and has a a propagation delay of 6 nsec typically. The positive clock (CLK IN) pulse width must be kept between 10 nsec and 300 nsec for the

SPT7824 and 20 to 300 nsec for SPT7820. This is due to the internal THA. When operating the SPT7820 or SPT7824 faster than 3 MSPS, keep the clock duty cycle at approximately 50% ±10%. The probe jack PJ1 is the monitoring test point for the CLK IN. Use this test point when adjusting the clock duty cycle.

Logic low of the CLK IN (pin 17) causes the internal THA to go into track. It is necessary to keep the SPT7820 or SPT7824 in the track mode when the device is idle for an extended period of time or at the start-up time. This setup will prevent the internal THA from going to saturation due to the internal THA's droop. EB7820/24 provides a logic low to the clock of the SPT7820/24 when the pulse generator (CLK) is removed from the evaluation board.

TTL-OUTPUT DATA LATCHES

The rise time (Trise) and fall time (Tfall) of SPT7820/24 (D0-D9) are not symmetrical. The propagation delay with respect to trise (at the 2.4 V crossing) is typically 14 nsec and 6 nsec is typical with respect to tfall (at the 2.4 V crossing). Figure 5 shows the actual output characteristic of the SPT7820/24. This nonsymmetrical trise and tfall creates approximately 8 nsec of invalid data.

In an application where a reconstruction DAC is needed, the above invalid data zone will cause the reconstruction signal to have an unwanted heavy glitch if the DAC is directly interfaced with SPT7820 or SPT7824. To avoid this, buffer the SPT7820/24 by the edge-triggered latches. FAST family TTL logic will fit well in this application due to its fast setup and hold time.

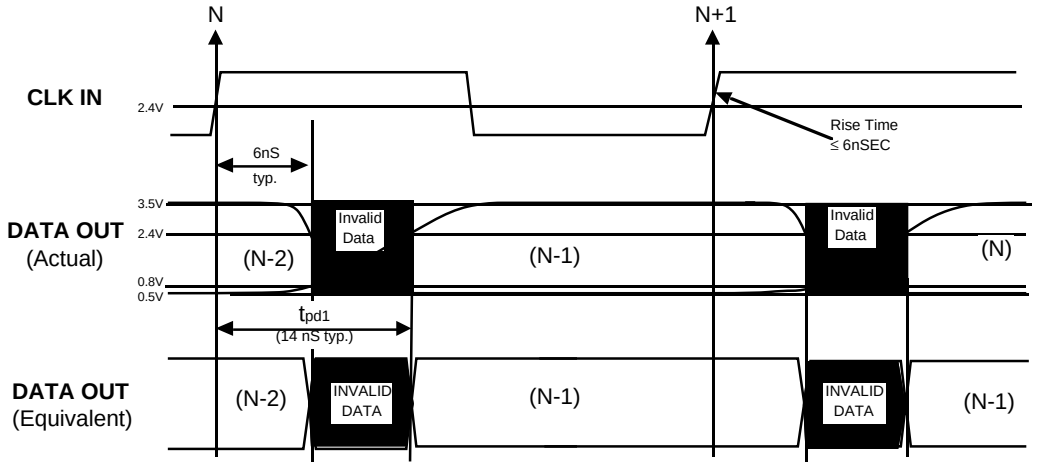
U7 and U8 (74F174) are the output latches. The FAST family TTL-logic is very sensitive to electrostatic discharge (ESD). RN1 and RN2 are the 8 pin SIP resistor networks, 10 kΩ. They protect U7 and U8 by providing the ESD path to DGND. The BNC connector (CCLK) is the capture clock, which has 51 Ω termination R12 on board. The outputs of the data latches (D0-D9) are routed through the standard 26-pin female ribbon connector (P2). SJ3-5 are the solder jumper options for the capture clock. Only one of these jumpers needs to be connected:

- When SJ3 is installed (factory installed when this board is shipped), SPT7820/24 and the latches (U7 and U8) are clocked at the same time. With this configuration, the data seen at the connector P2 adds another clock of latency (two clocks of latency total as shown in figure 6).

- When SJ4 is installed, the capture clock must be supplied externally through CCLK. The setup time (ts) and hold time (th) in table 5 must be met when selecting this option.

- When SJ5 is selected, the buffers will be latched at the falling edge of the CLK IN (SPT7820/24). With this option, the setup time (ts) and hold time requirements for the 74F174 latches must be met (table 5). The placement of this capture clock edge is dependent on the clock pulse width and the sampling frequency. This option is not recommended above 25 MSPS to avoid latching the invalid data.

Figure 5 - Digital Output Characteristic of the SPT7820 or SPT7824



The digital outputs (latched) are routed through P2, 26 pin ribbon connector. (See table 4.)
The overrange bit (D10) could be viewed through test point TP13. D10 does not bring out through P2.

Figure 6 - EB7820/24 Timing Diagram Where CCLK is the Same as CLK IN

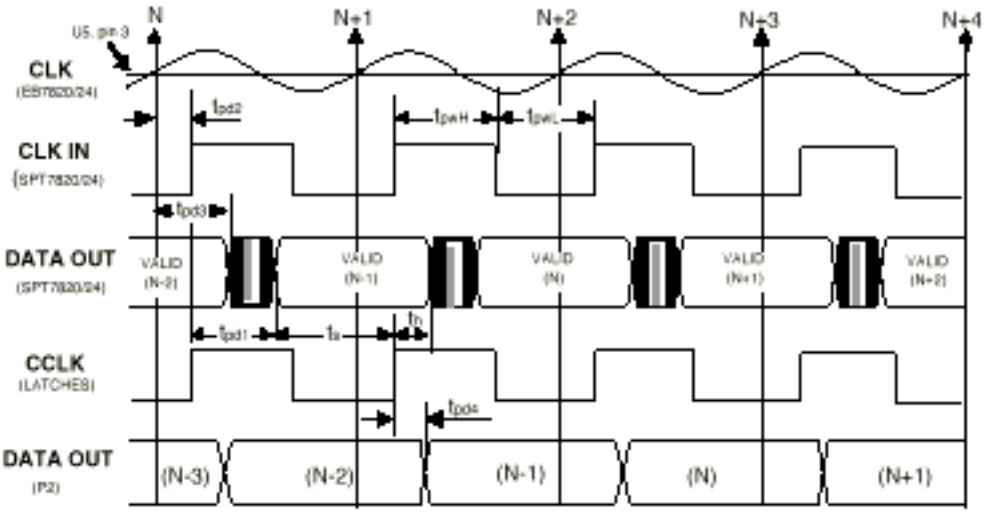


Figure 7 - EB7820/24 Timing Diagram Where CCLK is 180° Out of Phase From CLK IN

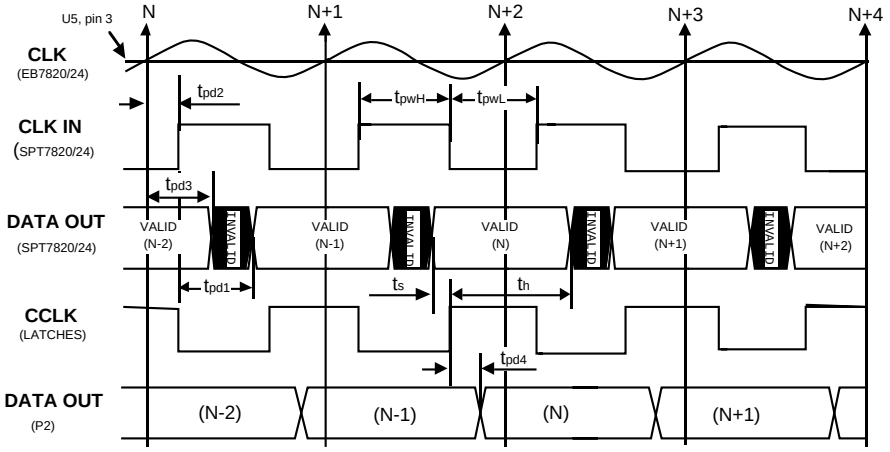


Table 4 - P2, SPT7820/24 Output Data (Latched) , 26-Pin Female Ribbon Connector

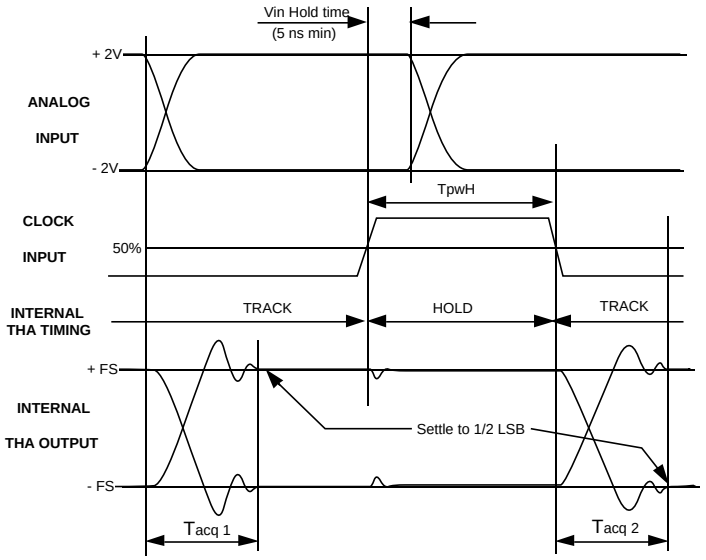
P2	Function	Logic	P2	Function	Logic
1	CCLK	TTL	2	DGND	DGND
3	N/A	TTL/LO	4	DGND	DGND
5	N/A	TTL/LO	6	DGND	DGND
7	D0 (LSB)	TTL	8	DGND	DGND
9	D1	TTL	10	DGND	DGND
11	D2	TTL	12	DGND	DGND
13	D3	TTL	14	DGND	DGND
15	D4	TTL	16	DGND	DGND
17	D5	TTL	18	DGND	DGND
19	D6	TTL	20	DGND	DGND
21	D7	TTL	22	DGND	DGND
23	D8	TTL	24	DGND	DGND
25	D9 (MSB)	TTL	26	DGND	DGND

Table 5: Timing Specification

Function	Description	Min	Typ	Max	Unit
tpd1	SPT7820/24, CLK to Data Valid Prop Delay	-	14	18	nsec
tdp2	MAX9686 Prop. Delay	-	6	9	nsec
tdp3	SPT7820/24, T(fall) Prop. Delay	4.5	7	10	nsec
tdp4	74F174, Prop. Delay	4.5	7	10	nsec
ts	74F174 Setup Time	4	-	-	nsec
th	74174, Hold Time	4	-	-	nsec
tpwH	CLK Positive Pulse Width (SPT7820)	20	-	300	nsec
tpwL	CLK Negative Pulse Width (SPT7820)	20	-	-	nsec
tpwH	CLK Positive Pulse width (SPT7824)	10	-	300	nsec
tpwL	CLK Negative pulse Width (SPT7824)	10	-	-	nsec

SPT7820/24 ACQUISITION TIME SPECIFICATION

Figure 8: Acquisition Time



The acquisition time (Tacq) is defined as the hold to track full scale settling time for the internal track-and-hold (THA). Logic low of the clock input corresponds to track mode and logic high is the hold mode for the internal THA. Figure 8 shows two types of acquisition time:

1) Tacq 1 is the settling time of the THA when it is in track and it is driven by the analog input switching.

2) Tacq 2 is the amount of time it takes for the internal THA of the ADC to reacquire the analog input when switching from hold to track (CLK IN from high to low) to within 1/2 LSB.

Both Tacq 1 and Tacq 2 need the same amount of time (see the acquisition time specification in the respective data sheet).

The low-to-high clock transition should be placed after both the analog input and internal THA are settled. The analog input must remain for at least 5 ns (Vin hold time) after the low to high clock transition. Keep the clock positive pulse width (TpwH) to within the recommended limit. (Refer to the specification in the respective data sheet.)

TIMING CONSIDERATIONS WHEN USING AN EXTERNAL TRACK-AND-HOLD

The signal-to-noise ratio (SNR) and the total harmonic distortion (THD) degrade as the analog input frequency increases. These parameters imply that the differential linearity error (DLE) and the integral linearity error (ILE) degrades as well at high frequency. This degradation is mainly due to aperture jitter and/or analog input bandwidth limitation and/or slew rate limitation of the SPT7820 and SPT7824. Below 1 MHz, the SNR and THD of the SPT7820 and SPT7824 are generally constant. In order to bring these accuracies up (at high frequency), you may need to buffer the analog input using a track-and-hold amplifier (THA). THAs can be imperfect (especially at high frequency); otherwise, the dynamic performance of the SPT7820 or SPT7824 would be constant and equal to its performance at 1 MHz.

Selecting an acceptable THA for a specific application is sometimes difficult. The timing diagram shown in figure 9 and table 6 illustrate the critical timing necessary when driving the ADC from a THA.

Figure 9-Critical Timing Between External THA and ADC

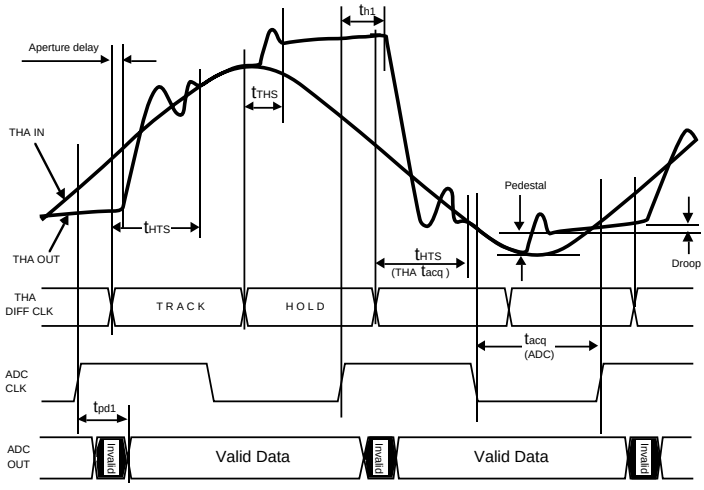


Table 6 : Critical Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
tHTS	THA, Hold to Track Settling Time	X	X	X	
tTHS	THA, Track to Hold Settling Time	X	X	X	
tacq	SPT7820 ADC Acquisition Time 4 V Step		20		nsec
tacq	SPT7824 ADC Acquisition Time 4 V Step		12		nsec
th1	Hold Time After the ADC Rising Clock	5			nsec

X= This Limit Depends on the THA Chosen

The settling time to 1/2 LSB (1.953 mV) is one of the principal requirement in a 10-bit THA. This includes both track to hold (tTHS) and hold-to-track (tHTS) settling time. tHTS varies with the step size (voltages) that the THA needs to swing. The rising edge of the ADC's clock should be placed after tTHS has settled. SPT7820/24 requires that the analog input be held for an additional 5 nsec minimum (th1) after the rising edge of the clock. Figure 9 shows the ADC running at Nyquist; the sampling frequency is practically twice the input frequency. In this example, the ADC could have as much as a 4 Volt step (±FS) from one conversion to the next. The acquisition time (tacq) of the ADC must be met. This is the time necessary to allow the internal THA of the SPT7820/24 to track (CLK= low) and settle to 1/2 LSB while the input is sharply changed to its new continuous level. The minimum acquisition time is 20 nsec for a 4 volt step and 12 nsec for a 0.5 volt or less step.

The maximum sampling rate of the SPT7820 or SPT7824 when driving from an external THA can be decided from the proper combination of tTHS, tHTS and tacq .

The pedestal and the droop of the THA shown in figure 9 are not critical to the dynamic performance as long as they are constant with respect to the analog input range. They are seen as offset errors.

LOW LEVEL ANALOG INPUT SIGNAL

SPT7820 and SPT7824 require that the analog input (VIN) range be operated within ± 2 V ± 2%. Amplification and level shifting are needed for a low voltage level VIN.

Figure 10: Driving Circuit Block Diagram

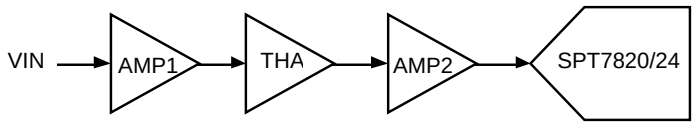


Figure 10 shows the typical analog driving circuit. AMP1 and/or AMP2 are optional. For an application in which noise is the major concern, use AMP1 (disregard AMP2) low noise amplifier to gain up to ± 2 volts before getting to the THA. In another application in which high frequency VIN is the major concern, use AMP2 instead of AMP1 to amplify the THA signal to ±2 volts before reaching to SPT7820 or SPT7824. In the latter case, the low level VIN provides a faster acquisition time for the THA.

UNCOMMITTED PROTO SOCKET SPACE

Referring to the detail schematic figure 17, there are two slots available for applications where additional circuits may be needed to interface with the EB7820/24. These two slots (labeled A and D in the PCB assembly) are electrically noncommitted:

- Slot A is physically located near VIN (BNC) and is intended for the analog interfacing circuit. It has one 16-DIP and one 8-SIP.
- Slot D is physically located between P2 and P3 connectors and is intended for the digital interfacing circuit. It has three 16-DIPs, three 8-SIPs and one 37-pin D connector.

  Both slots have the appropriate power supplies and grounds in their vicinity as labeled.

DB792 DAUGHTER BOARD (RECONSTRUCTION DAC)

DB792 (figure 18) is the daughter board that interfaces directly to the EB7820/24 via P2 and P3. It is suited for an application where the reconstruction DAC is needed to evaluate the ADC performance in the time domain. DB792 is designed around the Analog Device's AD9713, 12-bit TTL, digital-to-analog converter, 80 MSPS update rate. It is setup in bipolar operation. The detailed schematic is shown in figure 18. Refer to Analog Device's AD9713B data sheet for detail.

SPT7820/24 INPUT AND LATCH-UP PROTECTIONS

The SPT7820/24 is free from any possible latch-up when the recommended interfacing circuit as shown in figure 11 is followed. The following lists are for both latch-up and input protection interface requirements:

1) Drive the input clock (pin 15) from a TTL logic (VIH ≤ 4.5 V). Fast TTL logic family or equivalent is strongly recommended due to its fast rise time (6 nsec or faster). In the event in which the clock is driven from a high current source (greater than 400 mA), use a 100 Ω resistor in series to current limit to roughly 45 mA.
2) D1 is a Schottkey or hot carrier diode (Motorola, 1N5817 or eq.) installed between VEE and AGND (reverse bias).
3) Both VCC (pin 18 & 25) and DVCC (pin 14 and 28) are driven from the same analog +5 V supply.
4) Mount the ferrite beads (FB1 and FB2) as closely to the device as possible. The bead to ADC connections should not be shared with any other device.

Figure 11: Recommended Interfacing Circuit

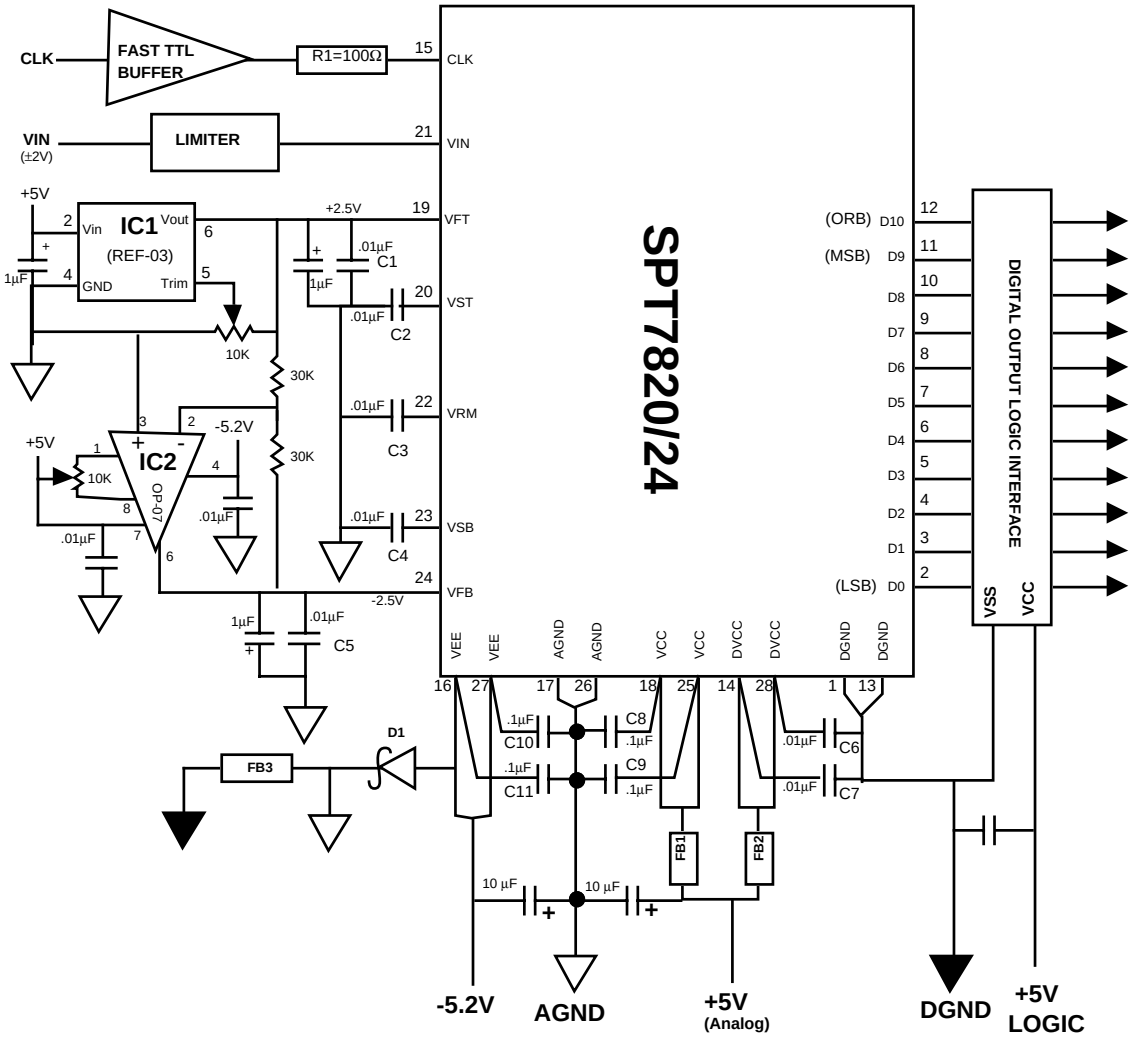
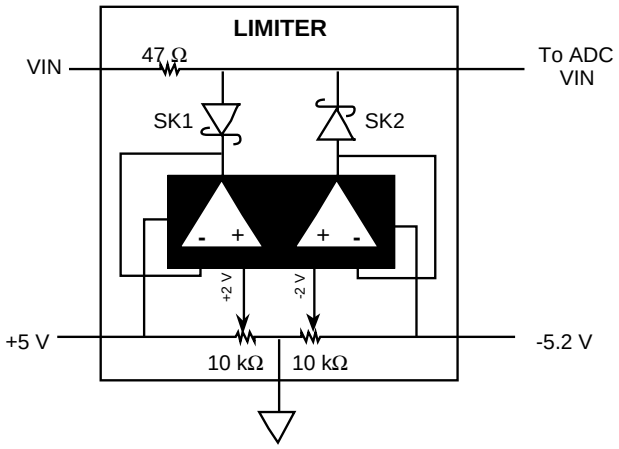


Figure 12 : An Example of an Input Limiter

5) Bypass all reference and power supply pinsas closely to the device pin as possible (chip caps C1-11 are preferred): 0.1 µF for VCC and VEE, and 0.01µF for DVCC and Vref.

6 The top reference (VFT) driver must be current limited to 20 mA maximum if a different reference driver circuit is used in place of the recommended circuit shown in figure 11.

7) The limiter is required if the maximum peak-to-peak voltage of the analog input exceeds ±2.5 V. Incorporate the limiter within the analog input driver or use the circuit shown in figure 12. Another option is to add a 100 Ω resistor in series to current limited the input. This last option adds another LSB error to both ± full scale compared to only 1/2 LSB when using the circuit shown in figure 12.



SK1,2 = Fast recovery Schottkey diode:
RCA, P/N SK9091 or equivalent

SPT7820/24 CHARACTERIZATION

Performance at speed is the main goal in evaluating any ADC, but it is beneficial to start from a relatively low speed and verify key parameters. It is also beneficial to predict performance at speed. If the transition noise and/or the differential linearity of the device perform poorly at low frequency, the SNR at speed cannot be expected to be better. In addition, the low frequency setup can be useful as a verification tool for the test set-up.

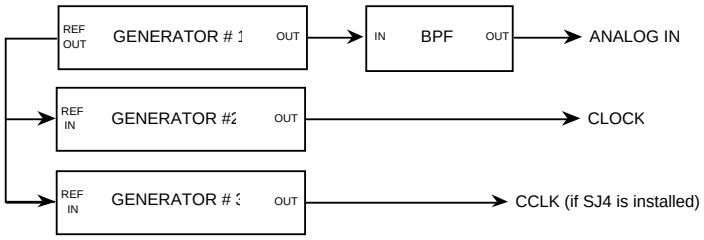
At low frequency there are numerous ways of characterizing the differential linearity error (DLE), integral linearity error (ILE), transition noise, missing codes (MC), synchronous noise, nonmonotonicity, power supply sensitivity and power supply currents. Fairchild will guide the user through two classical yet powerful testing approaches to achieve fast and relatively accurate results.

High frequency or dynamic testing, the missing codes test, ILE, DLE, VOS and the gain error tests are based on statistical results. They can be performed using the *histogram* technique. SNR and THD are tested by using the fast Fourier transform (FFT).

EB7820/24 was designed to provide optimum capability in fulfilling the above characterization needs.

EQUIPMENT HOOKUP

Figure 13: Synchronous Equipment Hookup



Coherent testing is recommended in characterizing the SPT7820/24. All three signals (VIN, CLK and CCLK) are synchronized. This testing gives well defined results when using the following suggested techniques for evaluating the performance of the device. These techniques also significantly reduce the testing time, especially the dynamic testing. The diagram in figure 13 suggests one way to achieve this goal. Generator 1 is the analog input. Generator 2 is the sampling clock, sinewave and ±3 V_{P-P} maximum. Generator 3 (only needed if solder jumper option SJ4 is used) is the capture clock, TTL. A phase adjustment option for generator 3 is necessary to place the edge of the capture clock at the proper setup time. R11 and R12 are 51 Ω and serve as termination resistors for generator 2 and generator 3, respectively.

SELECTION OF THE SIGNAL GENERATORS

For very high speed and high accuracy ADC testing, selection of both analog and clock inputs is critical. Two parameters are important in selecting the generators 1 and 2:

1) The purity of the output sinewave must be at least 76 dB or better of SNR. An appropriate band pass filter (BPF) installed after the generator will help improve the SNR.

2) The sampling clock jitter or aperture jitter can originate both inside and outside the A/D converter.

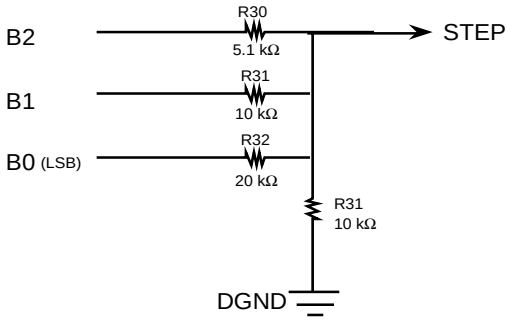
Consider the selection of an acceptable clock generator. The uncertainty of the clock placement due to the time jitter (aperture jitter) degrades the effective performance of the device. This jitter is translated into the ADC amplitude error and is proportional to the analog input slew rate. For a sinusoidal input, the uncertainty of the clock edge placement from cycle to cycle due to the equipment jitter has an effect on the A/D converter performance, especially the SNR:

SNR (Max) = {20 LOG [1/ (2π Fin Tj)] + 3.02 } dB,
Where : Fin = analog input frequency
and and Tj = the aperture jitter in RMS

Fairchild uses the following equipment when characterizing/testing the SNR and THD: HP8644A synthesized signal generator for both generators 1 and 2 and HP3325 function generator for generator 3.

LOW FREQUENCY PERFORMANCE CHECK

Figure 14 : Three-Bit Reconstruction DAC



This section describes one approach to visual evaluation of the differential linearity error (DLE), missing codes (MC), non-monotonicity, synchronous noise and transition noise. The BNC DAC OUT (from the mother board, figure 18) can be the monitoring point to view the quality of the quantization signal, but this may pose a great deal of difficulty. Fairchild suggests another approach commonly used in the industry.

This approach is to use a three-bit reconstruction DAC generated from LSB's TTL outputs of the last three LSBs. This circuit is shown in figure 17. When jumpers SJ9-SJ11 are installed, R30-R33 forms a three-bit DAC as shown in figure 14.

The output of this three bit reconstruction DAC can be viewed through the test point STEP with the scope. For this test, use a function generator for the generators 1 and 2 (HP3325A or equivalent) and set up for a ramp output. Replace the BPF with an RC low pass filter (1k and 0.01 µF) to eliminate all high frequency components. Set the slew rate of this ramp signal to 1 LSB per n conversions (sampling period) for a desired (1/n) test resolution. A minimum of n = 10 is recommended for this application. The P-P voltage and the period of the ramp input are then dependent on the selection of the number of steps (LSBs) within one ramp's period. You may need to remove R10 (51 Ω). Set CLK and CCLK to the same relatively low frequency, approximately 1 MHz or even slower. Adjust as needed to meet the tpwH and ts specifications. (See figure 5-6 and table 5.)

The following formulas summarize the criteria for selecting the analog ramp input signal:

The ramp peak-to-peak voltage:

Vp-p = m(FSR/1024)

The ramp period: T = (m) (n) / Fs Where:

m =	desired number of steps (LSBs) per ramp's period
Fs =	sampling frequency
FSR =	full scale range (typically SPT7820/24's FSR is 4 V)
n =	desired test resolution or the number of conversions/LSB

Figure 15 shows the relationship between the analog input ramp signal and the resulting three-bit reconstruction DAC. It shows 16 LSBs of P-P input voltage (i.e., two 8-level steps) per period. For an ideal ADC and an ideal ramp input, its digital output code changes state by 1 LSB every (n)th conversion (dash line in the transfer curve). Any error in the ADC makes the corresponding output codes change state before or after the (n)th conversion. This error will translate into smaller or larger respective step width. The DLE can be judged visually by comparing the actual step size with respect to the ideal step with ±(1/n) LSB of accuracy. In this case, the ideal step is the average of the step size. Other errors (MC, transition noise and nonmonotonicity) can be resolved in a similar way. Figure 15 also gives the identification of each error from the actual transfer curve.

Example:

1) SPT7820 is operated at 500 kHz (sampling frequency).
2) (1/10) of the test resolution is desired.
3) The scope is externally triggered to the ramp input. Three retraces of 8-level steps (or 24 total steps) per ramp's period are selected.

What peak-to-peak voltage (V p-p) and period (T) of the ramp input signal are required to drive the SPT7820?

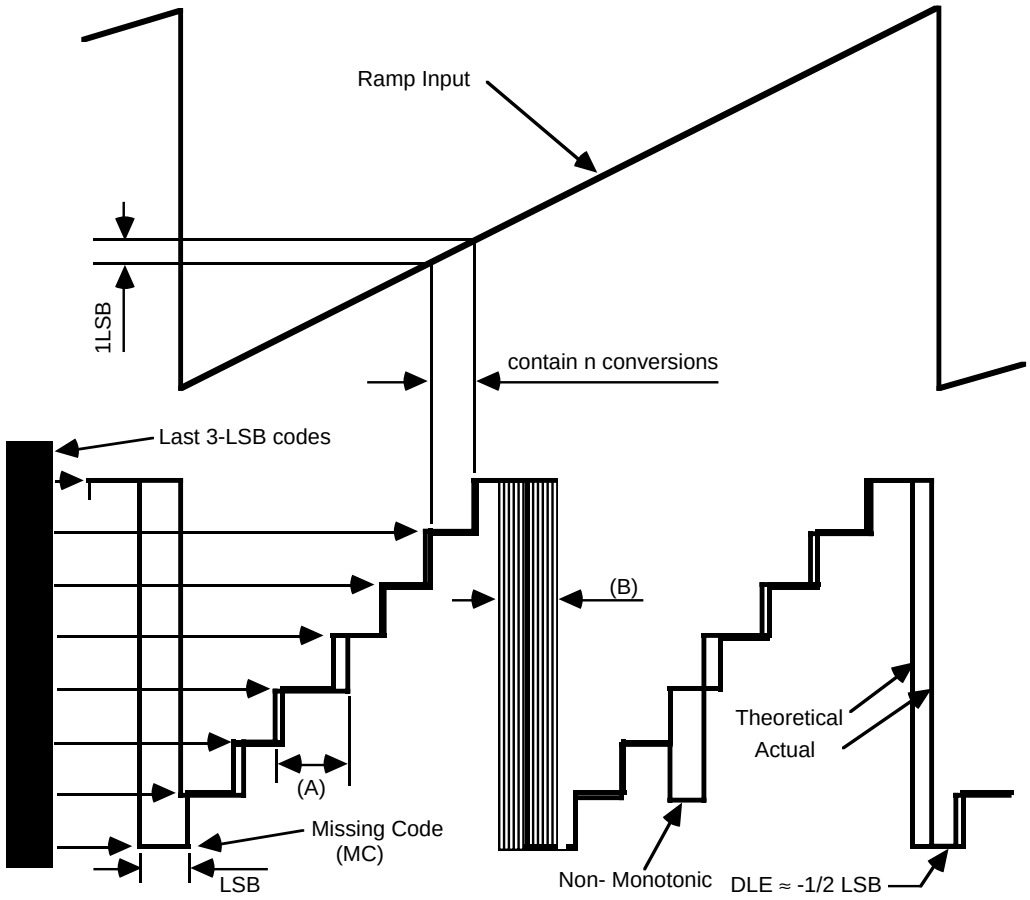
Answer:

1) Fs = 500 kHz,
2) n = 10 ,
3) m = 24, then V(p-p) = m (FSR / 1024) = 24(4 /1024) = 94 mV
   and T = (m) (n) / Fs = (24) (10) / 5000,000 = 480 µsec

Note that the above input signal will only cover 24 parts in 1024 of the FSR. To identify all errors through the full scale range, slowly sweep the ramp input from -FS to +FS and observe the output steps for the MC, transition noise, DLE and non-monotonicity as indicated in the transfer curve (figure 15). Most generators do not have the DC offset covering the range from +2.5 V to -2.5 V. You may need to construct an additional circuit using the classical summing amplifier to DC offset the above ramp input signal.

The synchronous noise in an ADC is the distortion of the performance of the device when the sampling frequency varies. (Normally, the DLE can be clearly observed.) This is usually caused by the digital signals being coupled back, internally into the analog input signal. This problem is very common for ADCs using the successive approximation register (SAR) architecture. The ADC that possesses this kind of symptom presents some weak performances at a specific sampling frequency (within the specified sampling rate), but shows better results when the sampling frequency is varied up or down from that weak spot. To verify the synchronous noise using this set-up, slowly change the sampling frequency and observe the transfer curve, especially the changes in DLE.

Figure 15: Three-Bit Reconstruction DAC Waveform Using Analog Input Ramp



(A) is the actual bit weight for the output code multiple of 011
(B) is the major transition noise. This noise level shown is greater than ± 1/2 LSB

Advantages:

1) Many tests (as stated above) can be extracted from this one, simple test set-up.

2) The missing code and the transition noise can be more accurately identified than with any other standard test methods.

3) Set-up is quick and relatively accurate.

Disadvantages:

1) The accuracy depends on human judgement and can be very difficult if the person is not familiar with it.

2) The exact code is not shown in the transfer curve, but in a multiple of the last three bits of the LSB. To overcome this problem, probe every bit using an oscilloscope or install LEDs at each output (P3 connector) to signal the state of each output bit.

DYNAMIC TESTING

Figure 16: Dynamic Testing Test Set-up

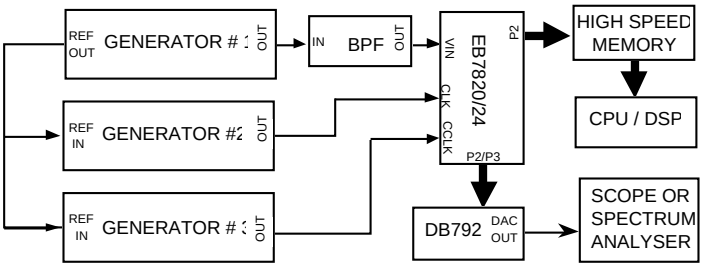


Figure 16 is the recommended block diagram for dynamic testing of the SPT7820 or SPT7824 using the EB7820/24 evaluation board. In earlier tests, the DAC OUT signal was used to analyze the ADC's dynamic performances (SNR and THD) through a spectrum analyzer. This method of testing presented some uncertainties. The DAC had to be near perfect and free from glitches, and its dynamic accuracy (DLE and ILE) had to be far better than the ADC under test. Any errors in the DAC wereadded to the total SNR and/or THD.

Today, it is preferable to perform these tests by means of digital signal processing (DSP). There are currently numerous standard software packages on the market to service this application. The EB7820/24 provides the data outputs through P2. (See table 5 for detail.) The reconstruction DAC can be obtained from DB792 daughter board. Both set-ups are very important in characterizing the dynamic performance of the SPT7820 or SPT7824.

In many cases, the speed of the capture memory is much slower than the available output valid data of the ADC under test. In this case, it is necessary to decimate the capture clock at a rate of Fs/N, where N is a power of 2. The beat frequency can be achieved by slightly changing the analog input frequency by an amount of Δfin. For a 4096-point FFT, the beat frequency of Δfin = Fc/4096 is added (or subtracted) to the analog input frequency. 4096 data points are filled in one test period where the input is at Fin $\pm$ (Fc/4096) and the output is updated at 1/Fc interval. Select Fin as the multiple (integer) of Fc to achieve a complete system synchronization. Both capture memory and the DAC run at a relatively low update rate (Fs/N).

The daughter board, DB972, is capable of updating to 80 MSPS.

EB7820/24 CALIBRATION

This section is a guide for the DC calibration of the EB7820/24 if needed. Note that this board was fully calibrated before shipment. VST and VSB voltages require new calibration on each new SPT7820 or 7824.

Check for installation of jumpers SJ2B, SJ2C and SJ3.

1.0 Equipment Needed
1.1 Four DC power supplies: analog +5 V, analog -5.2 V, digital +5 V and digital -5.2 V.
1.2 One Hewlett Packard, HP3325A, function generator or equivalent.
1.3 One DVM with 5 and 1/2 digit precision.
1.4 One Oscilloscope.

2.0 Equipment Set-Up / Hook-Up
2.1 Ensure that socket U1 does not haveSPT7820 or SPT7824 in it.
2.2 Connect all four power supplies as shown in table 1, and figures 2 and figure 3.
2.3 Connect the function generator to CLK BNC.
2.4 Set the CLK to 3 MHz, sine wave , $\pm$2 V.
2.5 Connect VIN to AGND.

3.0 References Calibration
3.1 Monitor TP1 with respect to AGND test point with DVM.
3.2 Adjust R1 for +2.500 V at TP1.
3.3 Monitor TP2 with respect to AGND test point with DVM.
3.4 Adjust R2 for -2.500 V at TP2.
3.5 Turn all power to off.
3.6 Install SPT7820 or SPT7824 into U1 socket. (Fepeat from this procedure for all new devices.)
3.7 Turn all power back to on.
3.8 Monitor U1, pin 22 (VST) with respect to AGND test point with DVM.
3.9 Adjust R1 for +2.000 V at VST.
3.10 Monitor U1, pin 27 (VSB) with respect to AGND test point with DVM.
3.11 Adjust R2 for -2.000 V at VSB.
3.12 Repeat the procedure from paragraph 3.8 until VST and VSB reach the desired voltages ($\pm$2.000 V respectively).

4.0 Clock Circuit Calibration
4.1 Monitor PJ1 with scope on channel 1 (externally sync to the generator).
4.2 Observe the TTL clock and adjust R3 for approximately 50% of duty cycle.

5.0 Latches (U7 and U8) Test
5.1 Remove R10.
5.2 Connect VIN to TP1.
5.3 Monitor P2, odd number pins (7-25), with scope and observe TTL-logic high on all pins.
5.4 Connect VIN to TP2 .
5.5 Monitor P2, odd number pins (7-25), with scope and observe TTL logic low on all pins.

End of calibration Procedure

EB7820/24 PARTS LIST, Rev B

#	Ref. Des.	Description	Vendor Part Number	Qty
1	C1-7,10	Capacitor, Tant., 10 µF, 25V, .10"	Sprague/199D106X0025B A1, or eq.	8
2	C20,22-28,30-32	Capacitor, 0.01 µF, Chip	Sprague/11C1206X7R103J050AB, or eq.	11
3	C21,29	Capacitor, 0.1 µF, Chip	Sprague/11C1206X7R104J050AB, or eq.	2
4	C50-58	Capacitor, 0.01 µF, 10%, Ceramic	MURATA/RPE110X7R103K050V or eq.	9
5	D1	Lead Mounted Hot Carrier Rectifier	MOT/IN5817, or eq.	1
6	FB1-3	Ferrite Bead, Lead Mounted	Fair Rite/2743001111	3
7	P2,3	Ribbon Plug Connector	T & B Ansley/622-2627, or eq.	2
8	P1	Power Connector, 9 Pins	Molex/09-18-5094, or eq.	1
9	P1/Recept	Power Connector, 9 Pins, Recept	Molex/03-09-1093, or eq	1
10	PJ1-2	Probe Connector (25 sets/bag)	Tektronix /131-4353-00	2
11	R3	Potentiometer, 2k , 12 Turns	Bourns/44F3531, or eq.	1
12	R1,2	Potentiometer, 10k , 12 Turns	Bourns/44F3533, or eq.	2
13	R10-12	Resistor, 51 Ω, 5%, 1/8 W	Allen-Bradley/BB-510-5, or eq.	3
14	R20,21	Resistor, 820 Ω, 5%, 1/8 W	Allen-Bradley/BB-821-5, or eq.	2
15	R26,27,30	Resistor, 20 kΩ, 5%, 1/8 W	Allen-Bradley/BB-203-5, or eq.	3
16	R28	Resistor, 1 MΩ, 5%, 1/8 W	Allen-Bradley/BB-105-5, or eq.	1
17	R32	Resistor, 5.1 kΩ, 5%, 1/8 W	Allen-Bradley/BB-512-5, or eq	1
18	R33	Resistor, 10 kΩ, 5%, 1/8 W	Allen-Bradley/BB-103-5, or eq.	1
19	RN1,2	8 pin SIP Resistor, 10K, 708A Type	Newark stock 81F9599, or eq.	2
20	TP1-3,AG,DG,STEP	Test Point Terminal. 76 Mil Hole Dia	Cambion/160-2044—02-01-00, or eq.	6
21	U1	Device Under Test, 10 Bit ADC	SPT7820 or SPT7824	1
22	U2	+2.5 V Precision Voltage Reference	PMI/REF-03GP, or eq.	1
23	U3	OP-AMP, Low Noise	PMI/ OP-07EP	1
24	U5	Single, Fast TTL comparator, 8 DIP	MAXIM/MAX9686CPA	1
25	U7,8	HEX D Flip-Flop, TTL, Fast Series	Fairchild/74F174, or eq.	2
26	N/A	BNC Connector, Receptacle	Amphenol/31-5329, or eq.	3
27	N/A	28-Pin DIP Socket, .600" (U1)	AMP/M528-611D, or eq.	1
28	N/A	SIP Socket Strip, 20, Break-Away	Adv. Intercon./SS-020-51-TG 1, or eq.	1
29	N/A	Nylon Standoff, 1", Round	Plastic Component Corp/C34005, or eq.	4
30	N/A	Nylon Screw, 4-40, 3/16", Round Head	Plastic Component Corp/S120040, or eq.	4
31	N/A	Crimp Male Terminal for P3	Molex, 02-09-2103	1
32	N/A	Crimp Female Terminal for P3	Molex, 02-09-1104	8
33	EB7820/24,PCB	Printed Circuit Board	Fairchild/ EB7820/24 Drawing, Rev: B	1

DB792 PARTS LIST, Rev A

#	Ref. Des.	Description	Vendor Part Number	Qty
1	C1-2	Capacitor, Tant., 10 µF, 25 V, .10"	Sprague/199D106X0025B A 1, or eq.	2
2	C10-16	Capacitor, 0.01 µF, Chip	Sprague/11C1206X7R103J050AB, or eq.	7
3	C21-25	Capacitor, 0.1 µF, 10%, Ceramic	MURATA/RPE110X7R104K050V or eq.	5
4	D1	2 Terminal IC, 1.2 V Reference	Maxim/ ICL8069CCSQ2, or eq.	1
5	P2,3	26 Pin Dual Row Vert PCB Mount Conn	Molex 15-44-3213, or eq.	2
6	R1	Potentiometer, 10k , 12 Turns	Bourns/44F3533, or eq.	1
7	R2	Resistor, 7.5 kΩ, 5%, 1/8 W	Allen-Bradley/BB-752-5, or eq.	1
8	R3	Resistor, 22 Ω, 5%, 1/8 W	Allen-Bradley/BB-220-5, or eq.	1
9	R4	Resistor, 10 kΩ, 5%, 1/8 W	Allen-Bradley/BB-103-5, or eq.	1
10	R5	Resistor, 15 kΩ, 5%, 1/8 W	Allen-Bradley/BB-153-5, or eq.	1
11	R6	Resistor, 20 kΩ, 5%, 1/8 W	Allen-Bradley/BB-203-5, or eq.	1
12	R7	Resistor, 1kΩ, 5%, 1/8 W	Allen-Bradley/BB-102-5, or eq.	1
13	R8	Resistor, 1 kΩ, 5%, 1/8 W	Allen-Bradley/BB-102-5, or eq.	1
14	R11,12	Resistor, 150 Ω, 5%, 1/8 W	Allen-Bradley/BB-151-5, or eq.	2
15	R20,21	Resistor, 820 Ω, 5%, 1/8 W	Allen-Bradley/BB-821-5, or eq.	2
16	R22	Resistor, 200 Ω, 5%, 1/8 W	Allen-Bradley/BB-221-5, or eq.	1
17	TP1,AG,DG	Test Point Terminal. 76 Mil Hole Dia	Cambion/160-2044—02-01-00, or eq.	3
18	U9	DAC/TTL, 100 MHz, 12 Bits	AD9713	1
19	U10	OP-AMP, Low Noise	PMI/ OP-07EP	1
20	U11	OP-AMP, Low Distortion	AD9617JN	1
21	N/A	BNC Connector, Receptacle	Amphenol/31-5329, or eq.	1
22	N/A	Crimp Male Terminal for P3	Molex, 02-09-2103	1
23	DB792,PCB	Printed Circuit Board	Fairchild/DB792,PCB Drawing, Rev: A1	1
24	FB1-2	Ferrite Bead, Lead Mounted	Fair Rite/2743001111	2

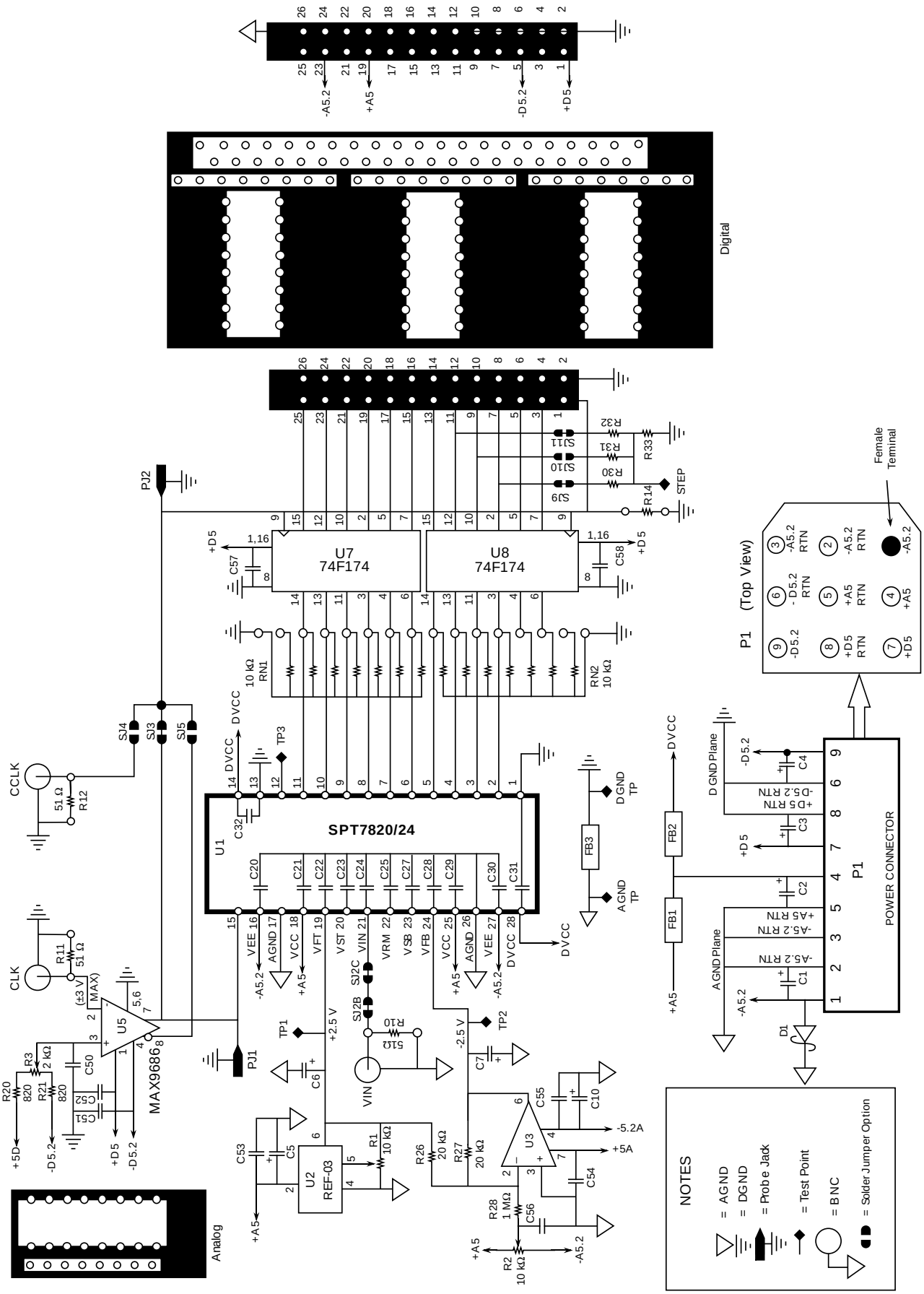
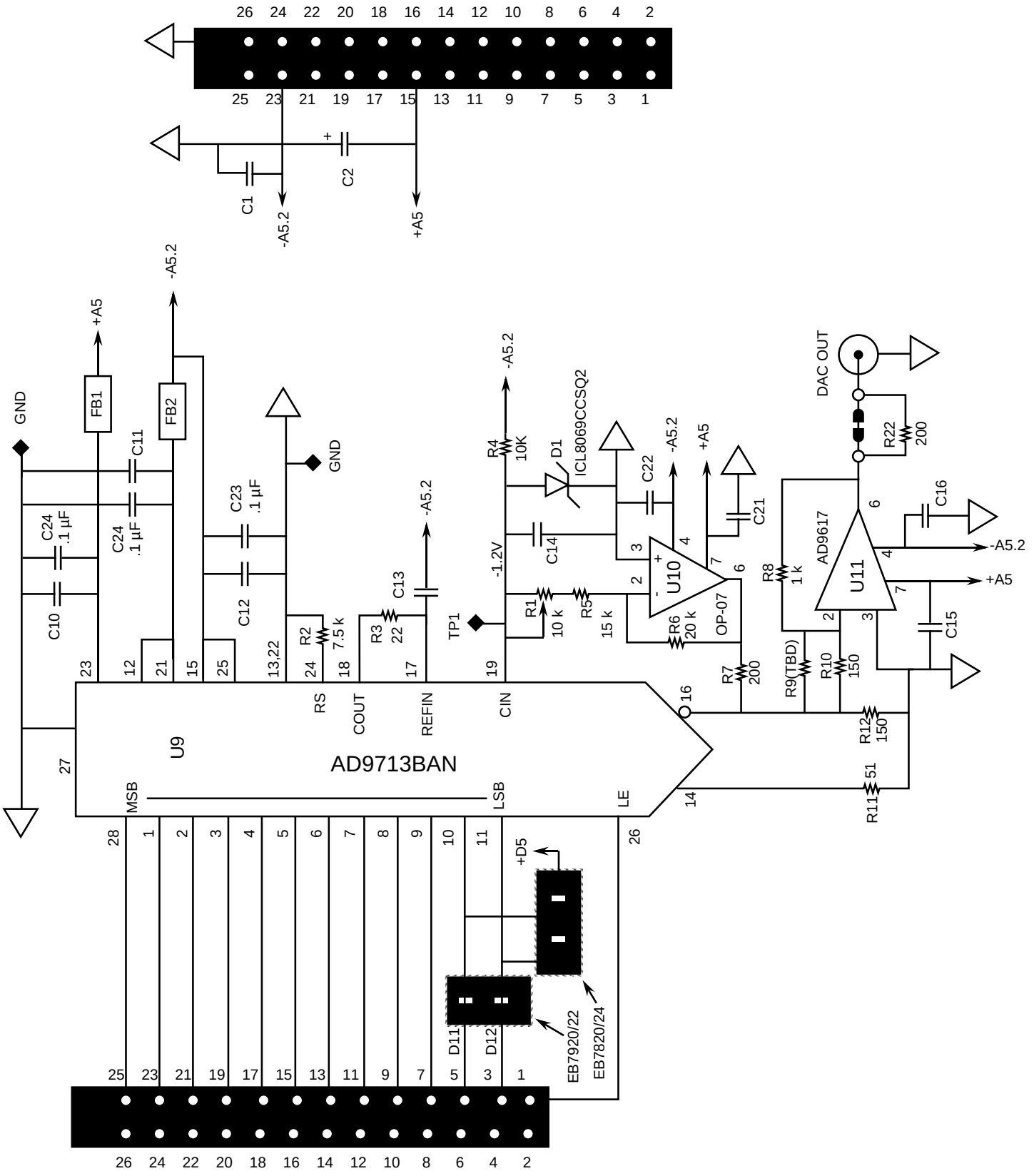


Figure 17 - EB7820/24 Detail Schematic, Rev B


26 24 22 20 18 16 14 12 10 8 6 4 2
25 23 21 19 17 15 13 11 9 7 5 3 1
C1
C2
-A5.2
+A5
GND
FB1
FB2
C10 .1 µF
C11
C12
C23 .1 µF
C24 .1 µF
R2 7.5 k
R3 22
C13
TP1
R1 10 k
R5 15 k
R4 10K
D1 ICL8069CCSQ2
C14
-1.2V
U10 OP-07
R6 20 k
C22
C21
R7 200
DAC OUT
R22 200
C16
AD9617
U11
R8 1 k
R9(TBD)
R10 150
R12 150
R11 51
C15
U9
AD9713BAN
RS
COUT
REFIN
CIN
MSB
LSB
LE
+D5
D11
D12
EB7920/22
EB7820/24

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.