

FIN3385 • FIN3383 Low Voltage 28-Bit Flat Panel Display Link Serializers

General Description

The FIN3385 and FIN3383 transform 28 bit wide parallel LVTTTL (Low Voltage TTL) data into 4 serial LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data stream over a separate LVDS link. Every cycle of transmit clock 28 bits of input LVTTTL data are sampled and transmitted.

These chipsets are an ideal solution to solve EMI and cable size problems associated with wide and high-speed TTL interfaces.

Features

- Low power consumption
- 20 MHz to 85 MHz shift clock support
- $\pm 1V$ common-mode range around 1.2V
- Narrow bus reduces cable size and cost
- High throughput (up to 2.38 Gbps throughput)
- Internal PLL with no external component
- Compatible with TIA/EIA-644 specification
- Devices are offered in 48- and 56-lead TSSOP packages

Ordering Code:

Order Number	Package Number	Package Description
FIN3383MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FIN3385MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

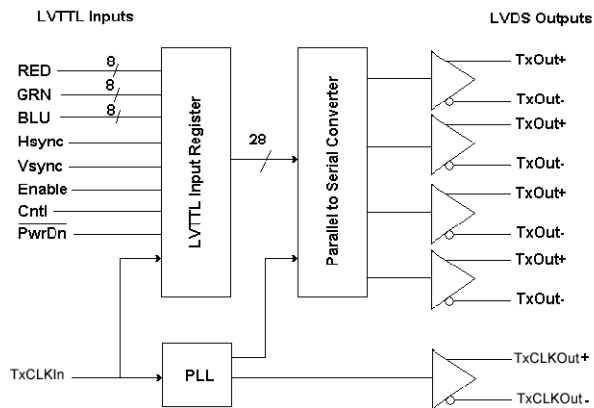
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

TABLE 1. Display Panel Link Serializers/De-Serializers Chip Matrix

Part	CLK Frequency	LVTTTL IN	LVDS OUT	Package
FIN3385	85	28	4	56 TSSOP
FIN3383	66	28	4	56 TSSOP

Block Diagram

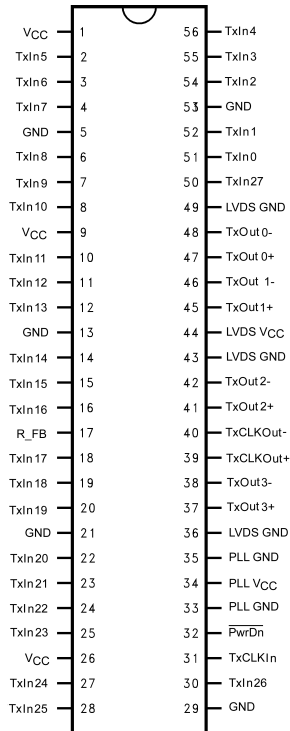
Functional Diagram for FIN3385 and FIN3383



Pin Descriptions

Pin Names	I/O Type	Number of Pins	Description of Signals
TxIn	I	28/21	LVTTTL Level Inputs
TxCLKIn	I	1	LVTTTL Level Clock Input The rising edge is for data strobe.
TxOut+	O	4/3	Positive LVDS Differential Data Output
TxOut-	O	4/3	Negative LVDS Differential Data Output
TxCLKOut+	O	1	Positive LVDS Differential Clock Output
TxCLKOut-	O	1	Negative LVDS Differential Clock Output
R_FB	I	1	Rising Edge Clock (HIGH), Falling Edge Clock (LOW)
PwrDn	I	1	LVTTTL Level Power-Down Input Assertion (LOW) puts the outputs in High Impedance state.
PLL V _{CC}	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V _{CC}	I	1	Power Supply Pin for LVDS Outputs
LVDS GND	I	3	Ground Pins for LVDS Outputs
V _{CC}	I	3	Power Supply Pins for LVTTTL Inputs
GND	I	5	Ground pins for LVTTTL Inputs
NC			No Connect

Connection Diagram



Truth Table

Inputs			Outputs	
TxIn	TxCLKIn	PwrDn (Note 1)	TxOut±	TxCLKOut±
Active	Active	H	L/H	L/H
Active	L/H/Z	H	L/H	X (Note 2)
F	Active	H	L	L/H
F	F	H	L	X (Note 2)
X	X	L	Z	Z

H = HIGH Logic Level
 L = LOW Logic Level
 X = Don't Care
 Z = High Impedance
 F = Floating

Note 1: The outputs of the transmitter or receiver will remain in a High Impedance state until V_{CC} reaches 2V.

Note 2: TxCLKOut± will settle at a free running frequency when the part is powered up, PwrDn is HIGH and the TxCLKIn is a steady logic level (L/H/Z).

Absolute Maximum Ratings (Note 3)

Power Supply Voltage (V_{CC})	-0.3V to +4.6V
TTL/CMOS Input/Output Voltage	-0.5V to +4.6V
LVDS Input/Output Voltage	-0.3V to +4.6V
LVDS Output Short Circuit Current (I_{OSD})	Continuous
Storage Temperature Range (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 4 seconds)	260°C
ESD Rating (HBM, 1.5 k Ω , 100 pF)	
I/O to GND	>10.0 kV
All Pins	>6.5 kV
ESD Rating (MM, 0 Ω , 200 pF)	>400V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Operating Temperature (T_A) <small>(Note 3)</small>	-10°C to +70°C
Maximum Supply Noise Voltage (V_{CCNPP})	100 mV _{P-P} <small>(Note 4)</small>

Note 3: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 4: 100mV V_{CC} noise should be tested for frequency at least up to 2 MHz. All the specification below should be met under such a noise.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Note 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
Transmitter LVTTTL Input Characteristics							
V_{IH}	Input High Voltage		2.0		V_{CC}	V	
V_{IL}	Input Low Voltage		GND		0.8	V	
V_{IK}	Input Clamp Voltage	$I_{IK} = -18$ mA		-0.79	-1.5	V	
I_{IN}	Input Current	$V_{IN} = 0.4V$ to 4.6V		1.8	10.0	μ A	
		$V_{IN} = GND$	-10.0	0			
Transmitter LVDS Output Characteristics <small>(Note 6)</small>							
V_{OD}	Output Differential Voltage	$R_L = 100 \Omega$, See Figure 1	250	TBD	450	mV	
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				35.0	mV	
V_{OS}	Offset Voltage		1.125	1.25	1.375	V	
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH					mV	
I_{OS}	Short Circuit Output Current	$V_{OUT} = 0V$		-3.5	-5.0	mA	
I_{OZ}	Disabled Output Leakage Current	$DO = 0V$ to 4.6V, $PwrDn = 0V$		± 1.0	± 10.0	μ A	
Transmitter Supply Current							
I_{CCWT}	28:4 Transmitter Power Supply Current for Worst Case Pattern (With Load) <small>(Note 7)</small>	$R_L = 100 \Omega$, See Figure 2	32.5 MHz		31.0	49.5	mA
			40.0 MHz		32.0	55.0	
			66.0 MHz		37.0	60.5	
			85.0 MHz		42.0	66.0	
I_{CCPDT}	Powered Down Supply Current	$PwrDn = 0.8V$		10.0	55.0	μ A	
I_{CCGT}	28:4 Transmitter Supply Current for 16 Grayscale <small>(Note 7)</small>	See Figure 11 <small>(Note 8)</small>	32.5 MHz		29.0	41.8	mA
			40.0 MHz		30.0	44.0	
			65.0 MHz		35.0	49.5	
			85.0 MHz		39.0	55.0	

Note 5: All Typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 3.3V$.

Note 6: Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage are referenced to ground unless otherwise specified (except ΔV_{OD} and V_{OD}).

Note 7: The power supply current for both transmitter and receiver can be different with the number of active I/O channels.

Note 8: The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t _{TCP}	Transmit Clock Period		11.76	T	50.0	ns
t _{TCH}	Transmit Clock (TxCLKIn) HIGH Time	See Figure 4	0.35	0.5	0.65	T
t _{TCL}	Transmit Clock Low Time		0.35	0.5	0.65	T
t _{CLKT}	TxCLKIn Transition Time (Rising and Falling)	(10% to 90%) See Figure 5	1.0		6.0	ns
t _{JIT}	TxCLKIn Cycle-to-Cycle Jitter				3.0	ns
t _{XIT}	TxIn Transition Time		1.5		6.0	ns
LVDS Transmitter Timing Characteristics						
t _{TLH}	Differential Output Rise Time (20% to 80%)	See Figure 3		0.75	1.5	ns
t _{THL}	Differential Output Fall Time (80% to 20%)			0.75	1.5	ns
t _{STC}	TxIn Setup to TxCLNIn	See Figure 4 (f = 85 MHz)	2.5			ns
t _{HTC}	TxIn Holds to TCLKIn		0			ns
t _{TPDD}	Transmitter Power-Down Delay	See Figure 7, (Note 9)			100	ns
t _{TCCD}	Transmitter Clock Input to Clock Output Delay	(T _A = 25°C and with V _{CC} = 3.3V)			5.5	ns
	Transmitter Clock Input to Clock Output Delay	See Figure 6	2.8		6.8	
Transmitter Output Data Jitter (f = 40 MHz) (Note 10)						
t _{TPPB0}	Transmitter Output Pulse Position of Bit 0	See Figure 9 $a = \frac{1}{f \times 7}$	-0.25	0	0.25	ns
t _{TPPB1}	Transmitter Output Pulse Position of Bit 1		a-0.25	a	a+0.25	ns
t _{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a-0.25	2a	2a+0.25	ns
t _{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a-0.25	3a	3a+0.25	ns
t _{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a-0.25	4a	4a+0.25	ns
t _{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a-0.25	5a	5a+0.25	ns
t _{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a-0.25	6a	6a+0.25	ns
Transmitter Output Data Jitter (f = 65 MHz) (Note 10)						
t _{TPPB0}	Transmitter Output Pulse Position of Bit 0	See Figure 9 $a = \frac{1}{f \times 7}$	-0.2	0	0.2	ns
t _{TPPB1}	Transmitter Output Pulse Position of Bit 1		a-0.2	a	a+0.2	ns
t _{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a-0.2	2a	2a+0.2	ns
t _{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a-0.2	3a	3a+0.2	ns
t _{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a-0.2	4a	4a+0.2	ns
t _{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a-0.2	5a	5a+0.2	ns
t _{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a-0.2	6a	6a+0.2	ns
Transmitter Output Data Jitter (f = 85 MHz) (Note 10)						
t _{TPPB0}	Transmitter Output Pulse Position of Bit 0	See Figure 9 $a = \frac{1}{f \times 7}$	-0.2	0	0.2	ns
t _{TPPB1}	Transmitter Output Pulse Position of Bit 1		a-0.2	a	a+0.2	ns
t _{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a-0.2	2a	2a+0.2	ns
t _{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a-0.2	3a	3a+0.2	ns
t _{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a-0.2	4a	4a+0.2	ns
t _{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a-0.2	5a	5a+0.2	ns
t _{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a-0.2	6a	6a+0.2	ns
t _{JCC}	FIN3385 Transmitter Clock Out Jitter (Cycle-to-Cycle)	f = 40 MHz		350	370	ps
		f = 65 MHz		210	230	
		f = 85 MHz		110	150	
t _{TPLLS}	Transmitter Phase Lock Loop Set Time (Note 11)	See Figure 12, (Note 10)			10.0	ms

Note 9: Outputs of all transmitters stay in 3-STATE until power reaches 2V. Both clock and data output begins to toggle 10ms after V_{CC} reaches 3V and Power-Down pin is above 1.5V.

Note 10: This output data pulse position works for TTL inputs except the LVDS output bit mapping difference (see Figure 8). Figure 9 shows the skew between the first data bit and clock output. Also 2-bit cycle delay is guaranteed when the MSB is output from transmitter.

Note 11: This jitter specification is based on the assumption that PLL has a ref clock with cycle-to-cycle input jitter less than 2ns.

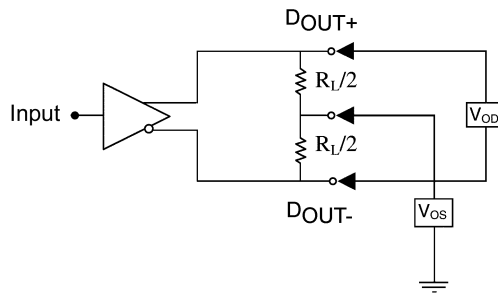
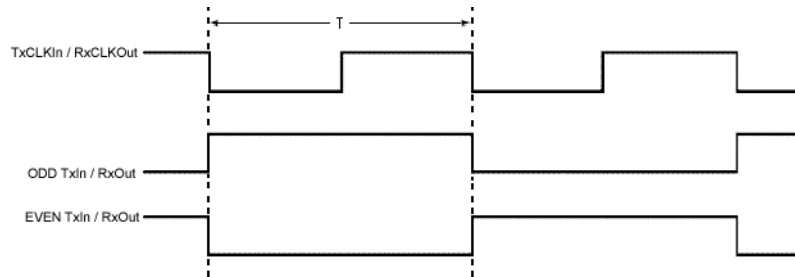


FIGURE 1. Differential LVDS Output DC Test Circuit

AC Loading and Waveforms



Note: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVTTTL/CMOS I/O. Depending on the valid strobe edge of transmitter, the TxCLKIn can be either rising or falling edge data strobe.

FIGURE 2. "Worst Case" Test Pattern

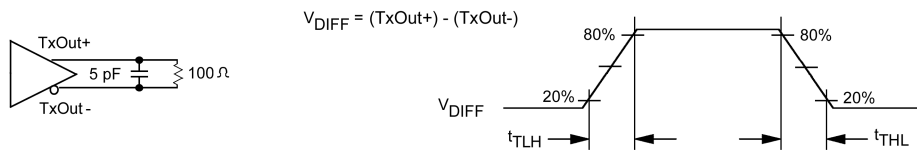


FIGURE 3. Transmitter LVDS Output Load and Transition Times

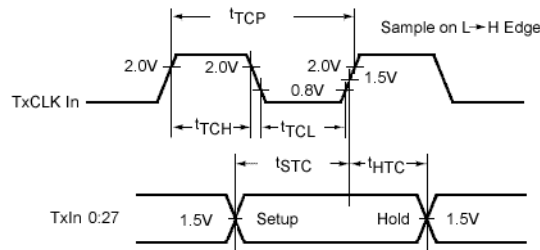


FIGURE 4. Transmitter Setup/Hold and HIGH/LOW Times (Rising Edge Strobe)

AC Loading and Waveforms (Continued)

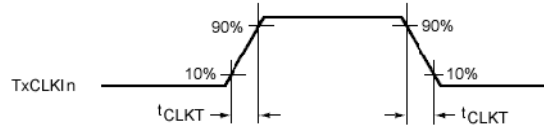


FIGURE 5. Transmitter Input Clock Transition Time

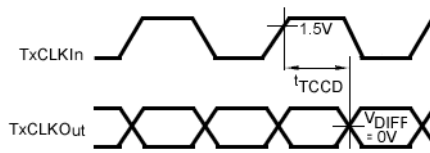


FIGURE 6. Transmitter Clock In to Clock Out Delay (Rising Edge Strobe)

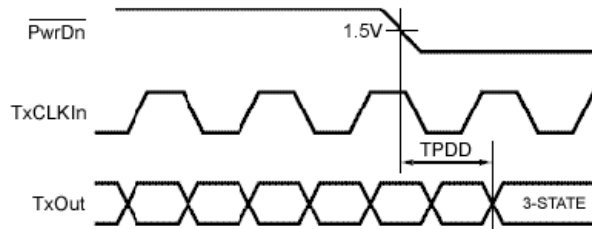
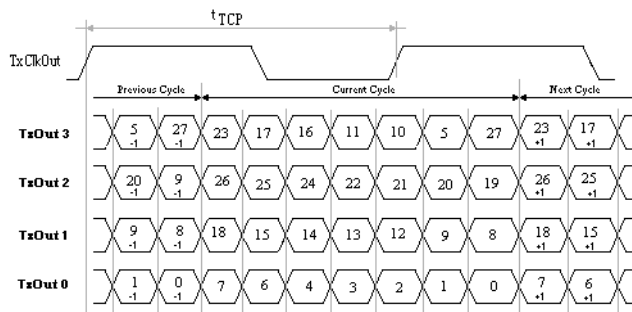


FIGURE 7. Transmitter Power-Down Delay



Note: The information in this diagram shows the relationship between clock out and the first data bit. A 2-bit cycle delay is guaranteed when the MSB is output from the transmitter.

FIGURE 8. 28 Parallel LVTTL Inputs Mapped to 4 Serial LVDS Outputs

AC Loading and Waveforms (Continued)

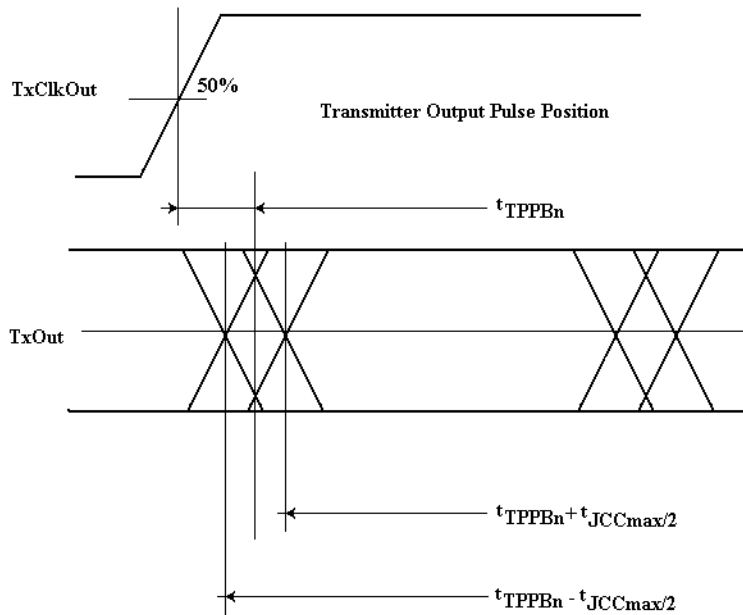
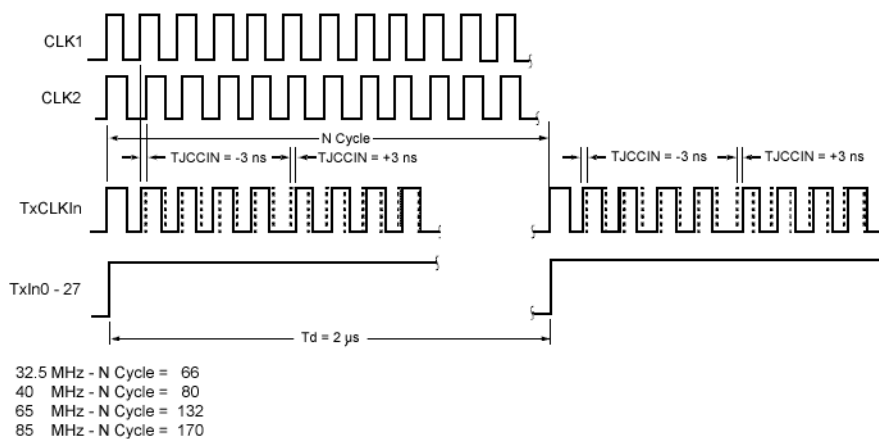


FIGURE 9. Transmitter Output Pulse Bit Position



Note: This jitter pattern is used to test the jitter response (Clock Out) of the device over the power supply range with worst jitter ± 3 ns (cycle-to-cycle) clock input. The specific test methodology is as follows:

- Switching input data TxIn0 to TxIn20 at 0.5 MHz, and the input clock is shifted to left -3 ns and to the right $+3$ ns when data is HIGH.
- The ± 3 ns cycle-to-cycle input jitter is the static phase error between the two clock sources. Jumping between two clock sources to simulate the worst case of clock edge jump (3 ns) from graphical controllers. Cycle-to-cycle jitter at TxCLK out pin should be measured cross V_{CC} range with 100mV noise (V_{CC} noise frequency < 2 MHz).

FIGURE 10. Timing Diagram of Transmitter Clock Input with Jitter

AC Loading and Waveforms (Continued)

Device Pin Name	Signal	Signal Pattern	Signal Frequency
TxCLKIn / RxCLKOut	Dot CLK		f
TxIn0 / RxOut0	R0		f / 16
TxIn1 / RxOut1	R1		f / 8
TxIn2 / RxOut2	R2		f / 4
TxIn3 / RxOut3	R3		f / 2
TxIn4 / RxOut4	R4		Steady State, LOW
TxIn5 / RxOut5	R5		Steady State, LOW
TxIn6 / RxOut6	G0		f / 16
TxIn7 / RxOut7	G1		f / 8
TxIn8 / RxOut8	G2		f / 4
TxIn9 / RxOut9	G3		f / 2
TxIn10 / RxOut10	G4		Steady State, LOW
TxIn11 / RxOut11	G5		Steady State, LOW
TxIn12 / RxOut12	B0		f / 16
TxIn13 / RxOut13	B1		f / 8
TxIn14 / RxOut14	B2		f / 4
TxIn15 / RxOut15	B3		f / 2
TxIn16 / RxOut16	B4		Steady State, LOW
TxIn17 / RxOut17	B5		Steady State, LOW
TxIn18 / RxOut18	HSYNC		Steady State, HIGH
TxIn19 / RxOut19	VSYNC		Steady State, HIGH
TxIn20 / RxOut20	ENA		Steady State, HIGH

Note: The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

FIGURE 11. "16 Grayscale" Test Pattern

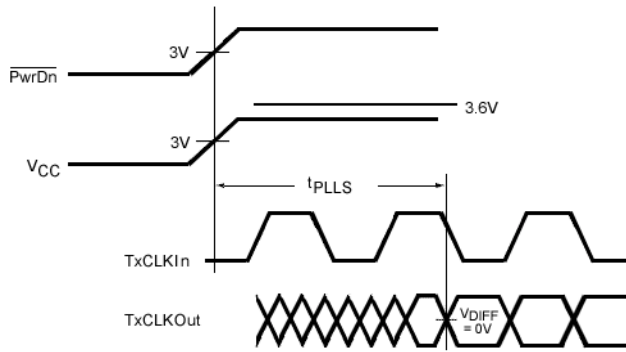
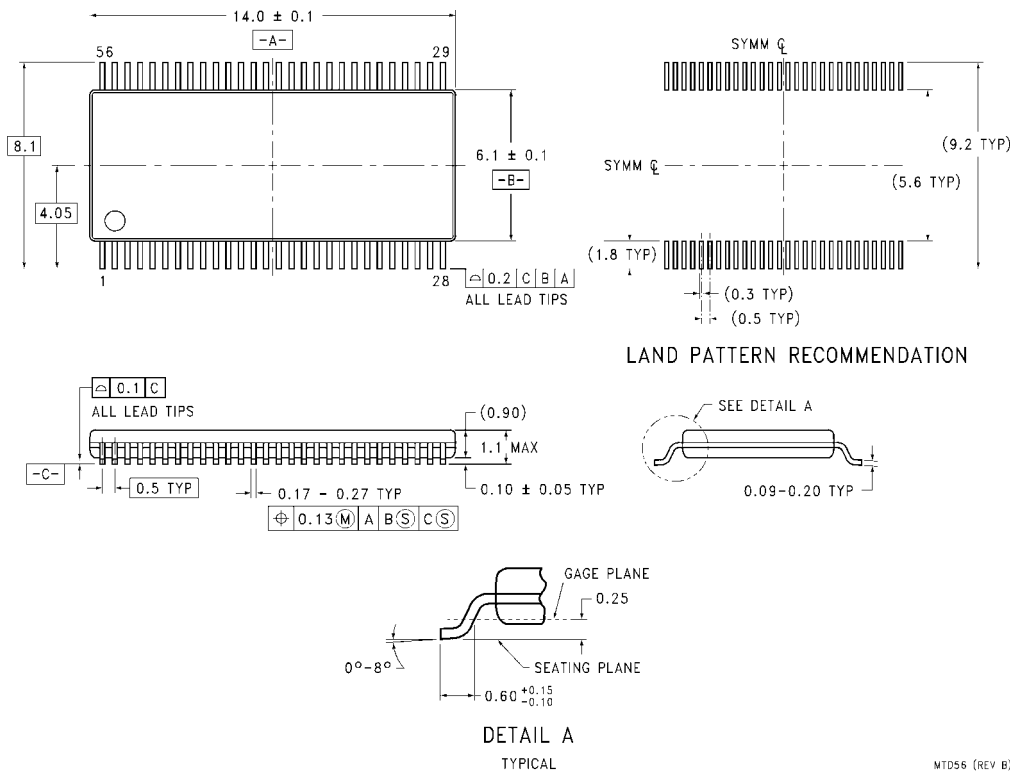


FIGURE 12. Transmitter Phase Lock Loop Time

Physical Dimensions inches (millimeters) unless otherwise noted



MTD56 (REV B)

**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com