TMC3533

Triple Video D/A Converter

8 bit, 80 Msps, 3.3V

Features

- 8-bit resolution
- 80, 50, and 30 megapixels per second
- ±0.5 LSB linearity error
- Sync, blank, and white controls
- Independent sync current output
- 1.0V p-p video into 37.5Ω or 75Ω load
- Enhancement of the ADV7120
  - Internal bandgap voltage reference
  - Double-buffered data for low distortion
  - Power-down sleep mode
- Double-buffered data for low distortion
- TTL-compatible inputs
- Low glitch energy
- Single +3.3V±5% Volt power supply

Applications

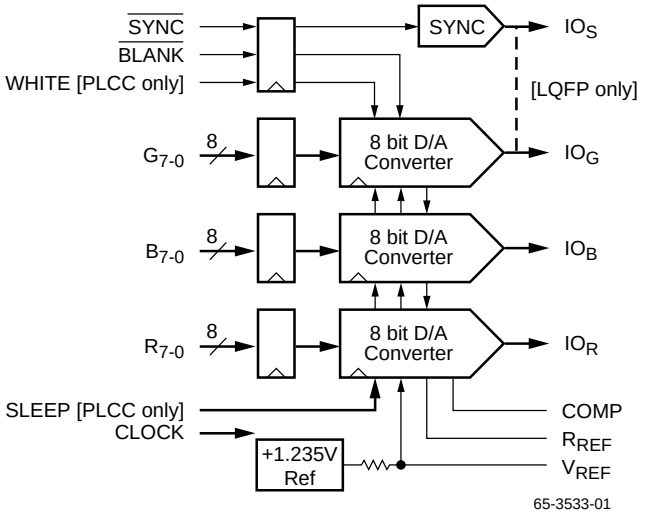
- Video and graphics displays
- Image processing systems
- Video signal conversion
- Broadcast television equipment
- Digital synthesis

Description

The TMC3533 is a high-speed triple 8-bit D/A converter especially suited for video and graphics applications. It offers 8-bit resolution, TTL-compatible inputs, low power consumption, a power-down sleep mode, and requires only a single +3.3V±5% Volt power supply. It has single-ended current outputs, $\overline{SYNC}$ and $\overline{BLANK}$ control inputs, and a separate current source for adding sync pulses to any D/A converter output. WHITE and SLEEP control inputs are available on PLCC parts. It is ideal for generating analog RGB from digital RGB and driving computer display and video monitors. Three speed grades are available: 30, 50, and 80 Msps.

The TMC3533 triple D/A converter is available in a 44-lead plastic J-leaded PLCC. It is also available in a 48-lead plastic LQFP package. It is fabricated on a sub-micron CMOS process with performance guaranteed from 0°C to 70°C.

Block Diagram



Functional Description

The TMC3533 is a low-cost triple 8-bit CMOS D/A converter designed to directly drive computer CRT displays at pixel rates up to 80 Msps. It comprises three identical 8-bit D/A converters with registered data inputs, common clock, and internal voltage reference. An independent current source allows sync to be added to any D/A converter output.

Digital Inputs

All digital inputs are TTL-compatible. Data are registered on the rising edge of the CLK signal. The analog output changes t_{DO} after the rising edge of CLK. There is one stage of pipeline delay on the chip. The guaranteed clock rates of the TMC3533 are 80, 50, and 30 MHz.

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs control the output level (Figure 1 and Table 1) of the D/A converters during CRT retrace intervals. $\overline{\text{BLANK}}$ forces the D/A outputs to the blanking level while $\overline{\text{SYNC}}$ turns off a separate current source which is brought off the chip through the IO_S pin.

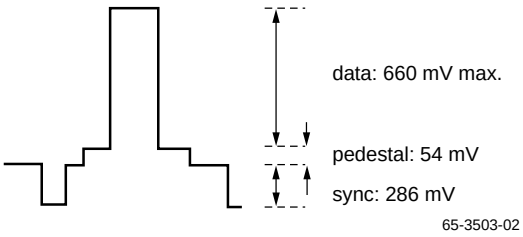


Figure 1. Nominal Output Levels

IO_S may be connected to any one D/A output, or used independently. It is commonly tied to the green D/A converter for “Sync on Green” operation. This connection adds a 40 IRE sync pulse to the D/A output and brings that D/A output to 0.0 Volts during the sync tip. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are registered on the rising edge of CLK.

$\overline{\text{BLANK}}$ gates the D/A inputs and sets the pedestal voltage. If $\overline{\text{BLANK}}$ = HIGH, the D/A inputs are added to a pedestal which offsets the current output. If $\overline{\text{BLANK}}$ = LOW, data inputs and the pedestal are disabled.

WHITE

The WHITE control drives all three D/As to full-scale, overriding the data inputs. It is overridden by the $\overline{\text{BLANK}}$ input, and is independent of $\overline{\text{SYNC}}$.

SLEEP

The SLEEP control, when HIGH, places the TMC3533 in a power-down state. This function operates asynchronously.

D/A Outputs

Each D/A output is a current source. To obtain a voltage output, a resistor must be connected to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

Normally, a source termination resistor of 75 Ohms is connected between the D/A current output pin and GND near the D/A converter. A 75 Ohm coaxial cable may then be connected with another 75 Ohm termination resistor at the far end of the cable. This "double termination" presents the D/A converter with a net resistive load of 37.5 Ohms.

The TMC3533 may also be operated with a single 75 Ohm terminating resistor. To lower the output voltage swing to the desired range, the value of the resistor on R_{REF} should be increased.

Voltage Reference

The TMC3533 has an internal bandgap voltage reference of +1.235 Volts. An external voltage reference may be connected to the V_{REF} pin, overriding the internal voltage reference. All three D/A converters are driven from the same reference.

A 0.1µF capacitor must be connected between the COMP pin and V_{DD} to stabilize internal bias circuitry and ensure low-noise operation.

Power and Ground

The TMC3533 D/A converter requires a single +3.3 Volt power supply. The analog (V_{DD}) power supply voltage should be decoupled to GND to reduce power supply induced noise. 0.1µF decoupling capacitors should be placed as close as possible to the power pins.

The high slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

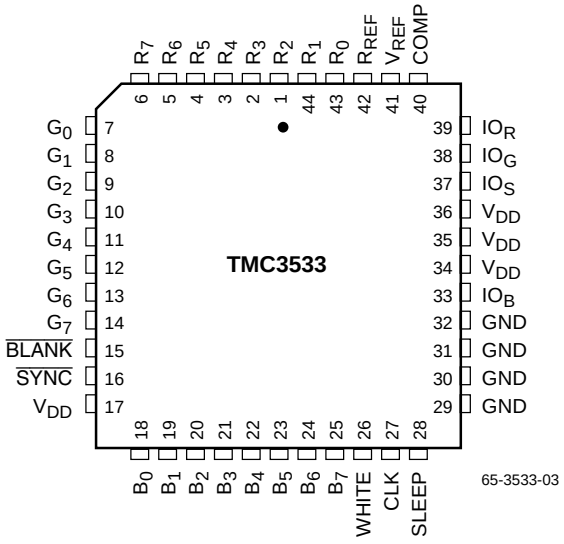
Table 1. Output Voltage versus Input Code, $\overline{SYNC}$, $\overline{BLANK}$, and WHITE

V_{REF} = 1.235 V, R_{REF} = 572 Ω, R_L = 37.5 Ω

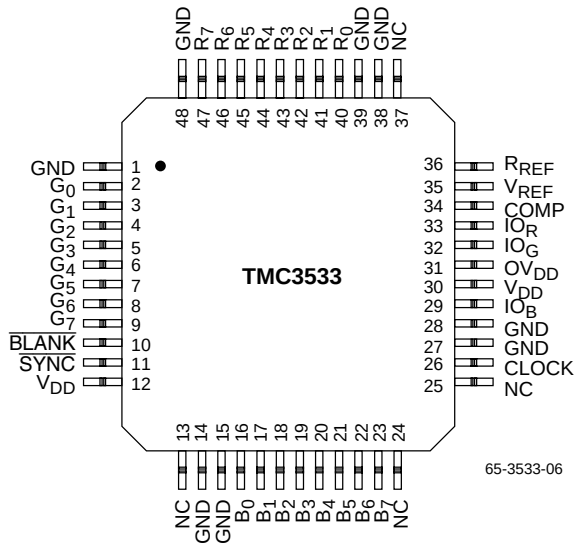
RGB7-0 (MSB…LSB)	All D/As				D/A with IOS Connected			
	$\overline{SYNC}$	$\overline{BLANK}$	WHITE	VOUT	$\overline{SYNC}$	$\overline{BLANK}$	WHITE	VOUT
XXXX XXXX	X	1	1	0.714	1	1	1	1.000
1111 1111	X	1	0	0.714	1	1	0	1.000
1111 1110	X	1	0	0.711	1	1	0	0.997
1111 1101	X	1	0	0.709	1	1	0	0.995
• •	• •	• •	• •	• •	• •	• •	• •	• •
0000 0000	X	1	0	0.385	1	1	0	0.671
1111 1111	X	1	0	0.383	1	1	0	0.669
• •	• •	• •	• •	• •	• •	• •	• •	• •
0000 0010	X	1	0	0.059	1	1	0	0.345
0000 0001	X	1	0	0.057	1	1	0	0.343
0000 0000	X	1	0	0.054	1	1	0	0.340
XXXX XXXX	X	0	X	0.000	1	0	X	0.286
XXXX XXXX	X	0	X	0.000	0	0	X	0.000

Pin Assignments

PLCC Package



LQFP Package



Notes (LQFP Package Only):

1. Pin functions White and Sleep are not available.
2. IO_S function is internally tied to IO_G pin.

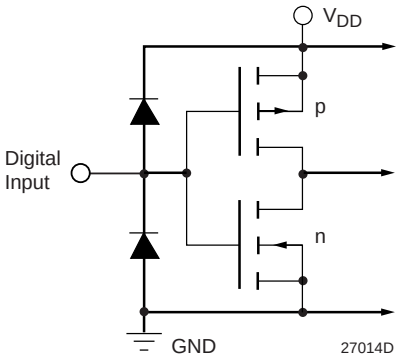
Pin Descriptions

Pin Name	Pin Number LQFP	Pin Number PLCC	Value	Pin Function Description
Clock and Pixel I/O				
CLK	26	27	TTL	**Clock Input.** The clock input is TTL-compatible and all pixel data is registered on the rising edge of CLK. It is recommended that CLK be driven by a dedicated TTL buffer to avoid reflection induced jitter, overshoot, and undershoot.
R_{7-0} G_{7-0} B_{7-0}	47-40 9-2 23-16	6-1, 44-43 14-7 25-18	TTL	**Red, Green, and Blue Pixel Inputs.** The R, G, and B digital inputs are TTL-compatible and registered on the rising edge of CLK.
Controls				
$\overline{SYNC}$	11	16	TTL	**Sync Pulse Input.** Bringing $\overline{SYNC}$ LOW, turns off a 40 IRE (7.62 mA) current source which forms a sync pulse on any D/A converter output connected to IO_S. $\overline{SYNC}$ is registered on the rising edge of CLK along with pixel data and has the same pipeline latency as $\overline{BLANK}$ and pixel data. $\overline{SYNC}$ does not override any other data and should be used only during the blanking interval. If the system does not require sync pulses, $\overline{SYNC}$ and IO_S should be connected to GND.
$\overline{BLANK}$	10	15	TTL	**Blanking Input.** When $\overline{BLANK}$ is LOW, pixel inputs are ignored and the D/A converter outputs are driven to the blanking level. $\overline{BLANK}$ is registered on the rising edge of CLK and has the same two-pipe latency as $\overline{SYNC}$ and Data.
WHITE	—	26	TTL	**Force Full Scale Input.** When WHITE is HIGH, pixel inputs are ignored and the D/A converter outputs are driven to their full-scale output level. A $\overline{BLANK}$ input overwrites a WHITE input. WHITE is register on the rising edge of CLK and has the same two-pipe latency as $\overline{SYNC}$ and Data.
SLEEP	—	28	TTL	**Power-down Control Input.** When HIGH, SLEEP places the D/A converter in a low-power-dissipation mode. The D/A current sources and the digital processing are disabled. The last data loaded into the input and D/A registers is retained. This control is asynchronous.
Video Outputs				
IO_R IO_G IO_B	33 32 29	39 38 33	0.714 V_{p-p}	**Red, Green, and Blue Data Outputs.** The current source outputs of the D/A converters are capable of driving RS-343A/SMPTE-170M compatible levels into doubly-terminated 75 Ohm lines. Sync pulses may be added to any D/A output.
IO_S	32 (connected to IO_G)	37	0.714 V_{p-p}	**SYNC Current Output.** When this pin is connected to any of the D/A converter outputs, a 40 IRE offset can be added to the video level. When the $\overline{SYNC}$ input is LOW, the current is turned off, bring the sync tip voltage to 0.0V. If no sync pulse is required, IO_S should be grounded. When $\overline{SYNC}$ is HIGH, the current flowing out of IO_S is: $IO_S = 3.64 (V_{REF} / R_{REF})$
Voltage Reference				
V_{REF}	35	41	+1.235 V	**Voltage Reference Input/Output.** An internal voltage source of +1.235 Volts is output on this pin. An external +1.235 Volt reference may be applied here which overrides the internal reference. Decoupling V_{REF} to GND with a 0.1µF ceramic capacitor is required.

Pin Descriptions (continued)

Pin Name	Pin Number LQFP	Pin Number PLCC	Value	Pin Function Description
R_{REF}	36	42	572 Ω	**Current-setting Resistor.** The full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. The nominal value for R_{REF} is found from: $R_{REF} = 9.1 (V_{REF}/I_{FS})$, but is optimized to be 572 Ω. I_{FS} is the full-scale (white) output current (amps) from an output without sync. Sync current is 0.4 I_{FS}. D/A full-scale (white) current may also be calculated from: $I_{FS} = V_{FS}/R_L$ Where V_{FS} is the white voltage level and R_L is the total resistive load (ohms) on each D/A converter. V_{FS} is the blank to full-scale voltage.
COMP	34	40	0.1 µF	**Compensation Capacitor.** A 0.1 µF ceramic capacitor must be connected between COMP and V_{DD} to stabilize internal bias circuitry.
Power, Ground				
V_{DD}	12, 30, 31	17, 34–36	+3.3 V	**Power Supply.**
GND	1, 14, 15, 27, 28, 38, 39, 48	29–32	0.0V	**Ground.**
NC	13, 24, 25, 37	—	—	**No Connect**

Equivalent Circuits



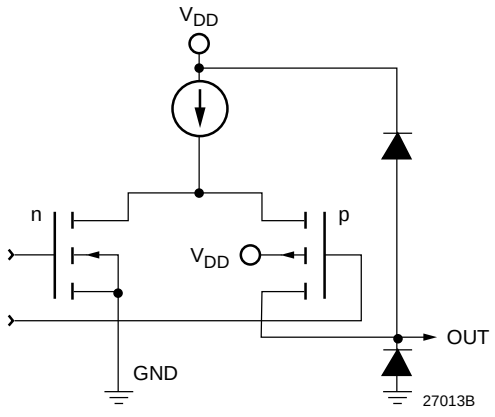


Figure 2. Equivalent Digital Input Circuit Figure 3. Equivalent Analog Output Circuit

Equivalent Circuits (continued)

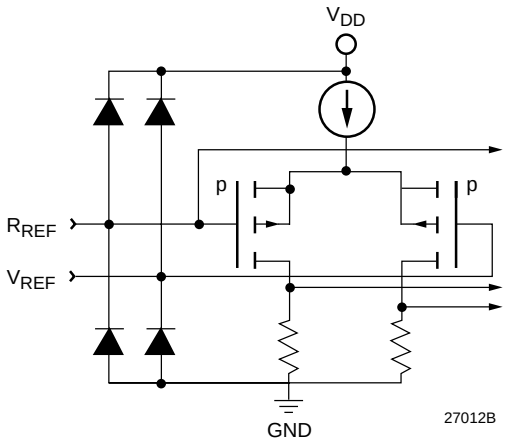


Figure 4. Equivalent Analog Input Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage				
V_{DD} (Measured to GND)	-0.5		7.0	V
Inputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-10.0		10.0	mA
Outputs				
Applied Voltage (measured to GND)[2]	-0.5		V_{DD} + 0.5	V
Forced Current[3,4]	-60.0		60.0	mA
Short Circuit Duration (single output in HIGH state to ground)			infinite	second
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase Soldering (1 minute)			220	°C
Storage	-65		150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
f_S	Conversion Rate	TMC3533-30			30	Msps
		TMC3533-50			50	Msps
		TMC3533-80			80	Msps
t_{PWH}	CLK Pulsewidth, HIGH		4			ns
t_{PWL}	CLK Pulsewidth, LOW		4			ns
t_s	Input Data Setup Time		3			ns
t_h	Input Date Hold Time		2			ns
V_{REF}	Reference Voltage, External		1.0	1.235	1.5	V
C_C	Compensation Capacitor			0.1		µF
R_L	Output Load			37.5		Ω
V_{IH}	Input Voltage, Logic HIGH		2.0		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.8	V
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions[3]	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[2]	V_{DD} = Max TMC3533-30 TMC3533-50 TMC3533-80			 95 95 105	 mA mA mA
I_{DDS}	Power Supply Current, Sleep Mode	V_{DD} = Max			3	mA
PD	Total Power Dissipation[2]	V_{DD} = Max TMC3533-30 TMC3533-50 TMC3533-80			 330 330 346	 mW mW mW
R_O	Output Resistance			100		kΩ
C_O	Output Capacitance	I_{OUT} = 0mA			30	pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = 3.0V			-1	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0.4V			1	µA
I_{REF}	V_{REF} Input Bias Current			0	±100	µA
V_{REF}	Reference Voltage Output			1.235		V
V_{OC}	Output Compliance	Referred to V_{DD}	-0.4	0	+1.5	V
C_{DI}	Digital Input Capacitance			4	10	pF

Notes:

1. Values shown in Typ column are typical for V_{DD} = +3.3V and T_A = 25°C
2. Minimum/Maximum values with V_{DD} = Max and T_A = Min
3. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 572Ω

Switching Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
t_D	Clock to Output Delay	V_{DD} = Min		10	15	ns
t_{SKEW}	Output Skew			1	2	ns
t_R	Output Risetime	10% to 90% of Full Scale		3	4	ns
t_F	Output Falltime	90% to 10% of Full Scale		3	4	ns
t_{SET}	Output Settling Time	to 3%/FS		15		ns

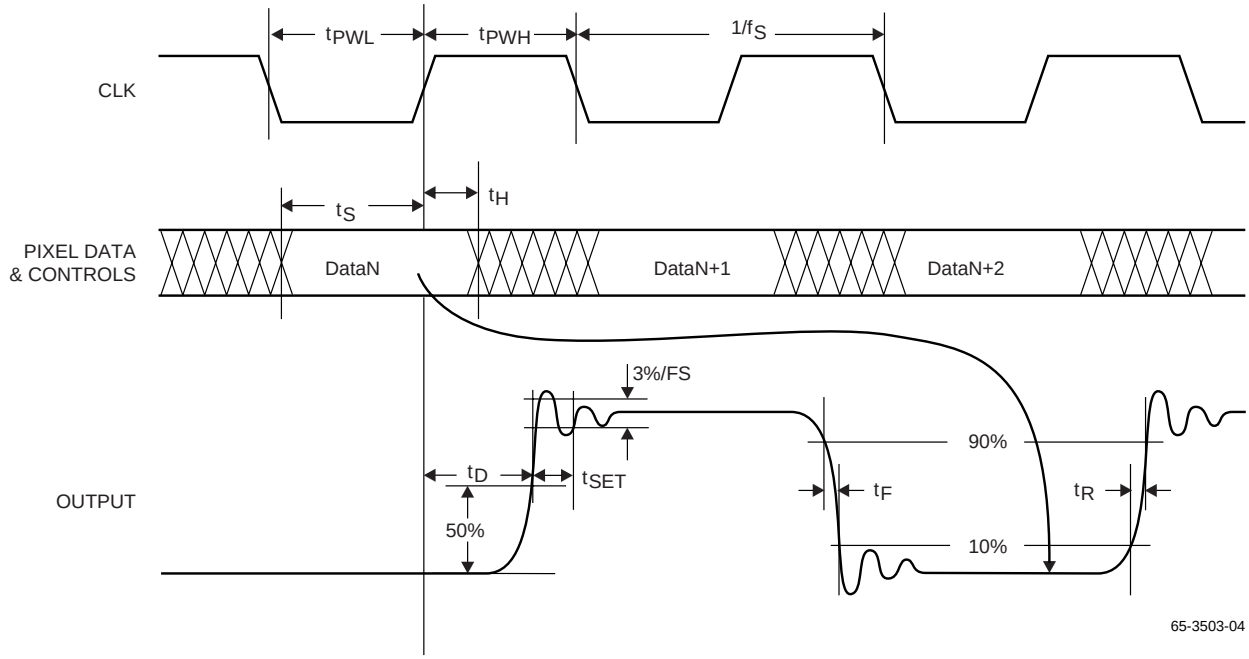
Notes:
1. Values shown in Typ column are typical for V_{DD} = +3.3V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 572Ω.

System Performance Characteristics

Parameter		Conditions[2]	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error	V_{DD}, V_{REF} = Nom		±0.1	±0.25	%/FS
E_{LD}	Differential Linearity Error	V_{DD}, V_{REF} = Nom		±0.1	±0.25	%/FS
E_{DM}	DAC to DAC Matching	V_{DD}, V_{REF} = Nom		7	10	%
I_{OFF}	Output Off Current	V_{DD} = Max, R, G, B = 000h $\overline{SYNC}$ = $\overline{BLANK}$ = 0			20	nA
PSRR	Power Supply Rejection Ratio				0.05	%/%

Notes:
1. Values shown in Typ column are typical for V_{DD} = +3.3V and T_A = 25°C.
2. V_{REF} = 1.235V, R_{LOAD} = 37.5Ω, R_{REF} = 572Ω.

Timing Diagram



Application Notes

Figure 4 illustrates a typical TMC3533 interface circuit. In this example, an optional 1.2 Volt bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the TMC3533 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The TMC3533 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DD}) come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_S, IO_R, IO_G, IO_B) as short as possible and as far as possible from all digital signals. The TMC3533 should be located near the board edge, close to the analog output connectors.
2. The power plane for the TMC3533 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC3533 is the same as that of the system's digital circuitry, power to the TMC3533 should be decoupled with 0.1µF and 0.01µF capacitors and isolated with a ferrite bead.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.
4. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC3533, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC3533 and its related analog circuitry can have an adverse effect on performance.
5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Related Products

- TMC3003 Triple 10-bit 80 Msps D/A Converter
- TMC2242C/TMC2243/TMC2246A Video Filters
- TMC2081 Digital Video Mixer
- TMC3503 Triple Video D/A Converter, 5V
- TMC22x5y Video Decoder

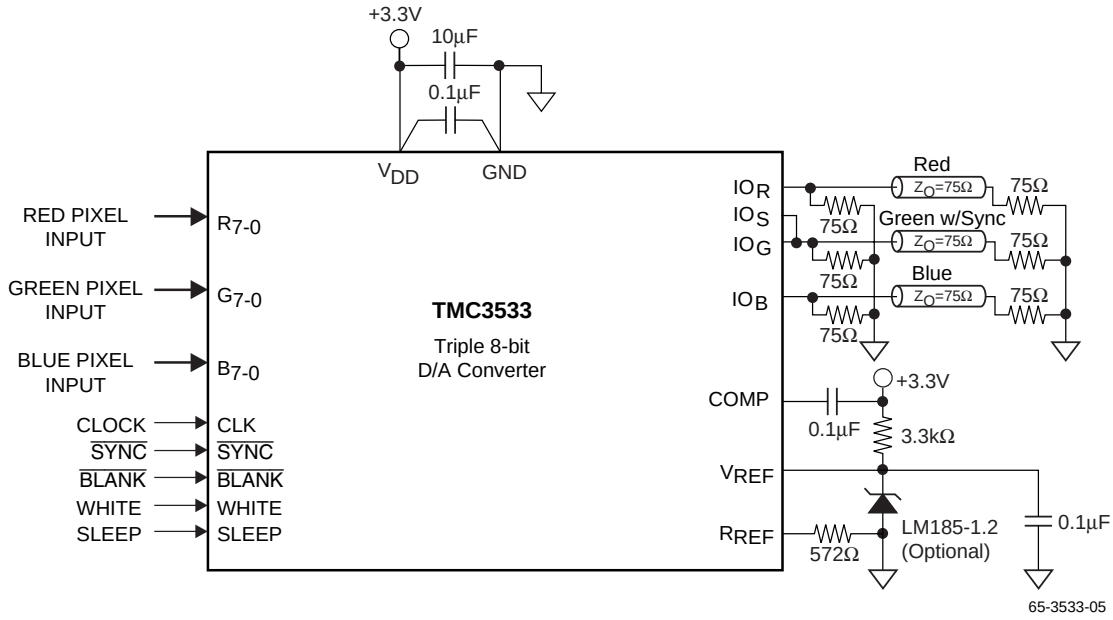


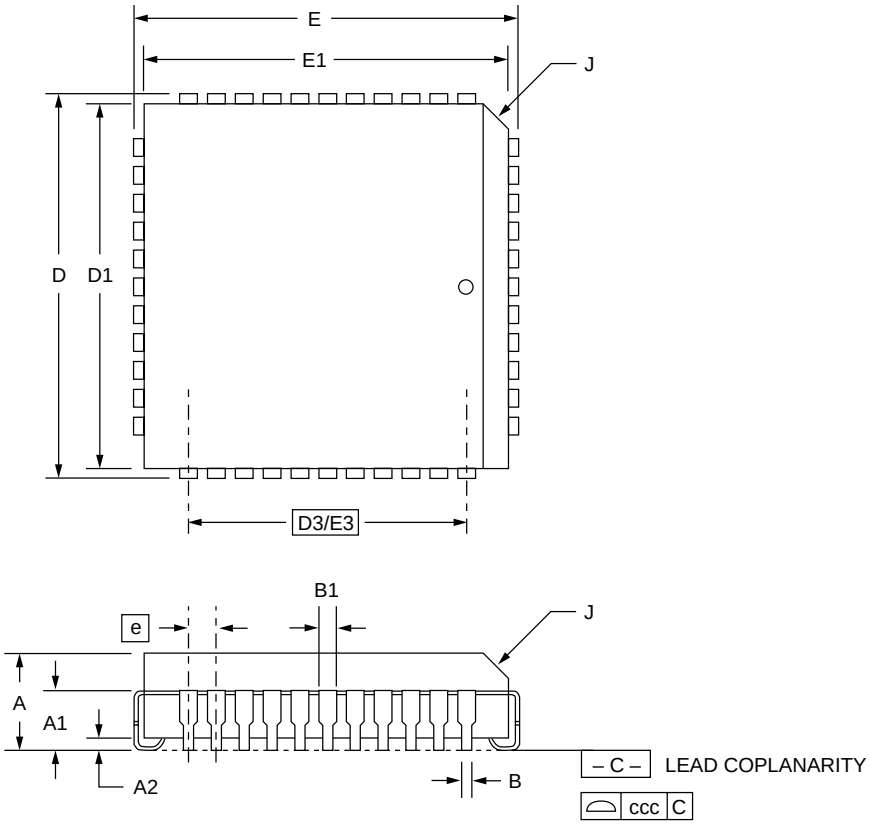
Figure 4. Typical Interface Circuit

Mechanical Dimensions – 44-pin PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)

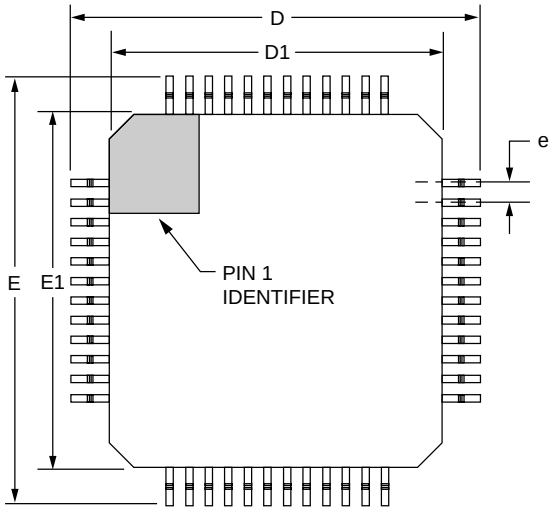


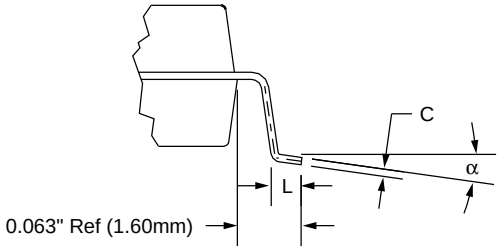
Mechanical Dimensions – 48-pin LQFP Package

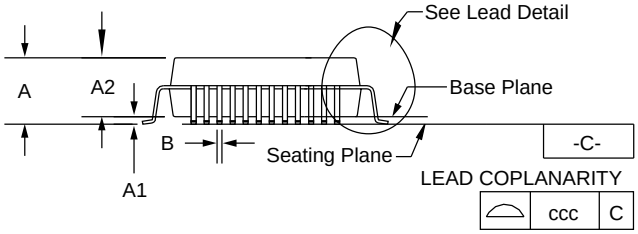
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.055	.063	1.40	1.60	
A1	.001	.005	.05	.15	
A2	.053	.057	1.35	1.45	
B	.006	.010	.17	.27	7
D/E	.346	.362	8.8	9.2	8
D1/E1	.268	.284	6.8	7.2	2
e	.019 BSC		.50 BSC		
L	.017	.029	.45	.75	6
N	48		48		4
ND	12		12		5
α	0°	7°	0°	7°	
ccc	.004		0.08		

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Pin 1 identifier is optional.
4. Dimension ND: Number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
8. To be determined at seating place —C—







Ordering Information

Product Number	Conversion Rate (Msps)	Temperature Range	Screening	Package	Package Marking
TMC3533R2C30	30 Msps	T_A = 0˚C to 70˚C	Commercial	44-Lead PLCC	3533LR2C30
TMC3533R2C50	50 Msps	T_A = 0˚C to 70˚C	Commercial	44-Lead PLCC	3533LR2C50
TMC3533R2C80	80 Msps	T_A = 0˚C to 70˚C	Commercial	44-Lead PLCC	3533LR2C80
TMC3533KRC30	30 Msps	T_A = 0˚C to 70˚C	Commercial	48-Lead LQFP	3533LKRC30
TMC3533KRC50	50 Msps	T_A = 0˚C to 70˚C	Commercial	48-Lead LQFP	3533LKRC50
TMC3533KRC80	80 Msps	T_A = 0˚C to 70˚C	Commercial	48-Lead LQFP	3533LKRC80