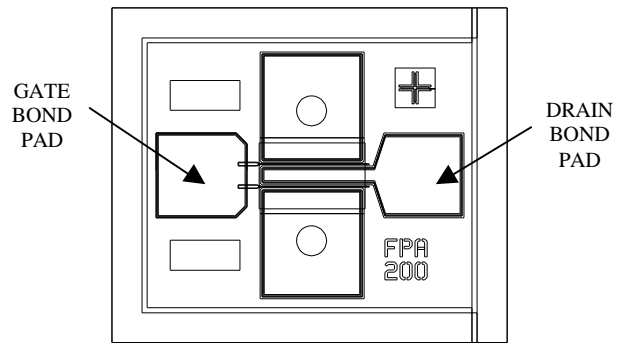


**FEATURES**

- ◆ 21 dBm Output Power at 1-dB Compression at 18 GHz
- ◆ 12.5 dB Power Gain at 18 GHz
- ◆ 55% Power-Added Efficiency
- ◆ Source Vias to Backside Metallization



DIE SIZE: 15.6X13.2 mils (395x335  $\mu\text{m}$ )  
 DIE THICKNESS: 3.9 mils (100  $\mu\text{m}$ )  
 BONDING PADS: 3.1X3.1 mils (80x80  $\mu\text{m}$ )

**DESCRIPTION AND APPLICATIONS**

The FPDA200V is an Aluminum Gallium Arsenide / Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25  $\mu\text{m}$  by 200  $\mu\text{m}$  Schottky barrier gate. The recessed “mushroom” gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for high dynamic range.

Typical applications include high dynamic range driver stages for commercial applications including wireless infrastructure systems, broad bandwidth amplifiers, and optical systems.

Source vias have been added for improved performance and assembly convenience. Each via hole has 0.02 nH of inductance. Additionally, the via holes remove the need for source bond wires, meaning only two bond wires are required for assembly. Because the via connects the source pad to the backside metallization, self-bias configurations should be designed with caution.

**ELECTRICAL SPECIFICATIONS @  $T_{\text{Ambient}} = 25^{\circ}\text{C}$** 

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Saturated Drain-Source Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 2 \text{ V}; V_{\text{GS}} = 0 \text{ V}$	40	60	85	mA
Power at 1-dB Compression	P-1dB	$V_{\text{DS}} = 5 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	19	21		dBm
Power Gain at 1-dB Compression	G-1dB	$V_{\text{DS}} = 5 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$	11	12.5		dB
Power-Added Efficiency	PAE	$V_{\text{DS}} = 5 \text{ V}; I_{\text{DS}} = 50\% I_{\text{DSS}}$		55		%
Maximum Drain-Source Current	$I_{\text{MAX}}$	$V_{\text{DS}} = 2 \text{ V}; V_{\text{GS}} = 1 \text{ V}$		125		mA
Transconductance	$G_{\text{M}}$	$V_{\text{DS}} = 2 \text{ V}; V_{\text{GS}} = 0 \text{ V}$	50	70		mS
Gate-Source Leakage Current	$I_{\text{GSO}}$	$V_{\text{GS}} = -5 \text{ V}$		1	10	$\mu\text{A}$
Pinch-Off Voltage	$V_{\text{P}}$	$V_{\text{DS}} = 2 \text{ V}; I_{\text{DS}} = 1 \text{ mA}$	-0.25	-0.8	-1.5	V
Gate-Source Breakdown Voltage Magnitude	$ V_{\text{BDGS}} $	$I_{\text{GS}} = 1 \text{ mA}$	6	7		V
Gate-Drain Breakdown Voltage Magnitude	$ V_{\text{BDGD}} $	$I_{\text{GD}} = 1 \text{ mA}$	8	9		V
Thermal Resistivity	$\Theta_{\text{JC}}$			260		$^{\circ}\text{C}/\text{W}$

frequency=18 GHz

**• ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	$V_{DS}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		8	V
Gate-Source Voltage	$V_{GS}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		-3	V
Drain-Source Current	$I_{DS}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		$2 \times I_{DSS}$	mA
Gate Current	$I_G$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		10	mA
RF Input Power	$P_{IN}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		100	mW
Channel Operating Temperature	$T_{CH}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		175	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	—	-65	175	$^{\circ}\text{C}$
Total Power Dissipation	$P_{TOT}$	$T_{Ambient} = 22 \pm 3 \text{ }^{\circ}\text{C}$		550	mW

**Notes:**

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Power Dissipation defined as:  $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$ , where  
 $P_{DC}$ : DC Bias Power  
 $P_{IN}$ : RF Input Power  
 $P_{OUT}$ : RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 25 $^{\circ}\text{C}$ :  
 $P_{TOT} = 550\text{mW} - (3.7\text{mW}/^{\circ}\text{C}) \times T_{HS}$   
 where  $T_{HS}$  = heatsink or ambient temperature.

**• HANDLING PRECAUTIONS**

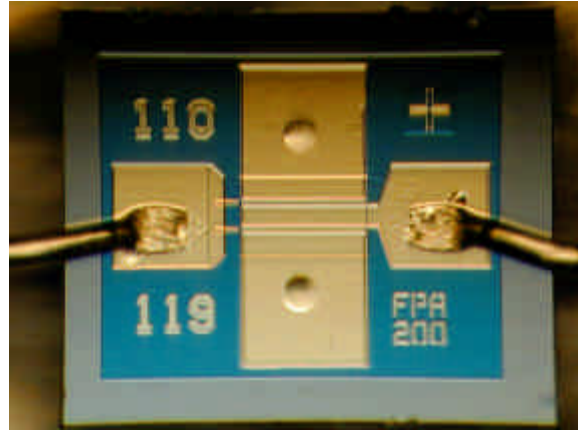
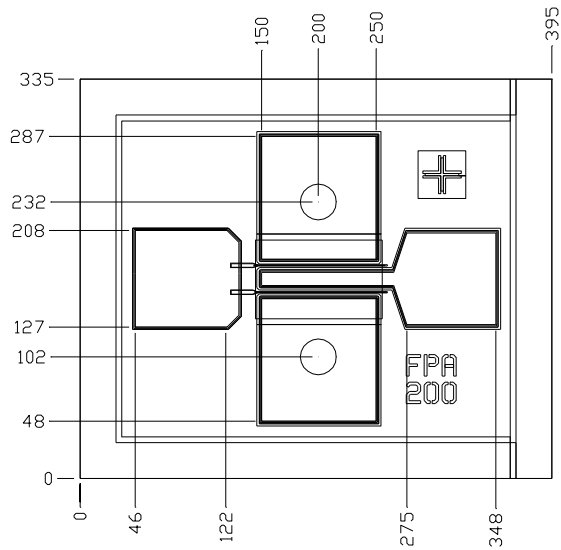
To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A (0-500 V). Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

**• ASSEMBLY INSTRUCTIONS**

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290 $^{\circ}\text{C}$ ; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260 $^{\circ}\text{C}$ .

**• APPLICATIONS NOTES & DESIGN DATA**

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.



Units in microns

All information and specifications are subject to change without notice.