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	頁 次 Page : 1 / 1

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1.0	2001/08/29	2001/08/29		新增訂
1.1	2001/10/22	2001/10/22	2	1. 刪除Fig.2. Pin Diagram。
			3	2. 修改Pin List。
			11、12	3. 修改Pin description。
1.2	2002/07/09	2002/07/10	6	1. 修改T <sub>OPR</sub> = -20 to +75°C
			7	2. 修改XDON function

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**EK7304**

DATA SHEET

**256 Output TFT Gate Driver IC**



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## 256- Output TFT Gate Driver IC

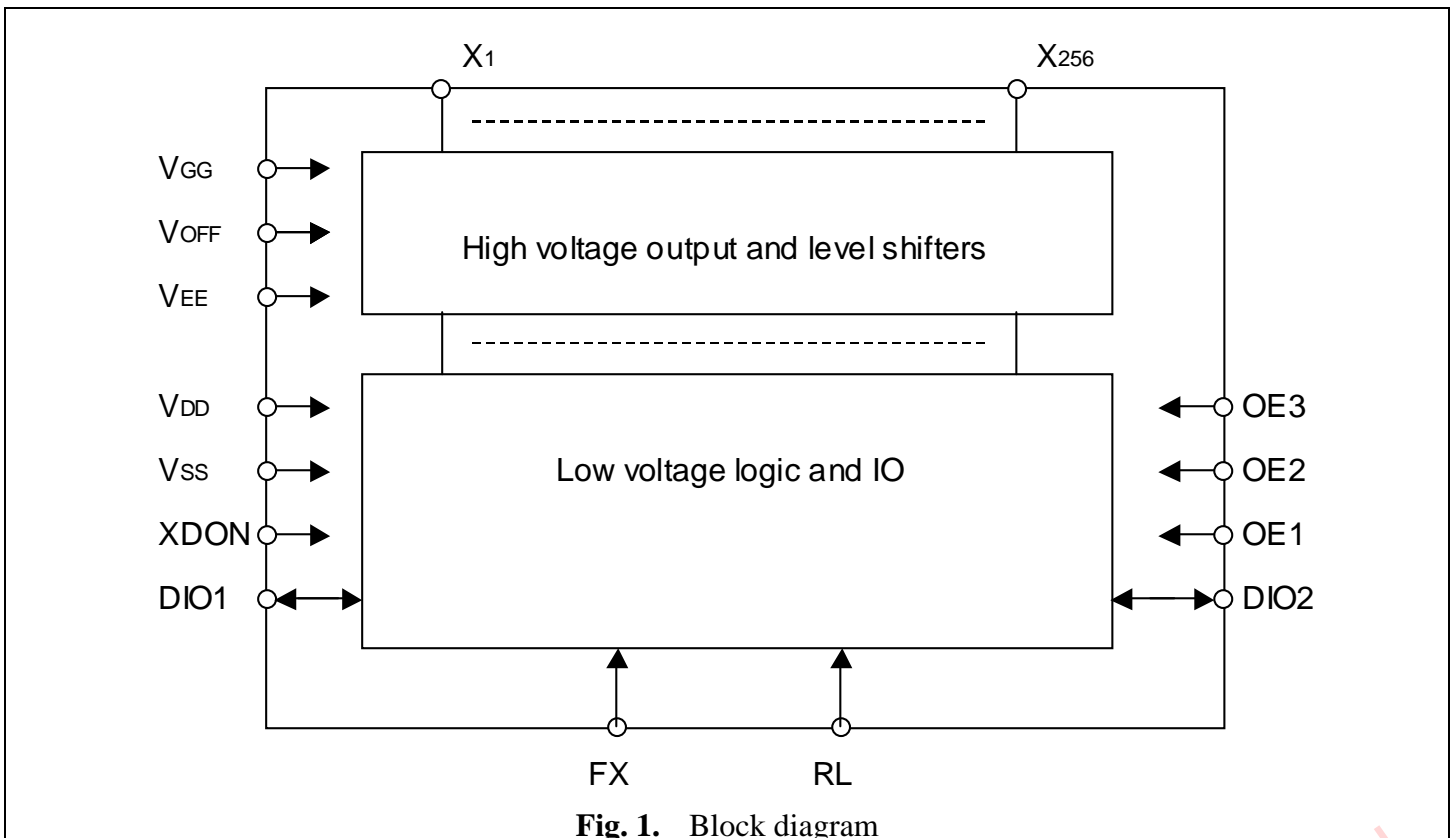
### DESCRIPTION

The EK7304 is a 256-output TFT gate driver IC suitable for driving large/medium scale of TFT LCD panels. Through the use of TCP, it substantially decreases the size of the frame section of LCD module.

### FEATURES

- Output channels: 256 outputs
- Driver operating frequency: max. 1200kHz
- LCD drive voltage: max.  $V_{EE}+43V$
- Driver output levels: two ("L" level is changeable)
- Incorporates bi-directional shift register.
- Supports multi chip operation via output pins.
- Pulse width modulation function.

### BLOCK DIAGRAM



## PINNING INFORMATION

**Table 1. Pin List**

Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name
1	Dummy	44	X154	87	X111	130	X068	173	X041	216	VEE	259	X226
2	X196	45	X153	88	X110	131	X067	174	X040	217	VSS	260	X225
3	X195	46	X152	89	X109	132	X066	175	X039	218	DIO1	261	X224
4	X194	47	X151	90	X108	133	X065	176	X038	219	RL	262	X223
5	X193	48	X150	91	X107	134	X064	177	X037	220	FX	263	X222
6	X192	49	X149	92	X106	135	X063	178	X036	221	OE1	264	X221
7	X191	50	X148	93	X105	136	X062	179	X035	222	OE2	265	X220
8	X190	51	X147	94	X104	137	X061	180	X034	223	OE3	266	X219
9	X189	52	X146	95	X103	138	Dummy	181	X033	224	DIO2	267	X218
10	X188	53	X145	96	X102	139	Dummy	182	X032	225	XDON	268	X217
11	X187	54	X144	97	X101	140	Dummy	183	X031	226	VDD	269	X216
12	X186	55	X143	98	X100	141	Dummy	184	X030	227	VGG	270	X215
13	X185	56	X142	99	X099	142	Dummy	185	X029	228	Dummy	271	X214
14	X184	57	X141	100	X098	143	Dummy	186	X028	229	X256	272	X213
15	X183	58	X140	101	X097	144	Dummy	187	X027	230	X255	273	X212
16	X182	59	X139	102	X096	145	Dummy	188	X026	231	X254	274	X211
17	X181	60	X138	103	X095	146	Dummy	189	X025	232	X253	275	X210
18	X180	61	X137	104	X094	147	Dummy	190	X024	233	X252	276	X209
19	X179	62	X136	105	X093	148	Dummy	191	X023	234	X251	277	X208
20	X178	63	X135	106	X092	149	Dummy	192	X022	235	X250	278	X207
21	X177	64	X134	107	X091	150	Dummy	193	X021	236	X249	279	X206
22	X176	65	X133	108	X090	151	Dummy	194	X020	237	X248	280	X205
23	X175	66	X132	109	X089	152	Dummy	195	X019	238	X247	281	X204
24	X174	67	X131	110	X088	153	Dummy	196	X018	239	X246	282	X203
25	X173	68	X130	111	X087	154	X060	197	X017	240	X245	283	X202
26	X172	69	X129	112	X086	155	X059	198	X016	241	X244	284	X201
27	X171	70	X128	113	X085	156	X058	199	X015	242	X243	285	X200
28	X170	71	X127	114	X084	157	X057	200	X014	243	X242	286	X199
29	X169	72	X126	115	X083	158	X056	201	X013	244	X241	287	X198
30	X168	73	X125	116	X082	159	X055	202	X012	245	X240	288	X197
31	X167	74	X124	117	X081	160	X054	203	X011	246	X239	289	Dummy
32	X166	75	X123	118	X080	161	X053	204	X009	247	X238	290	Dummy
33	X165	76	X122	119	X079	162	X052	205	X008	248	X237	291	Dummy
34	X164	77	X121	120	X078	163	X051	206	X007	249	X236	292	Dummy
35	X163	78	X120	121	X077	164	X050	207	X006	250	X235	293	Dummy
36	X162	79	X119	122	X076	165	X049	208	X005	251	X234	294	Dummy
37	X161	80	X118	123	X075	166	X048	209	X004	252	X233	295	Dummy
38	X160	81	X117	124	X074	167	X047	210	X003	253	X232	296	Dummy
39	X159	82	X116	125	X073	168	X046	211	X002	254	X231	297	Dummy
40	X158	83	X115	126	X072	169	X045	212	X001	255	X230	298	Dummy
41	X157	84	X114	127	X071	170	X044	213	Dummy	256	X229	299	Dummy
42	X156	85	X113	128	X070	171	X043	214	VOFF	257	X228	300	Dummy
43	X155	86	X112	129	X069	172	X042	215	VEE	258	X227	301	Dummy
			X111									302	Dummy
												303	Dummy

**Notes:**

1. With the chip name EM7301 orientated normal the pin 1 is in the upper right corner.
2. Counting is anticlockwise.

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**Table 2 Pin description**

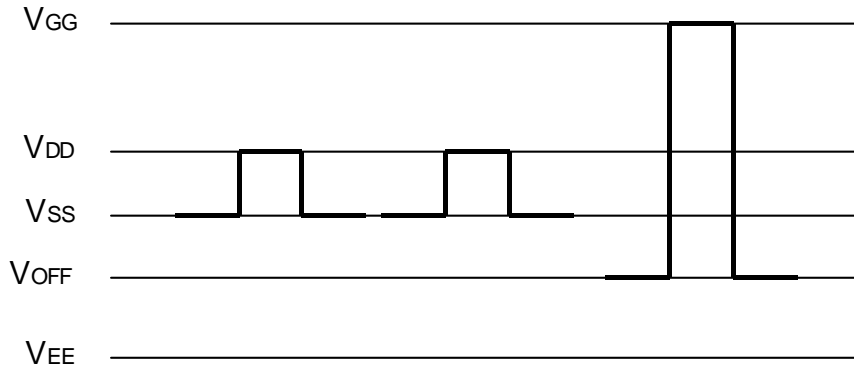
PIN NO	SYMBOL	I/O	Function	DESCRIPTION									
212 to 154 137 to 2 288 to 229	X <sub>001</sub> -X <sub>256</sub>	O	TFT gate driver output	Under the control of the shift register data, OE1 or OE2 or OE3, and DIO1 or DIO2, the driver outputs are V <sub>GG</sub> or V <sub>OFF</sub> and change their value at the rising edge of FX									
214	V <sub>OFF</sub>		Supply	Power supply for TFT driver output low level									
215, 216	V <sub>EE</sub>		Supply	Negative power supply for Level shifters. Chip ground									
217	V <sub>SS</sub>		Supply	Logic ground, Reference of the voltages									
219	RL	I	Shift direction selection signal	RL = "H" : X1 → X256 (Shift left) RL = "L" : X256 → X1 (Shift right)									
218 224	DIO1 DIO2	I/O	Start pulse input and output	<table border="1"> <thead> <tr> <th></th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td>RL = "H"</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>RL = "L"</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>		DIO1	DIO2	RL = "H"	Input	Output	RL = "L"	Output	Input
	DIO1	DIO2											
RL = "H"	Input	Output											
RL = "L"	Output	Input											
225	XDON	I	Negative active input pin	When XDON = "L" then the driver outputs are at the V <sub>GG</sub> level independent of any other input or register value.									
220	FX	I	Shift register clock input	The start pulse is sampled at the rising edge of FX, The carry pulse changes at the falling edge of FX.									
221 222 223	OE1 OE2 OE3	I	Negative active input pin	When OE <sub>N</sub> = "H" then the associated outputs are set to V <sub>OFF</sub> independent of the register data. This function is not synchronized with FX.									
226	V <sub>DD</sub>		Supply	Logic positive power									
227	V <sub>GG</sub>		Supply	High voltage power and TFT driver output high level									

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## FUNCTIONAL DESCRIPTION

### Power supply's

The TFT voltage is relative to the logic ground, it can be a negative voltage value.



**Fig. 2.** Relative position of the different supply voltages

### Shift direction

The input signals OE1,2,3 and the shift data control the value of the outputs ( $X_1$  till  $X_{256}$ ). Their value can be either  $V_{GG}$  or  $V_{OFF}$ .

The signal LR controls the shift direction of the shift register. The shift register takes its value from one of the input/output pins DIO at the rising edge of the clock FX and shifts the value to the other input/output pin DIO where it is presented at the falling edge of FX.

**Table 2. RL shift direction relation**

RL	Start pulse taken from:	Data shift direction	Output pulse given at:
RL="H"	DIO1	$X_1 \rightarrow X_{256}$	DIO2
RL="L"	DIO2	$X_{256} \rightarrow X_1$	DIO1

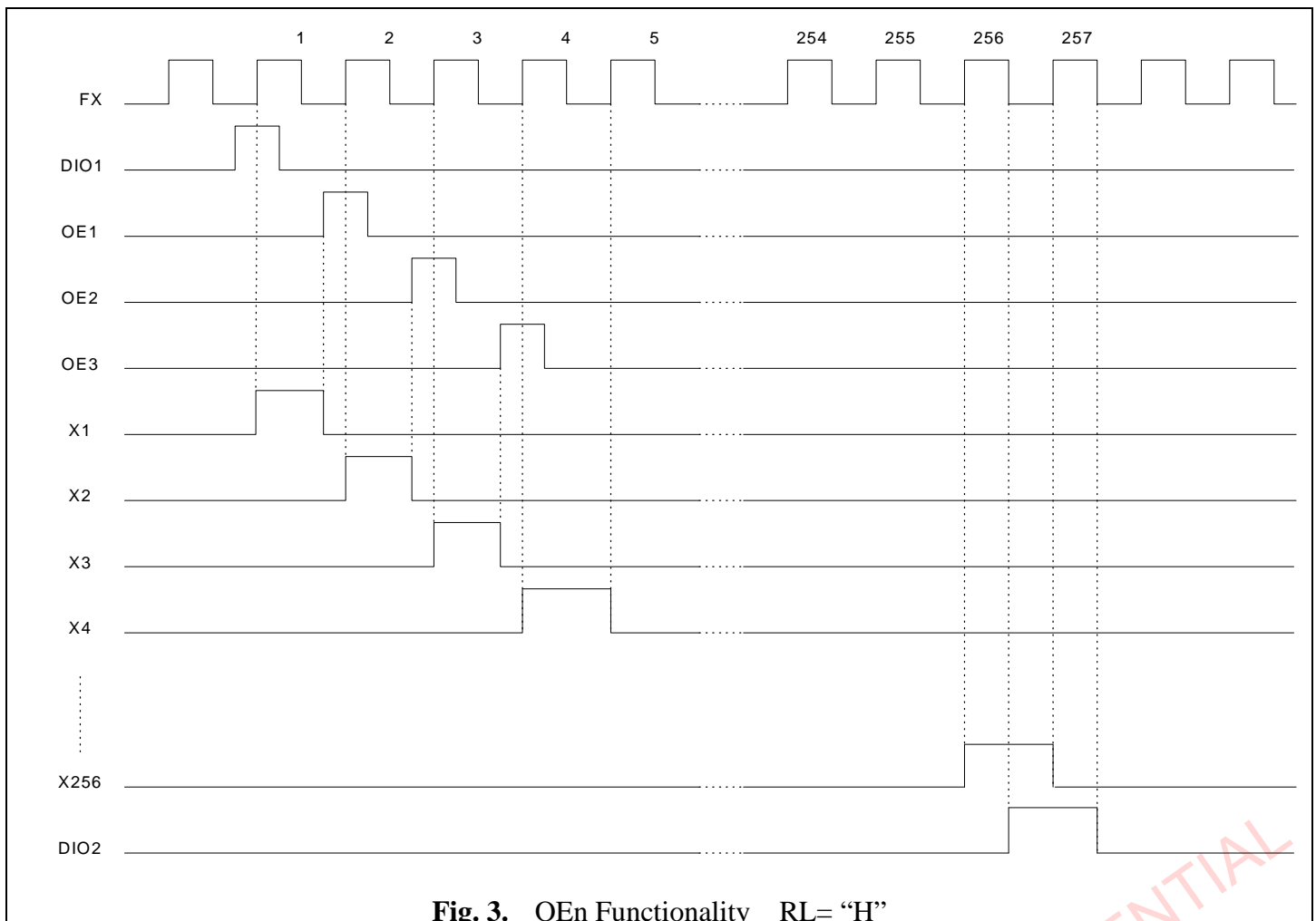
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## OE function

When the OE1, OE2, OE3 inputs are “H” than the outputs are driven to  $V_{OFF}$  regardless of the contents of the shift register. Each of the three inputs drives its own set of outputs. This function is not synchronized with FX. The signal XDON can override this function. In the Table below the relation between each OE1,2,3 and their related outputs is given.

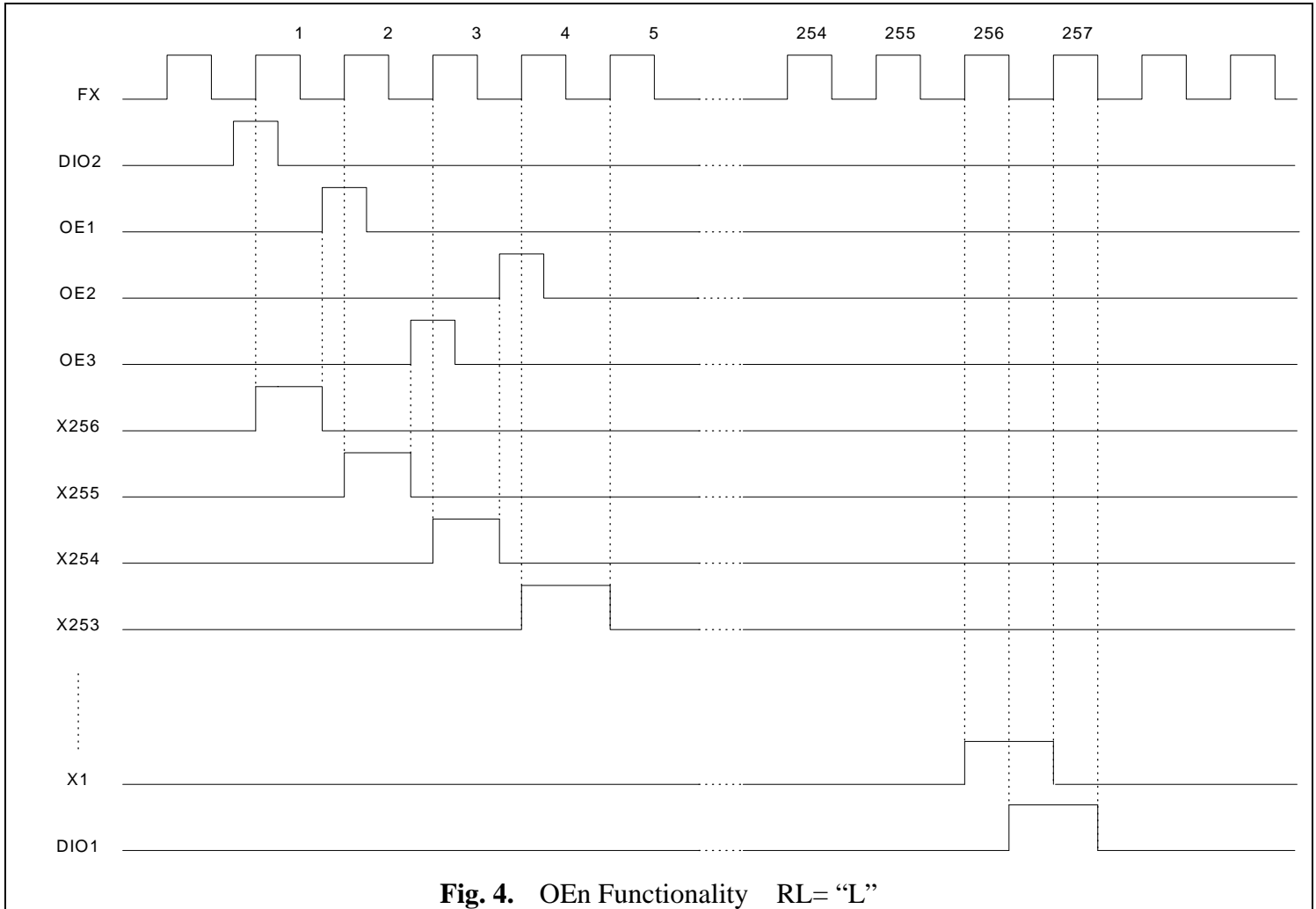
**Table 3. OE1,2,3 to Output relation**

Non-signal input	Symbol	LCD driver outputs
OE1	$X(3i+1) \ i=0\sim85$	$X_1, X_4, X_7, X_{10}, \dots, X_{247}, X_{250}, X_{253}, X_{256}$
OE2	$X(3i+2) \ i=0\sim84$	$X_2, X_5, X_8, X_{11}, \dots, X_{248}, X_{251}, X_{254}$
OE3	$X(3i+3) \ i=0\sim84$	$X_3, X_6, X_9, X_{12}, \dots, X_{249}, X_{252}, X_{255}$



**Fig. 3. OE<sub>n</sub> Functionality RL= "H"**

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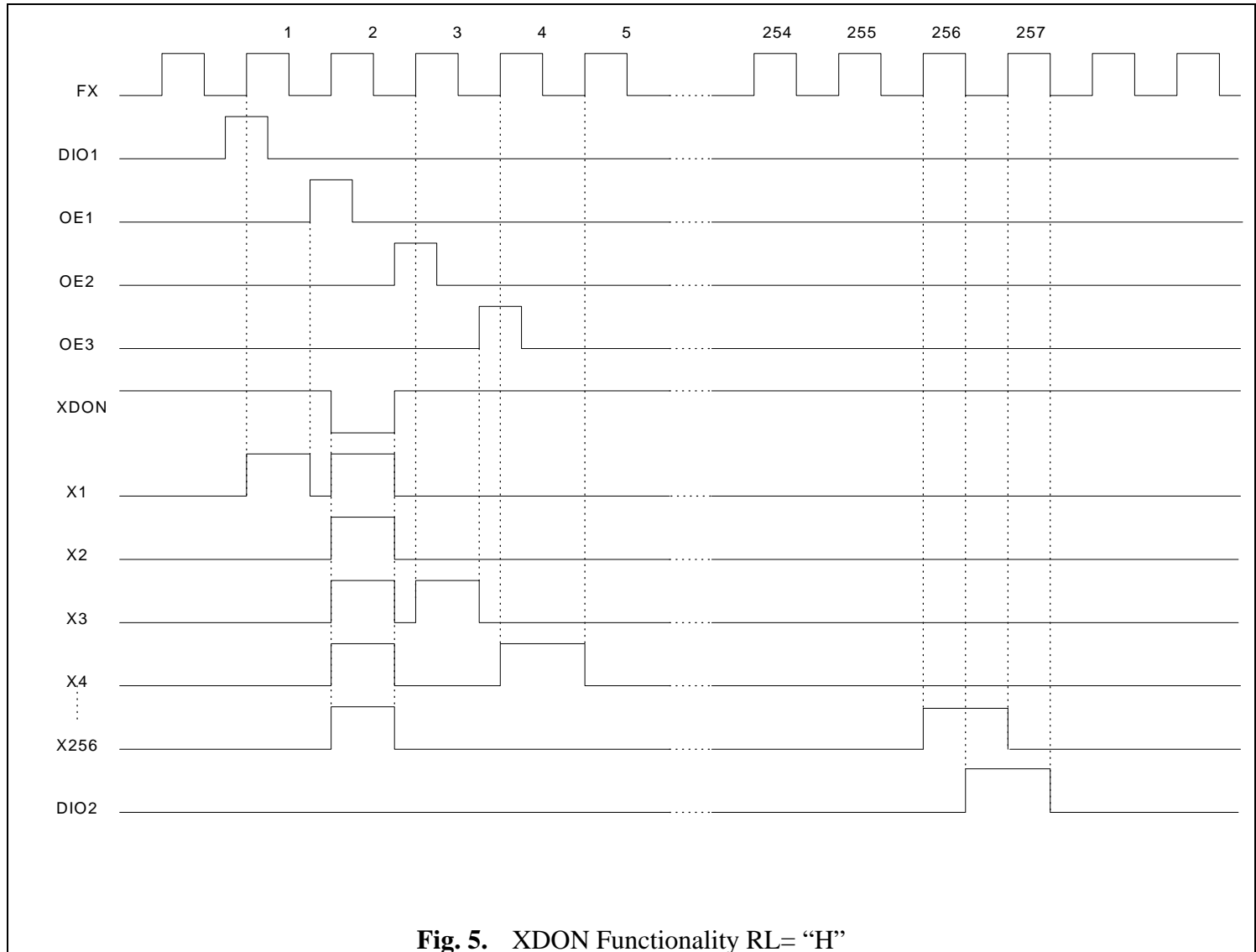
**Fig. 4.** OEn Functionality RL= "L"

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## XDON function

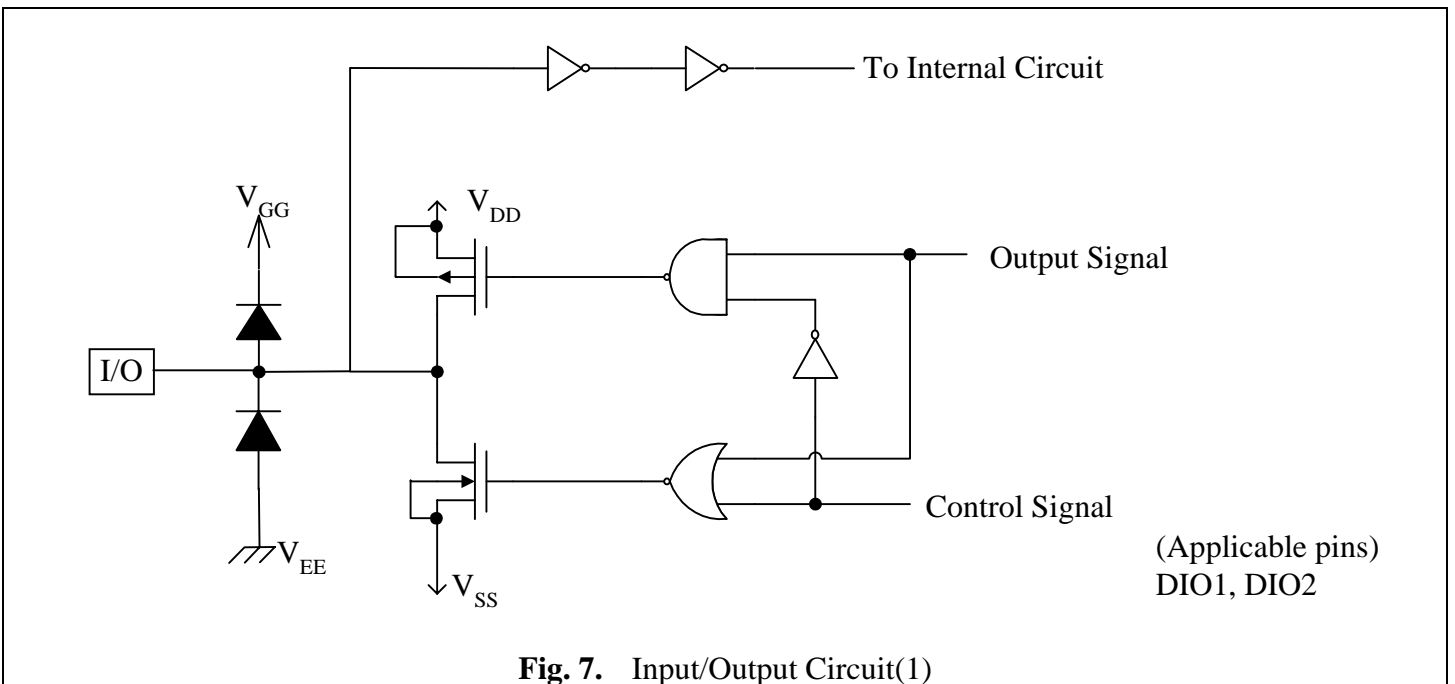
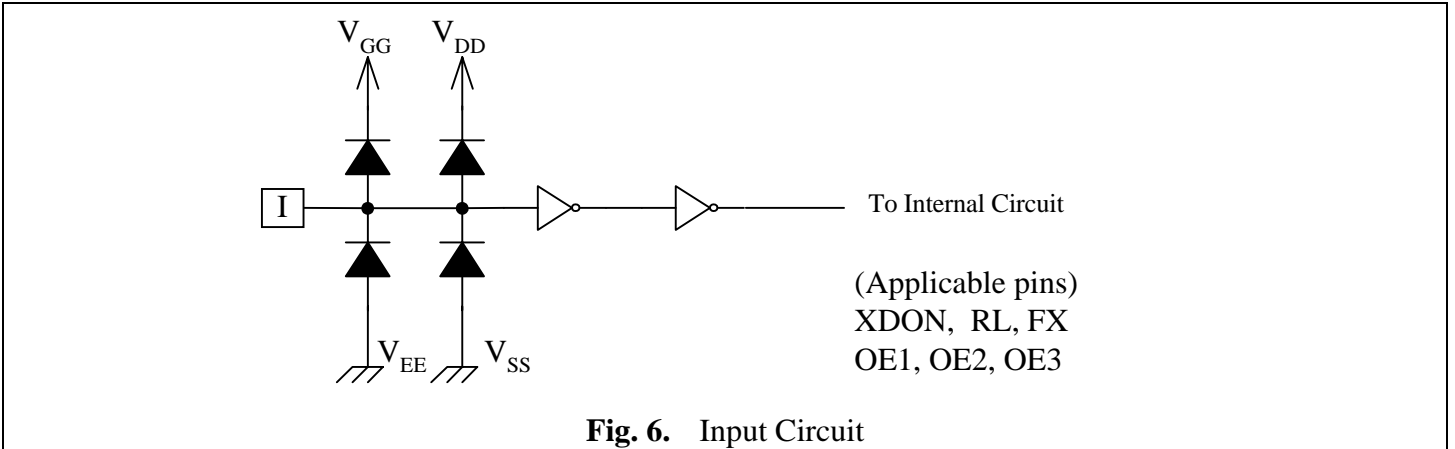
When XDON input is “L” then all outputs are driven to the  $V_{GG}$  level. This function is overriding all other inputs. With this input all TFT gates are set to high to enable a display off function. This function is not synchronized with FX.



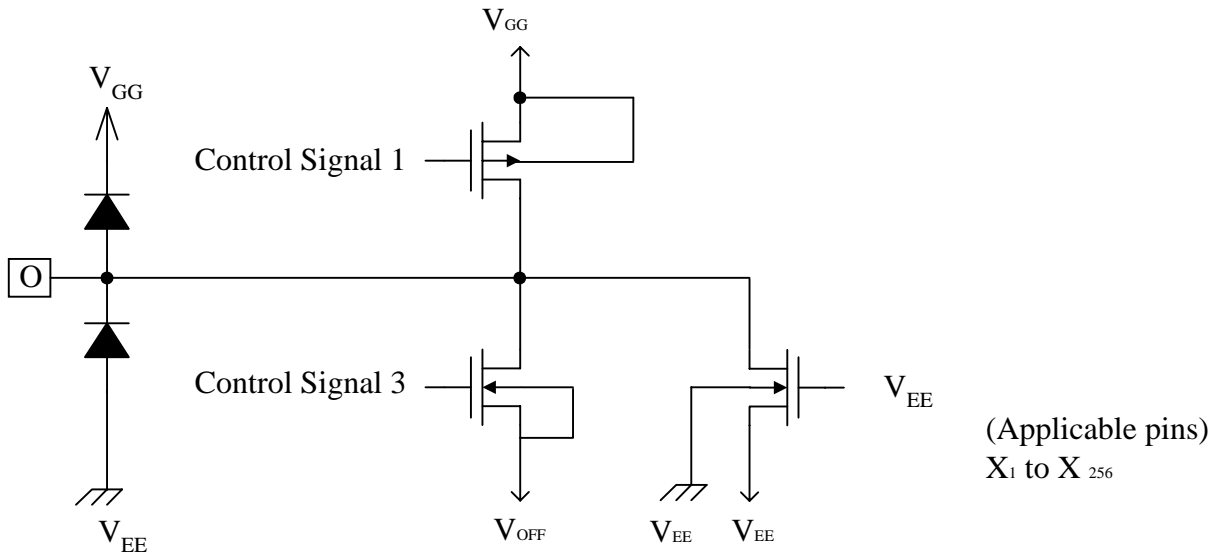
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## CIRCUIT DIAGRAMS

### Input/Output Circuit



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**Fig. 8.** TFT driver circuit

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## PRECAUTIONS

### Precaution when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.

## ABSOLUTE MAXIMUM RATINGS

**Table 4. Absolute maximum Ratings**

In accordance with the Absolute Maximum Ratings System (IEC 134); See notes 1 and 2

Parameter	Symbol	Applicable Pins	Ratings	Unit	NOTE
Supply voltage(1)	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>SS</sub> -0.3 to +7.0	V	1, 2
Supply voltage(2)	V <sub>GG</sub>	V <sub>GG</sub>	-0.3 to +45.0	V	
	V <sub>EE</sub>	V <sub>EE</sub>	V <sub>GG</sub> -45 to V <sub>GG</sub> +0.3	V	
	V <sub>OFF</sub>	V <sub>OFF</sub>	V <sub>EE</sub> -0.3 to V <sub>GG</sub> +0.3	V	
	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>EE</sub> -0.3 to V <sub>GG</sub> +0.3	V	
	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>EE</sub> -0.3 to V <sub>GG</sub> +0.3	V	
Input voltage	V <sub>I</sub>	EO1, EO2, EO3, DIO1 DIO2, RL, FX, XDON	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3 V <sub>EE</sub> -0.3 to V <sub>GG</sub> +0.3	V	
Storage temperature	T <sub>stg</sub>		-45 to +125	°C	

### Notes:

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device
2. Parameters are valid over operating temperature range unless otherwise specified.

## RECOMMENDED OPERATING CONDITIONS

**Table 5. Recommended operating conditions**

Parameter	Symbol	Applicable pins	Min.	Typ.	Max.	Unit	NOTE
Supply voltage(1)	V <sub>DD</sub>	V <sub>DD</sub>	+2.5		+5.5	V	1, 2
Supply voltage(2)	V <sub>GG</sub>	V <sub>GG</sub>	+10.0		+42.0	V	
Supply voltage(2)	V <sub>EE</sub>	V <sub>EE</sub>	-25		-5	V	
Operating temperature	T <sub>OPR</sub>		-20		+75	°C	

### Notes:

1. All voltages are with respect to V<sub>SS</sub> unless otherwise noted (0 V).
2. Ensure that voltages are set such that V<sub>EE</sub> ≤ V<sub>SS</sub> < V<sub>DD</sub> < V<sub>GG</sub>. and V<sub>EE</sub> ≤ V<sub>OFF</sub> < V<sub>GG</sub>

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## ELECTRICAL CHARACTERISTICS

**Table 6. DC Characteristics**

( $V_{SS}=0$  V,  $V_{DD}=+2.5$ V to  $+5.5$ V,  $V_{GG}=+15.0$  to  $+42.0$  V,  $T_{OPR}=-20$  to  $+75^{\circ}$ C)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit	Note	
Operating Supply Current	I <sub>DD</sub>	f <sub>FX</sub> =15.7kHz f <sub>SL</sub> =60Hz V <sub>DD</sub> =3.3V V <sub>EE</sub> =-15V V <sub>GG</sub> =15V Output with no load	V <sub>DD</sub>			800	μA		
Operating Supply Current	I <sub>GG</sub>		V <sub>GG</sub>			300	μA		
Standby quiescent supply current	I <sub>DS</sub>	Standby V <sub>DD</sub> =3.3V V <sub>EE</sub> =-15V V <sub>GG</sub> =15V	V <sub>DD</sub>			600	μA		
Standby quiescent Supply Current	I <sub>GS</sub>		V <sub>GG</sub>			100	μA		
<b>Input pin</b>									
H input voltage	V <sub>IH1</sub>		RL,FX, OE1~3, XDON	0.8xV <sub>DD</sub>		V <sub>DD</sub>	V		
L input voltage	V <sub>IL1</sub>			0		0.2xV <sub>DD</sub>	V		
Input leakage current	V <sub>LI1</sub>			-10		10	μA		
<b>Output pin</b>									
H input voltage	V <sub>IH3</sub>		DIO1, DIO2	0.8xV <sub>DD</sub>		V <sub>DD</sub>	V		
L input voltage	V <sub>IL3</sub>					0.2xV <sub>DD</sub>	V		
H output voltage	V <sub>OH</sub>	I <sub>O</sub> = -100 μA			V <sub>DD</sub> -0.4			V	
L output voltage	V <sub>OL</sub>	I <sub>O</sub> = 100 μA					0.4	V	
<b>Liquid crystal driving voltage input pin</b>									
Input leakage current	V <sub>LI2</sub>		V <sub>OFF</sub>	-100		100	μA		
<b>Liquid crystal driving output pin</b>									
Output leakage current	V <sub>LO1</sub>		X1~X256	-50		50	μA		
Output ON resistance	RON-V <sub>GG</sub>	V <sub>GG</sub> =15V V <sub>EE</sub> =-15V V <sub>OM</sub> =V <sub>GG</sub> -0.5V V <sub>OM</sub> is X1~X256				600	1000	Ω	
	RON-V <sub>OFF</sub>	V <sub>GG</sub> =15V V <sub>EE</sub> =-15V V <sub>OFF</sub> =-10V V <sub>OM</sub> =V <sub>OFF</sub> +0.5V V <sub>OM</sub> is X1~X256			600	1000	Ω		

## AC Characteristics

( $V_{SS}=0\text{ V}$ ,  $V_{DD}=+2.5\text{V to }+5.5\text{V}$ ,  $V_{GG}-V_{EE}=+30.0\text{ to }+42.0\text{ V}$ ,  $T_{OPR}=-20\text{ to }+75^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock period	tFX		833			ns
Pulse width of clock H level	tWH		350			ns
Pulse width of clock L level	tWL		350			ns
DIO data set up time	tsu		50			ns
DIO data hold time	th		350			ns
DIO output delay time	tpd1	CL=50pF			300	ns
Xn output delay time	tpd2	CL=300pF			800	ns

## Timing Chart

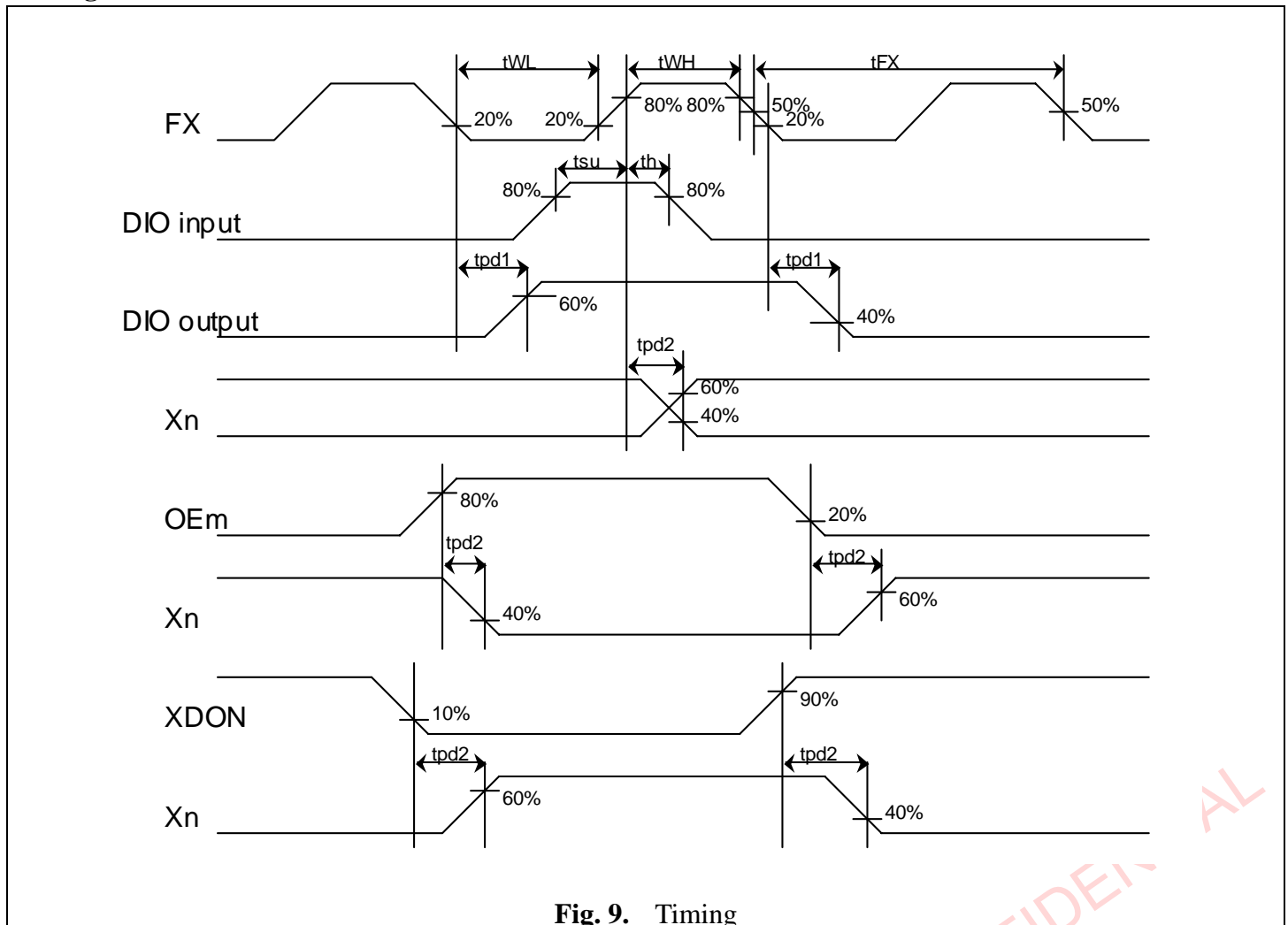


Fig. 9. Timing

## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

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