SDRAMs for the PC-100 Standard

MB81F16422B/822B/1622B
MB81F64442B/842B/1642B
MB81F64442C/842C/1642C
MB81F64442D/842D/1642D

16 M-bit and 64 M-bit SDRAMs feature low power consumption, high operating speed, full compatibility with PC-100 specifications, and retain compatibility with existing devices

Features

- ***Compatible with PC-100 specifications***
- ***PC-66 compatible DRAMs with reduced access time***
- ***Lower power consumption***
- ***JEDEC standard packages and pin assignments***

Overview

The supply and demand of DRAM continues to expand, radically affecting the memory marketplace. Specifically, DRAM devices are used not only in personal computers, workstations, and printers, but also in a variety of electronic devices, including DVDs, set-top processing boxes, IRDs, digital TV, game devices, portable devices, car navigation, and factory automation equipment. However, the predominate application for the DRAM industry is the personal computer, which accounts for more than 70% of all DRAM uses. Complete compatibility with the requirements of the key application, the personal computer, is an essential requirement for survival in the DRAM industry.

Photo 1. MB81F16822B External View

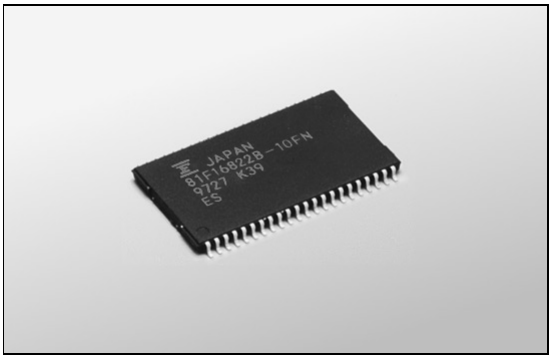


Photo 2. MB81F16822B Chip

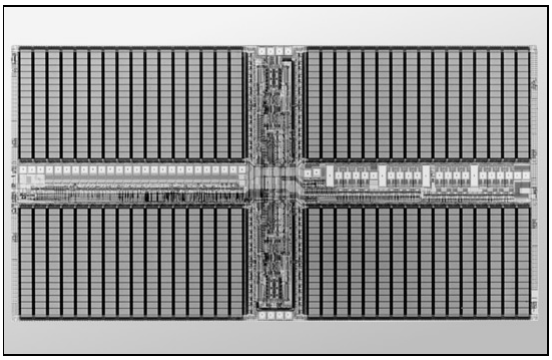
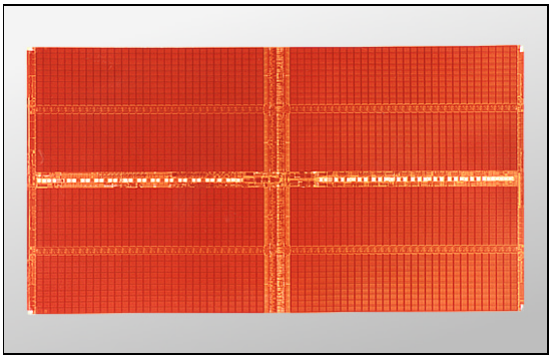


Photo 3. MB81F164442B/842B/1642B Chip



At present most DRAMs used in personal computer microprocessors operate on a memory bus frequency of 66 MHz (PC-66). The next level of processors, represented by the PC-100, will operate at memory bus frequencies around 100 MHz.

FUJITSU is mass-producing 16 M-bit and 64 M-bit SDRAMs that are fully compatible with the PC-66 specifications required by current personal computers. We are beginning to mass produce 16 M-bit and 64 M-bit SDRAMs fully compatible with the PC-100 specifications that the industry is moving toward.

The personal computer industry continually demands higher speeds and lower power consumption. The DRAM that meets the capabilities demanded by the personal computer can be expected to spread to a wide variety of other applications.

What Is PC-100?

The Intel PC-100 specifications are shown in Table 1 on p. xx. They include four levels of specifications for the following cycles:

- CAS latency: Clock pulses from read command input to data output.
- t_{RCD}: The interval from active command input (row address selection) to read or write command input (column address selection).
- t_{RP}: The interval from precharge command input to the next command input.

At the 2-cycle/2-cycle/2-cycle level (abbreviated as 2-2-2), a device operating at the same 100-MHz speed as a current PC-66 device will output read data one cycle faster. The device also will be faster, with access time from the clock pulse reduced from 9 ns to 6 ns.

"... access time from the clock pulse reduced from 9 ns to 6 ns."

The PC-100 standard will have clamping diodes inside the SDRAM at the CLK, CS, DQM, and CKE pins. At these pins, current flow will start at V_{CC} + 0.9V on the V_{CC} side, and V_{SS} – 0.7V on the V_{SS} side. This will provide full protection against undershoot and overshoot produced when multiple devices are used in combination.

Figure 1. Intel CPU/Chip Set Development Timeline

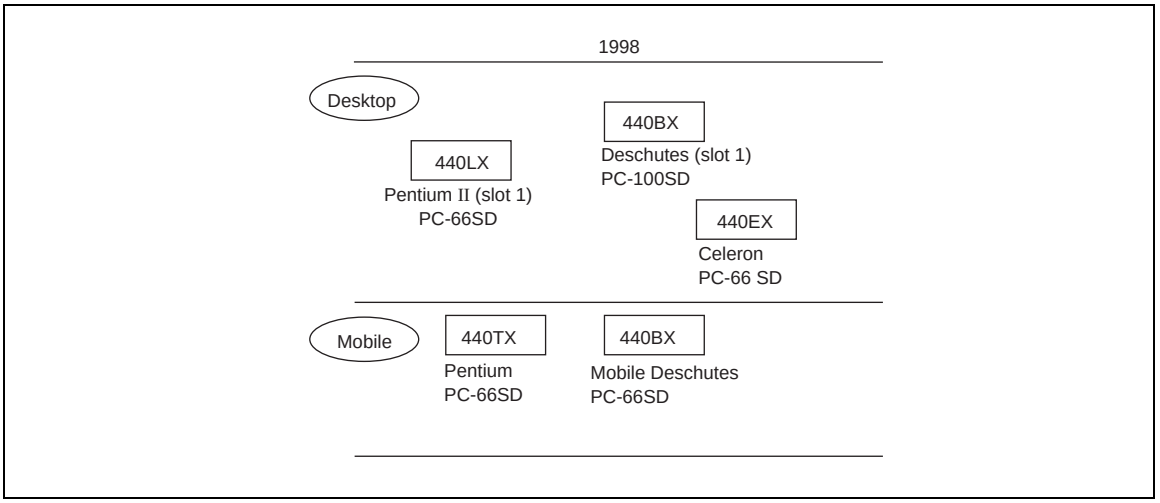


Table 1. Intel PC-100 Specifications

CAS Latency	t_{RCD}	t_{RP}	Abbreviation
3 Cycle	3 Cycle	3 Cycle	3-3-3
3 Cycle	2 Cycle	2 Cycle	3-2-2
3 Cycle	2 Cycle	3 Cycle	3-2-3
2 Cycle	2 Cycle	2 Cycle	2-2-2

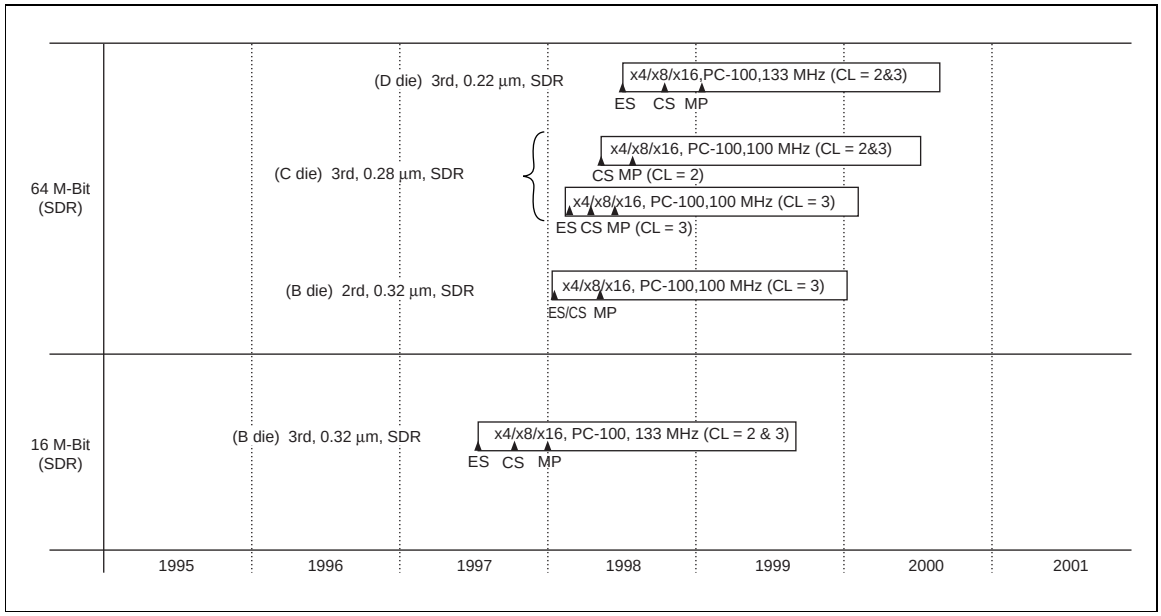
The PC-100 CPU and Chip Set

Figure 1 shows a development timeline of the CPU and chip set announced by Intel®. In the desktop field, the chip set 440LX with the Intel Pentium® II has a memory bus frequency of 66 MHz, and the 440BX with the next-generation Deschutes CPU has a frequency of 100 MHz. In the mobile field, a new chip set will be developed next year, and the memory bus frequency is likely to be 100 MHz.

FUJITSU Product Development

Figure 2 graphs the development plan for FUJITSU SDRAM products. The 16 M-bit DRAM 2-2-2 and the 64 M-bit 3-2-2 are already in mass production. Commercial samples of the 64 M-bit 2-2-2 have been delivered and preparations for mass production are in progress. Design work has been completed for a still faster product capable of operating at 133 MHz (CAS latency = 3), and mass production is scheduled for the beginning of 1999.

Figure 2. FUJITSU PC-100 SDRAM Development Timeline



PC-100 16 M-Bit SDRAM Features

The MB81F16422B (x4 model)/822B (x8 model) is a 2-2-2 product capable of operating at 100 MHz with CAS latency of 2. The MB81F161622B (x16 model) is an ultra-high-speed device with CAS latency of 3, available in two versions: model 80 with 125 MHz operating capability and model 75 with 133 MHz operating capability. These devices have been released in response to strong demand from graphic memory applications and have the following features:

- Fully compatible with JEDEC specifications
- Power supply voltage 3.3V ±0.3V, I/O levels LVTTL compatible
- I/O configuration (four versions available, depending on minimum operating clock frequency)
- Maximum frequency
  - MB81F16422B-102: x4 model Maximum frequency 100 MHz (CAS latency 2)
  - MB81F16822B-102: x8 model Maximum frequency 100 MHz (CAS latency 2)
  - MB81F161622B-75: x16 model Maximum frequency 133 MHz (CAS latency 3)
  - MB81F161622B-80: x16 model Maximum frequency 125 MHz (CAS latency 3)
- Verified compatible with previous devices
- Low power circuit technology for one-fifth the power demand of previous devices
- Packages
  - MB81F16422B/822B: TSOP II-44 (400 mil)
  - MB81F161622B: TSOP II-50 (400 mil)
- JEDEC standard pin assignments

Photo 4. MB81F64442C/842C/1642C External View

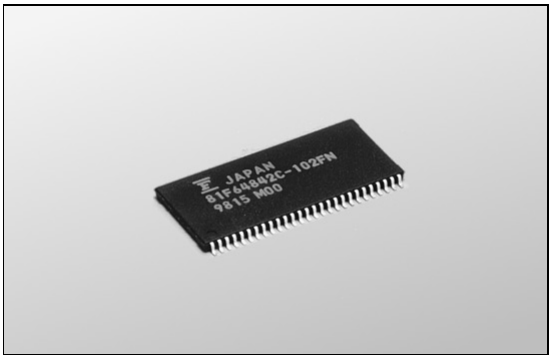


Photo 5. MB81F64442C/842C/1642C Chip

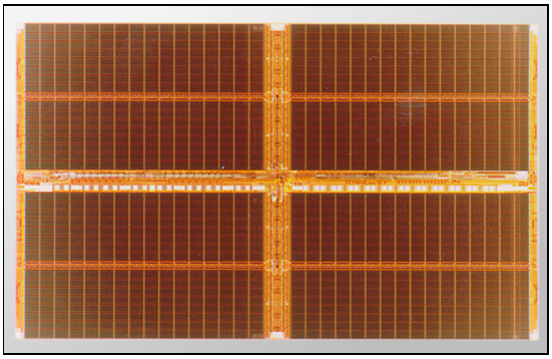
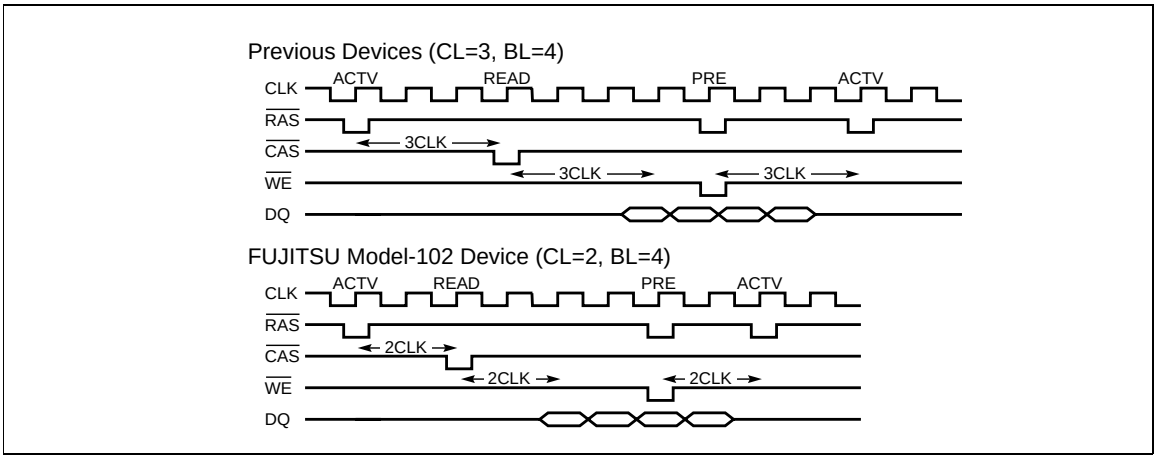


Figure 3. Basic Read Operation Timing Block Chart



PC-100 64 M-Bit SDRAM Features

The capacity of future SDRAMs is expected to expand substantially. Now that the appearance of the Windows® 98 operating system has increased base memory size greatly from the current 32 megabyte to 64 megabyte, the majority of computer products is expected to change from 16 M-bit models to 64 M-bit models. FUJITSU is therefore providing three models of SDRAM: the MB81F64442B/842B/1642B, MB81F64442C/842C/1642C, and MB81F64442D/842D/1642D.

The MB81F64442B/842B/1642B design is based on a PC-66 device and is intended to respond to initial demand in the PC-100 market. This SDRAM has 3-2-2 specifications and is already in mass production.

The MB81F64442C/842C/1642C has 2-2-2 specifications. The MB81F64442D/842D/1642D has 2-2-2 specifications with accelerated operating speeds and supports 133 MHz (CAS latency 3) operation. Each is available in the following models, depending on minimum clock frequencies:

- MB81F64442B/842B/1642B: 2 versions, model 10 and 103
- MB81F64442C/842C/1642C: 2 versions, model 103 and 102
- MB81F64442D/842D/1642D: 3 versions, model 75, 102, and 10

The model 10 versions are PC-66 products. The Model 103 versions are compatible with PC-100 (3-2-2) specifications, and the model 102 products are speed versions compatible with PC-100 (2-2-2) specifications. The model 75 version is an ultra-high-speed version operating at 133 MHz with CAS latency of 3. In addition to the above speeds, these 64 M-bit SDRAMs have the following characteristics:

- Fully compatible with JEDEC specifications
- Supply voltage 3.3V ± 0.3V, I/O levels LVTTL compatible
- Verified compatible with previous devices
- Packages: all versions TSOP II-54 (400 mil); PC-66 and PC-100 versions sealed in the same package, compatibility completely verified
- JEDEC standard pin assignments

Product Functions

The PC-100 SDRAM can operate in systems with memory bus frequencies of 100 MHz.

The model 102 versions are constructed to operate at even higher frequencies.

Figure 3 shows the timing block diagram of basic read operations in a model operating at 100 MHz with CAS latency of 2, in comparison with existing products.

The new SDRAM product is able to substantially reduce the number of cycles required for a basic read operation from ten cycles to eight cycles, in comparison with previous devices. As with earlier devices, each model has mode register settings providing the following mode selections:

". . . substantially reduce the number of cycles required for a basic read operation from ten cycles to eight cycles . . ."

- CAS latency: Select 2 or 3
- Burst length: Select 1/2/4/8 or full-column burst
- Burst type: Select sequential or interleave burst address increment method

Device Characteristics

Table 2 lists the principal product characteristics. ◆

Endnotes

Windows is a registered trademark of Microsoft Corporation.

Intel and Pentium are registered trademarks of Intel Corporation.

Table 2. SDRAM Principal Specifications

Item			16 M-Bit Models			64 M-Bit Models						
Model Name			MB81F16422B /822B	MB81F161622B		MB81F64442B/822B/ 1622B		MB81F64442C/822C/ 1622C		MB81F64442D/822D/1622D		
Speed Version			–102	–75	–80	–103	–10	–102	–103	–75	–102	–10
Device Options (CL -t_{RCD} -t_{RP}) [cycle]			2-2-2	3-3-3		3-2-2	3-3-3	2-2-2	3-2-2	3-3-3	2-2-2	3-3-3
Clock Frequency [MHz]			100	133*	125*	100*	100*	100	100*	133*	100	100*
Clock t_{CK} [ns]			10	7.5*	8*	10*	10*	10	10*	7.5*	10	10*
RAS Cycle t_{BC} [ns]			70	67.5	72	70	80	70	70	66	70	80
RAS-CAS Delay Time t_{RCD} [ns]			20	22.5	24	20	30	20	20	22	20	30
RAS Precharge Time t_{RP} [ns]			20	22.5	24	20	30	20	20	22	20	30
From Clock to Output Data Valid		t_{AC2} (CL=2) [ns]	6	7	7	8	8	6	8	7	6	8
		t_{AC2} (CL=3) [ns]	6	6	6	6	6	6	6	6	6	6
Power Supply Current	Operation (2-bank) ICC1D [mA]		140	170	160	220	180	190		210	180	160
	Standby ICC3N [mA]		40	60	55	30		25		30	25	25
	Burst ICC4 [mA]		95	120	110	140		85		140	120	120
	Power Saving ICC2P [mA]		0.4			3 (extra power version) 2 (normal power version) 1 (low power version)		2 (normal power version) 1 (low power version)		1		
	Self Refreshing ICC6 [mA]		0.4			2 (extra power version) 1 (normal power version) 0.5 (low power version)		1 (normal power version) 0.5 (low power version)		1		

*CAS Latency = 3