

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89560A Series

MB89567A/567AC/P568/PV560

■ DESCRIPTION

The MB89560A series has been developed as a general-purpose version of the F²MC*¹-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as I²C interface*², timers, 2 ch 8-bit PWM timers, 8/16-bit timer, 21-bit timebase timer, 8-bit PWC timer, 17-bit Watch prescaler, Watch-dog timer, High speed UART, 8-bit SIO, UART/SIO, LCD controller/driver (optional booster), Two type Programmable Pulse Generators (PPG), an A/D converter, and external interrupt.

*1 : F²MC stands for FUJITSU Flexible Microcontroller.

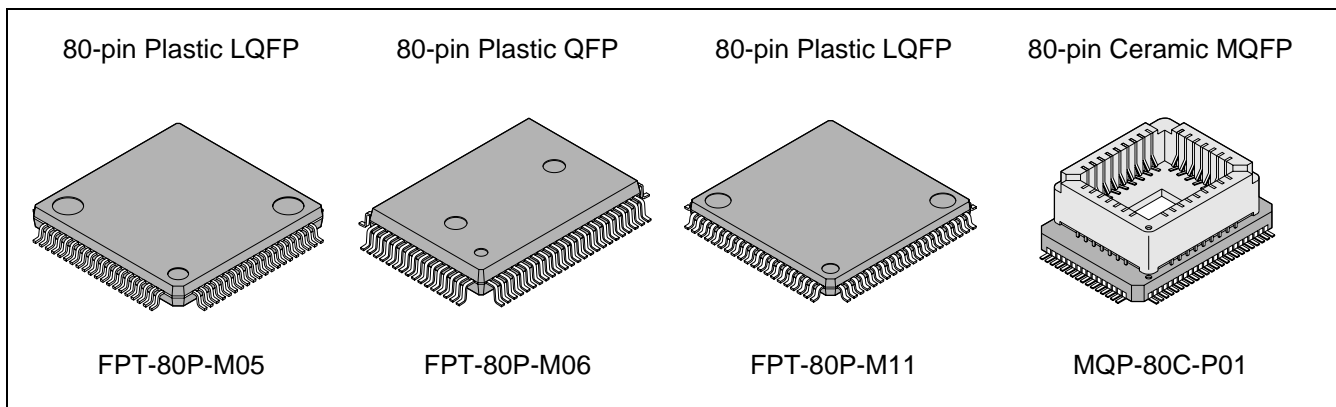
*2 : I²C of this product is complied to Intel Corp. System Management Bus Rev. 1.0 specification and to the Philips I²C specification.

■ FEATURES

- F²MC-8L family CPU core
- Low-voltage operation (when an A/D converter is not used)
- Low current consumption (applicable to the dual-clock system)
- Minimum execution time: 0.32 μs at 12.5 MHz /3.5 V to 5.5 V

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■ PACKAGES



MB89560A Series

(Continued)

- I²C interface circuit
- LCD controller/driver: 24 segments x 4 commons (Max 96 pixels, duty LCD mode and Static LCD mode)
- LCD booster function (option)
- Wild register (Max 6 different address locations)
- 10-bit A/D converter: 8 channels
- Three types of Serial Interface:
 - High Speed UART (Transfer rate from 300 bps to 192000 bps /10 MHz main clock)
 - 8-bit Serial I/O (SIO)
 - UART/SIO
- Two type of Programmable Pulse Generator(PPG): 6-bit PPG and 12-bit PPG
- Six types of timer
 - 8-bit PWM 2 channels timers
 - 8/16-bit timer/counter (8 bits x 2 channels or 16 bits x 1 channel)
 - 21-bit timebase timer
 - 8-bit PWC timer operation
 - 17-bit Watch prescaler
 - Watch-dog timer
- I/O ports: Max 50 channels
- External interrupt 1: 8 channels
- External interrupt 2 (wake-up function): 4 channels
- Low-power consumption modes (stop mode, sleep mode, and watch mode)
- LQFP-80 and QFP-80 package
- CMOS technology

MB89560A Series

■ PRODUCT LINEUP

Part number	MB89567A	MB89567AC	MB89P568	MB89PV560
Classification	Mass production products (mask ROM products)		OTP	Piggy-back
ROM size	32 K x 8-bit (internal mask ROM)		48 K x 8-bit (internal PROM)	56 K x 8-bit (external ROM)
RAM size	1 K x 8-bit			1 K x 8-bit
CPU functions	Number of instructions : 136 Instruction bit length : 8-bit Instruction length : 1 to 3 bytes Data bit length : 1-, 8-, 16-bit Minimum execution time : 0.32 μ s/12.5 MHz Minimum interrupt processing time : 2.88 μ s/12.5 MHz			
Ports	General-purpose I/O ports (N-channel open drain): 20 pins (2 shared with I ² C inputs, 16 shared with LCD, 2 shared with other resources) General-purpose I/O ports (CMOS) : 30 pins (shared with resources) Total : 50 pins			
21-bit timebase timer	21-bit Interrupt cycle: $(2^{13}, 2^{15}, 2^{18} \text{ or } 2^{22})/F_{CH}^{*7}$			
Watchdog timer	Reset generate cycle: Min $2^{21}/F_{CH}^{*7}$ for main clock, Min $2^{14}/F_{CL}^{*7}$ for sub clock			
Watch prescaler	17-bit Interrupt cycle: 31.25 ms, 0.25 s, 0.50 s, 1.00 s, 2.00 s, 4.00 s/32.768 kHz for subclock			
8/16-bit timer/counter	Can be operated either as a 2-channel 8-bit timer/counter (Timer 1 and Timer 2, each with its own independent operating clock cycle), or as one 16-bit timer/counter In Timer 1 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capable			
8-bit PWM 2 ch timer	8-bit interval timer operation (square wave output capable, operating clock cycle: 1 t_{inst} , 8 t_{inst} , 16 t_{inst} , 64 t_{inst}) 8-bit resolution PWM operation (conversion cycle: 128 x 1 t_{inst} to 256 x 64 t_{inst}) 8/16-bit timer/counter output for counter clock selectability			
PWC timer	8-bit timer operation (count clock cycle: 1 t_{inst} , 4 t_{inst} , 32 t_{inst}) 8-bit reload timer operation (toggle output possible, operating clock cycle: 1 to 32 t_{inst}) 8-bit pulse width measurement (continuous measurement possible: H-width, L-width, rising edge to rising edge, falling edge to falling edge, and rising edge to falling edge)			
10-bit A/D converter *2	10-bit resolution x 8 channels A/D conversion function (conversion time: 60 t_{inst}) Continuous activation by an 8/16-bit timer/counter output or a timebase timer output capable.			
6-bit PPG	Internal 6-bit counter Pulse width and cycle are program selectable			
12-bit PPG	Internal 12-bit counter Pulse width and cycle are program selectable			

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MB89560A Series

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Part number Parameter	MB89567A	MB89567AC	MB89P568	MB89PV560
I ² C interface*4	Not Available		1 channel	
High speed UART	Transfer data length: 4-, 6-, 7-, 8-bit Transfer rate (300 bps to 192000 bps /9.216 MHz main clock) support sub-clock mode			
UART/SIO	Transfer data length: 7-, 8-bit for UART, 8-bit for SIO Transfer rate (1201 bps to 78125 bps / 10 MHz main clock) support sub-clock mode			
8-bit serial I/O	8-bit, LSB first/MSB first selectability Transfer clocks (one external shift clock, three internal shift clocks: 2 t _{inst} , 8 t _{inst} , 32 t _{inst}) *5			
LCD	Common output: 4 (Max) Segment output: 24 (Max) LCD driving power (bias) pins: 4 LCD display RAM size: 12 bytes (24 × 4 bits, Max 96 pixels) Duty LCD mode and Static LCD mode Booster for LCD driving: option*1 Dividing resistor for LCD driving: option			
Wild register	Maximum of 6-byte data can be assigned in 6 different address. Used to replace any data in the ROM when specific address and data are assigned in Wild register. Wild register can be set up by using different communication methods through the device.			
External interrupt 1 (wake-up function)	8 independent channels (interrupt vector, request flag, request output enable) Edge selectability (rising/falling) Used also for wake-up from stop/sleep mode. (edge detection is also permitted in stop mode.)			
External interrupt 2 (wake-up function)	4 channels ("L" level interrupts, independent input enable). Used also for wake-up from stop/sleep mode. (Low-level detection is also permitted in stop mode.)			
Standby mode	Sub clock mode, sleep mode, stop mode and clock mode			
Process	CMOS			
Operating voltage *6	2.2 V to 5.5 V		2.7 V to 5.5 V	2.7 V to 5.5 V*3

*1 : When booster is used, the bias is reduced by 1/3. It can be selected by mask option.

*2 : Voltage varies with product.

*3 : When external ROM is used, EPROM: MBM27C512-20 should be used, the operating voltage: 4.5 V to 5.5 V.

*4 : I²C is complied to Intel Corp. System Management Bus Rev. 1.0 specification and to the Philips I²C specification.

*5 : 1 t_{inst} = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock if main clock mode is selected, or 1/2 of the subclock if subclock mode is selected.

*6 : Varies with conditions such as the operating frequency. (See "ELECTRICAL CHARACTERISTICS.")

*7 : F_{CH} : main clock source oscillation, F_{CL} : sub clock source oscillation

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89567A MB89567AC	MB89P568-101 MB89P568-102	MB89PV560-101 MB89PV560-102
FPT-80P-M05	○	○	×
FPT-80P-M06	○	○	×
FPT-80P-M11	○	○	×
MQP-80C-P01	×	×	○

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTPROM (one-time PROM) products, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- For the MB89PV560, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the one-time PROM product is greater than that for the mask ROM product. However, the current consumption is roughly the same in sleep or stop mode.
- For more information, see “■ ELECTRICAL CHARACTERISTICS.”

3. Mask Options

The functions available as options and the method of specifying options differ between products. Before using options check “■ MASK OPTIONS.”

4. Wild register function

The Wild Register can be used in the following address spaces.

Device	Address Space
MB89PV560	4000 _H to FFFF _H
MB89P568	4000 _H to FFFF _H
MB89567A/567AC	8000 _H to FFFF _H

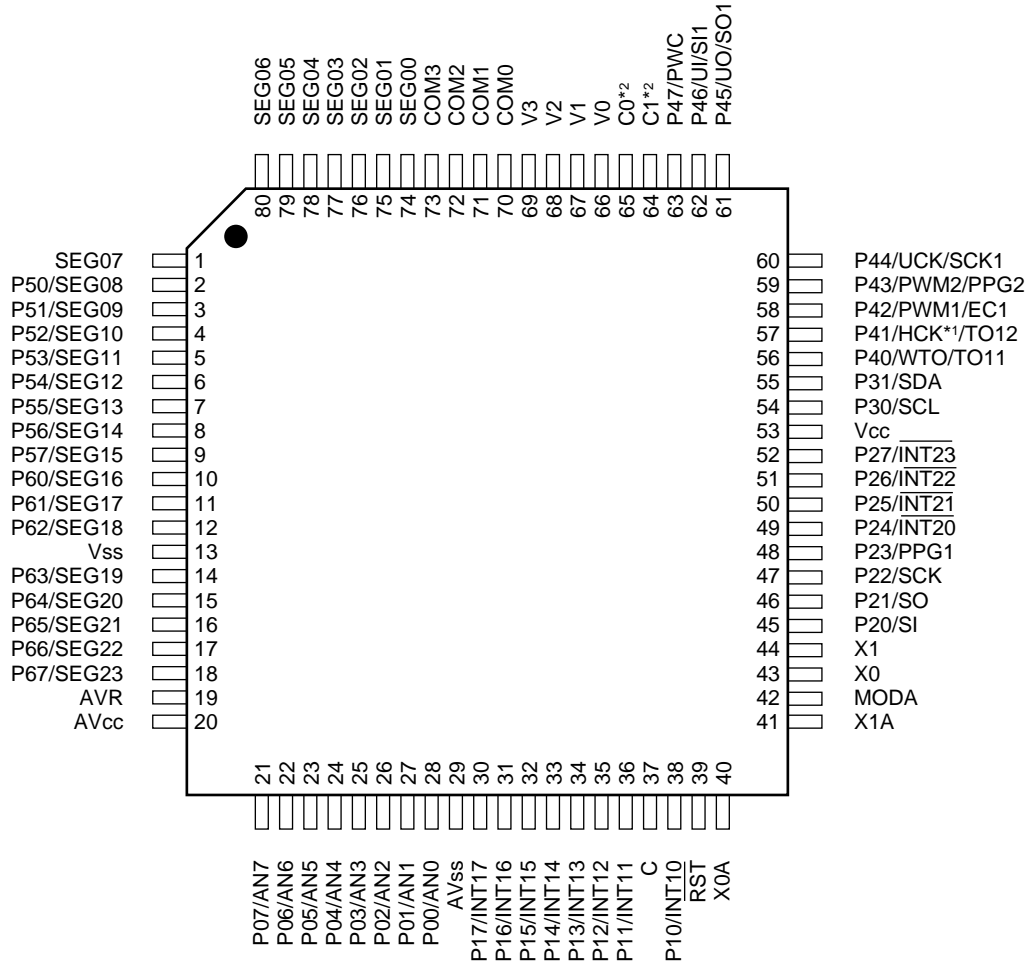
5. P40, P41

It will take about 64 count clock of external oscillation to initialize P40 and P41 pins in MB89PV560/P568. Therefore, these ports will be unstable for a while during power-on. For MB89567A/567AC, these ports will be in High-Z during power-on.

MB89560A Series

■ PIN ASSIGNMENT

(Top view)



(FPT-80P-M05)
(FPT-80P-M11)

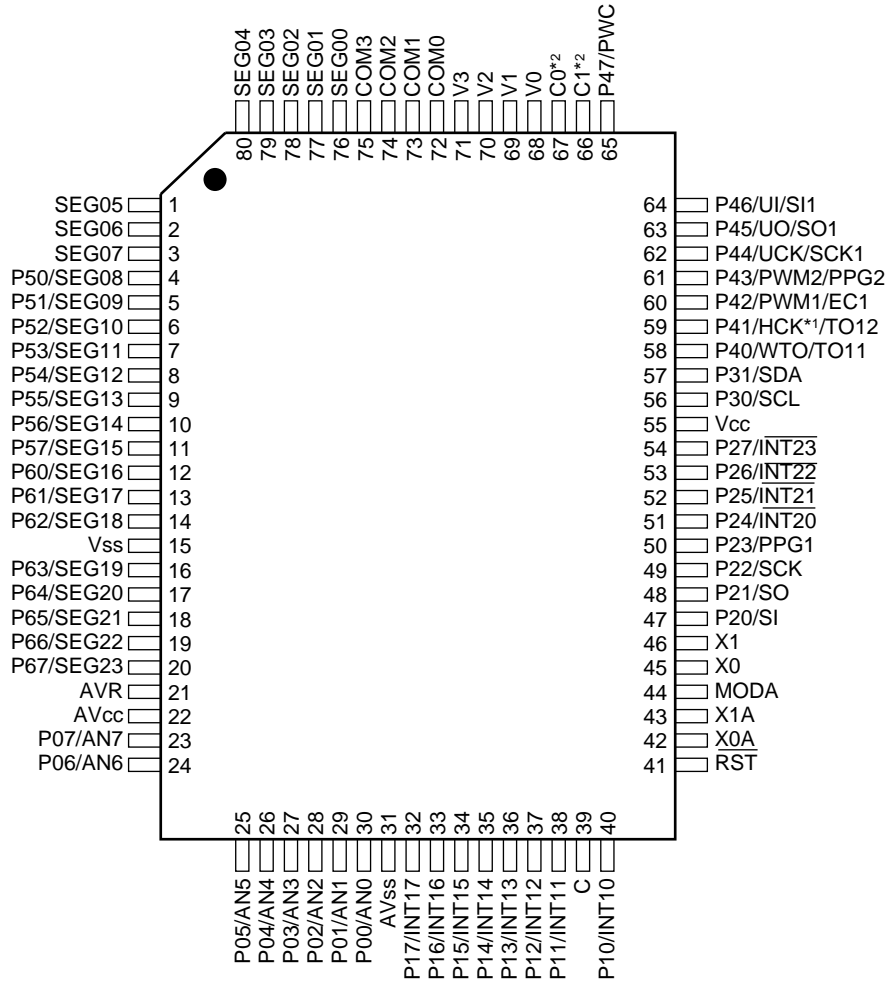
*1: Main clock divided by two output

*2: For built-in LCD booster only

Note: For mask option of *2, please refer to "■ MASK OPTIONS".

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(Top view)



(FPT-80P-M06)

*1: Main clock divided by two output

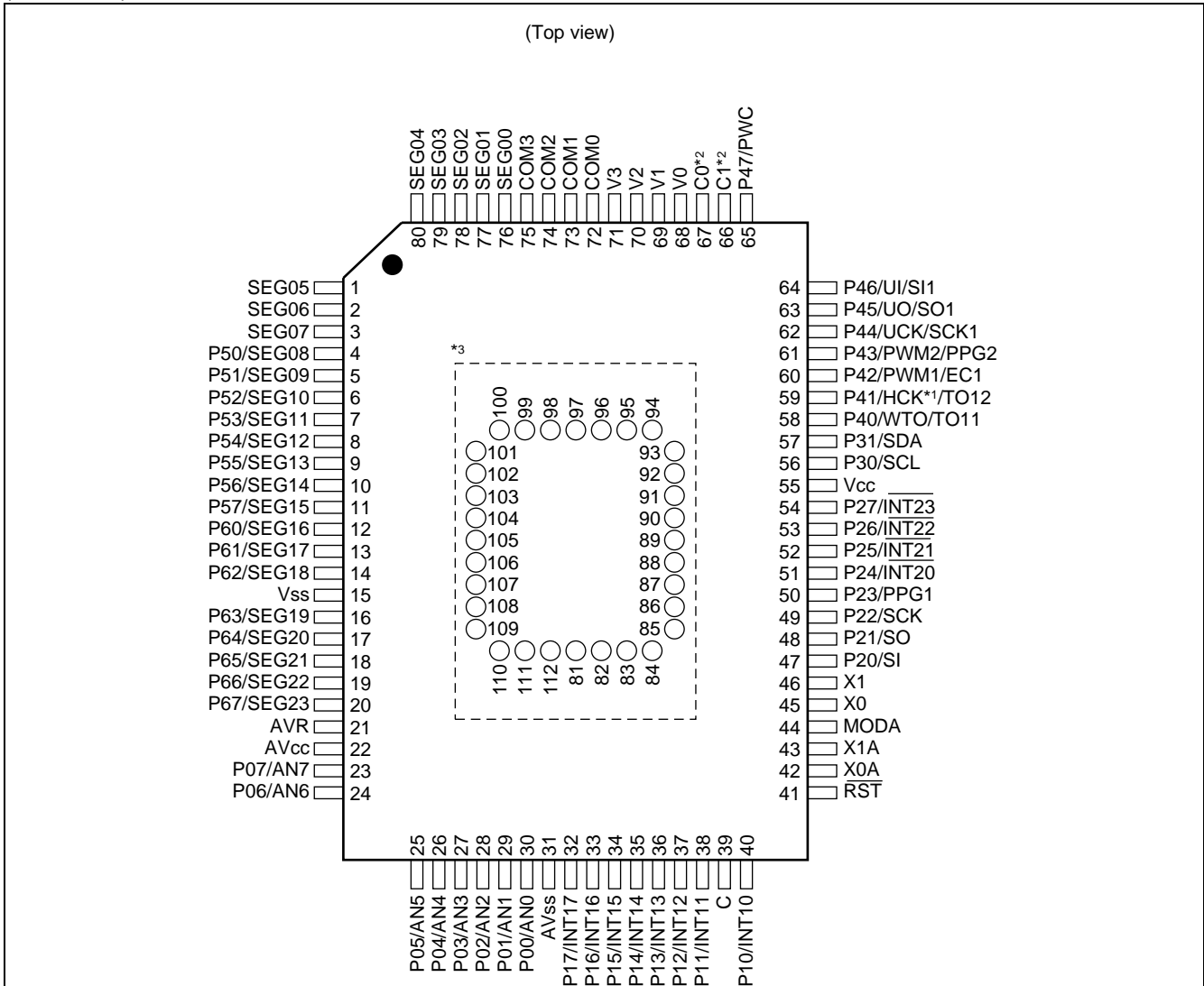
*2: For built-in LCD booster only

Note: For mask option of *2, please refer to "■ MASK OPTIONS".

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MB89560A Series

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- *1: Main clock divided by two output
- *2: For built-in LCD booster only
- *3: Pin assignment on package top (MB89PV560 only)

Pin no.	Pin	Pin no.	Pin	Pin no.	Pin	Pin no.	Pin
81	N.C.	89	AD2	97	N.C.	105	$\overline{\text{OE}}$
82	A15	90	AD1	98	O4	106	N.C.
83	A12	91	AD0	99	O5	107	A11
84	AD7	92	N.C.	100	O6	108	A9
85	AD6	93	O1	101	O7	109	A8
86	AD5	94	O2	102	O8	110	A13
87	AD4	95	O3	103	$\overline{\text{CE}}$	111	A14
88	AD3	96	VSS	104	A10	112	VCC

N.C.: Internally connected. Do not use.

Note: For mask option of *2, please refer to "■ MASK OPTIONS".

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type	Function
LQFP*1 LQFP*2	MQFP*3 QFP*4			
43	45	X0	A	Crystal or other resonator connector pins for the main clock. The external clock can be connected to X0. When this is done, be sure to leave X1 open.
44	46	X1		
42	44	MODA	C	Memory access mode setting pins. Connect directly to VSS. Hysteresis input type.
39	41	$\overline{\text{RST}}$	D	Reset I/O pin This pin is a CMOS output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset request (optional). The internal circuit is initialized by the input of “L”.
49 to 52	51 to 54	P24/ $\overline{\text{INT20}}$ to P27/ $\overline{\text{INT23}}$	E	General-purpose CMOS I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input. Selectable pull-up resistor.
30 to 36, 38	32 to 38, 40	P10/ $\overline{\text{INT10}}$ to P17/ $\overline{\text{INT17}}$	E	General-purpose CMOS I/O ports Also serve as input for external interrupt 1 input. External interrupt 1 input is hysteresis input. Selectable pull-up resistor.
60	62	P44/ $\overline{\text{UCK}}$ / SCK1	E	General-purpose CMOS I/O ports Also serve as the clock I/O for the High-speed UART and Serial I/O. The peripheral is a hysteresis input type. Selectable pull-up resistor.
61	63	P45/ $\overline{\text{UO}}$ / SO1	F	General-purpose CMOS I/O ports Also serves as the data output for the High-speed UART and Serial I/O.
62	64	P46/ $\overline{\text{UI}}$ / $\overline{\text{SI1}}$	G	N-ch open drain general-purpose I/O ports Also serves as the data input for the High-speed UART and Serial I/O. The peripheral is a hysteresis input type.
63	65	P47/ $\overline{\text{PWC}}$	G	N-ch open drain general-purpose I/O port Also serve as the external clock input for PWC. The peripheral is a hysteresis input.
56	58	P40/ $\overline{\text{WTO}}$ / TO11	F	General-purpose CMOS I/O port Also serves as an 8/16-bit timer/counter output and PWC output.

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MB89560A Series

Pin no.		Pin name	I/O circuit type	Function
LQFP*1 LQFP*2	MQFP*3 QFP*4			
57	59	P41/HCK/ TO12	F	General-purpose CMOS I/O port Also serves as an 8/16-bit timer/counter output. and half of main clock output Selectable pull-up resistor.
45	47	P20/SI	E	General-purpose CMOS I/O port Also serves as the data input for the serial I/O. The peripheral is a hysteresis input type. Selectable pull-up resistor.
46	48	P21/SO	F	General-purpose CMOS I/O port Also serves as the data output for the serial I/O. Selectable pull-up resistor.
47	49	P22/SCK	E	General-purpose CMOS I/O port Also serves as the clock I/O for the serial I/O. The peripheral is a hysteresis input type. Selectable pull-up resistor.
48	50	P23/PPG1	F	General-purpose CMOS I/O port Also serves as the 6 bit PPG output pin. Selectable pull-up resistor.
54	56	P30/SCL	G	N-ch open-drain general-purpose I/O port Clock I/O pin for I ² C interface
55	57	P31/SDA	G	N-ch open-drain general-purpose I/O port Data I/O pin for I ² C interface
65	67	C0	—	Function as capacitor connection pin in the products with a booster.
64	66	C1		
59	61	P43/ PWM2/ PPG2	F	General-purpose CMOS I/O port Also serves PWM wave output for the 8-bit PWM timer 1 and as 12 bit programmable pulse generator output. Selectable pull-up resistor.
58	60	P42/ PWM1/ EC1	E	General-purpose CMOS I/O port Also serves as the PWM wave output and external clock for the 8/16 bit timer counter. Selectable pull-up resistor.
21 to 28	23 to 30	P00/AN0 to P07/AN7	J	General-purpose CMOS I/O ports Also serve as the analog input for the A/D converter. Selectable pull-up resistor.

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MB89560A Series

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Pin no.		Pin name	I/O circuit type	Function
LQFP*1 LQFP*2	MQFP*3 QFP*4			
10 to 12 14 to 18	12 to 14 16 to 20	P60/ SEG16 to P67/ SEG23	H	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver segment output.
2 to 9	4 to 11	P50/SEG8 to P57/ SEG15	H	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver segment output.
74 to 80, 1	1 to 3 76 to 80	SEG0 to SEG7	I	LCD controller/driver segment output-only pins
70 to 73	72 to 75	COM0 to COM3	I	LCD controller/driver common output-only pins
66 to 69	68 to 71	V0 to V3	—	LCD driving power supply pins.
40	42	X0A	B	Crystal or other resonator connector pins for the subclock (Subclock: 32.768 kHz)
41	43	X1A		
53	55	Vcc	—	Power supply pin
37	39	C	—	Capacitor connection pin *5
13	15	Vss	—	Power supply (GND) pin
20	22	AVcc	—	A/D converter power supply pin
19	21	AVR	—	A/D converter reference voltage input pin
29	31	AVss	—	A/D converter power supply pin Use this pin at the same voltage as V _{SS} .

*1: FPT-80P-M05

*2: FPT-80P-M11

*3: MQP-80C-P01

*4: FPT-80P-M06

*5: When MB89567A / MB89567AC / MB89PV560-101 / MB89PV560-102 is used, this pin will become NC pin without internal connection. There is no problem to leave pins open, to fix pins at V_{CC} and to fix pins at V_{SS}. When MB89P568-101 or MB89P568-102 is used, this pin must be connected to V_{SS}.

MB89560A Series

- For External EPROM Socket (MB89PV560 ONLY)

Pin no.	Pin name	I/O	Function
82	A15	O	Address output pins
83	A12		
84	A7		
85	A6		
86	A5		
87	A4		
88	A3		
89	A2		
90	A1		
91	A0		
93	O1	I	Data input pins
94	O2		
95	O3		
96	Vss	O	Power supply (GND) pin
98	O4	I	Data input pins
99	O5		
100	O6		
101	O7		
102	O8		
103	\overline{CE}	O	ROM chip enable pin Outputs "H" during standby.
104	A10	O	Address output pin
105	\overline{OE}/V_{pp}	O	ROM output enable pin Outputs "L" at all times.
107	A11	O	Address output pins
108	A9		
109	A8		
110	A13		
111	A14		
112	Vcc	O	EPROM power supply pin
81	N.C.	—	Internally connected pins Be sure to leave them open.
92			
97			
106			

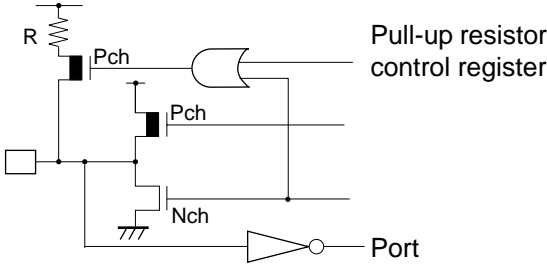
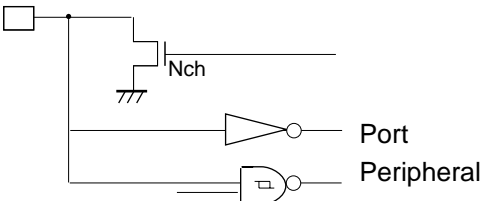
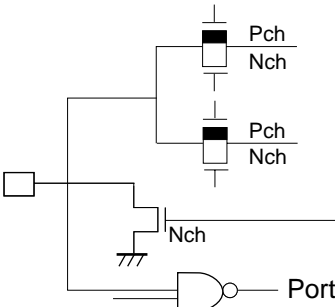
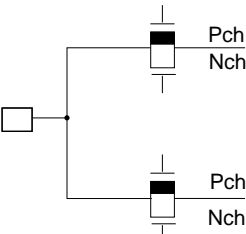
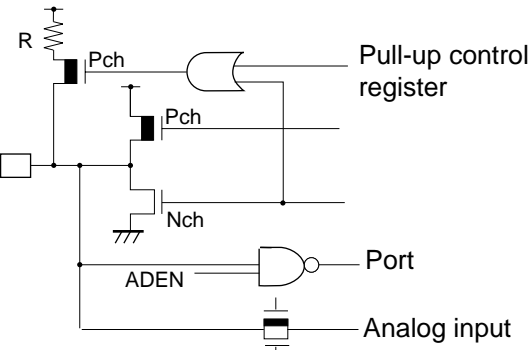
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	<p>Main clock control signal</p>	<p>Main clock (main clock crystal oscillator)</p> <ul style="list-style-type: none"> At an oscillation feedback resistor of approximately $1\text{ M}\Omega/5.0\text{ V}$
B	<p>Sub clock control signal</p>	<p>Subclock (subclock crystal oscillator)</p> <ul style="list-style-type: none"> At an oscillation feedback resistor of approximately $4.5\text{ M}\Omega/5.0\text{ V}$
C		<ul style="list-style-type: none"> Hysteresis input
D		<ul style="list-style-type: none"> CMOS output Hysteresis input At an output pull-up resistor (P-ch) of approximately $50\text{ k}\Omega/5.0\text{ V}$
E	<p>Pull-up control register</p> <p>Port</p> <p>Peripheral</p>	<ul style="list-style-type: none"> CMOS output CMOS input The peripheral is a hysteresis input type. Selectable pull-up resistor (P-ch) of approximately $50\text{ k}\Omega/5.0\text{ V}$

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MB89560A Series

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Type	Circuit	Remarks
F		<ul style="list-style-type: none"> • CMOS output • CMOS input • Selectable pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V
G		<ul style="list-style-type: none"> • N-ch open-drain input/output • CMOS input • The peripheral is a hysteresis input type. (P30,P31 are OR-type input for I²C)
H		<ul style="list-style-type: none"> • N-ch open-drain output • CMOS input • LCD controller/driver segment output
I		<ul style="list-style-type: none"> • LCD controller/driver common/segment output
J		<ul style="list-style-type: none"> • General CMOS I/O • Analog input (A/D converter) • Selectable pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Pull-up resistors must be disabled when used as an analog input.

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{CC} = DV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

7. Unused LCD dedicated pins

When LCD dedicated pins are not in use, keep it open.

8. Ports shared with SEG pin

When using port shared with SEG pin, be sure that the input voltage to port does not exceed the voltage of V3 (SEG driving voltage). This is particularly important to those devices with booster. When power-on or reset, SEG pin will output an initial value of “L”.

9. LCD not in use

When LCD is not in use, connect the V3 pin to V_{CC} and keep other LCD dedicated pins open.

10. Wild Register function

In MB89PV560, wild register function cannot be evaluated. To evaluate the wild register function, use MB89P568.

11. Programming operation on RAM

Program operation debugging at RAM is not possible even when using MB89PV560.

12. Note to Noise in the External Reset Pin (\overline{RST})

If the reset pulse applied to the external reset pin (\overline{RST}) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin (\overline{RST}).

MB89560A Series

■ PROGRAMMING TO THE EPROM ON THE MB89P568

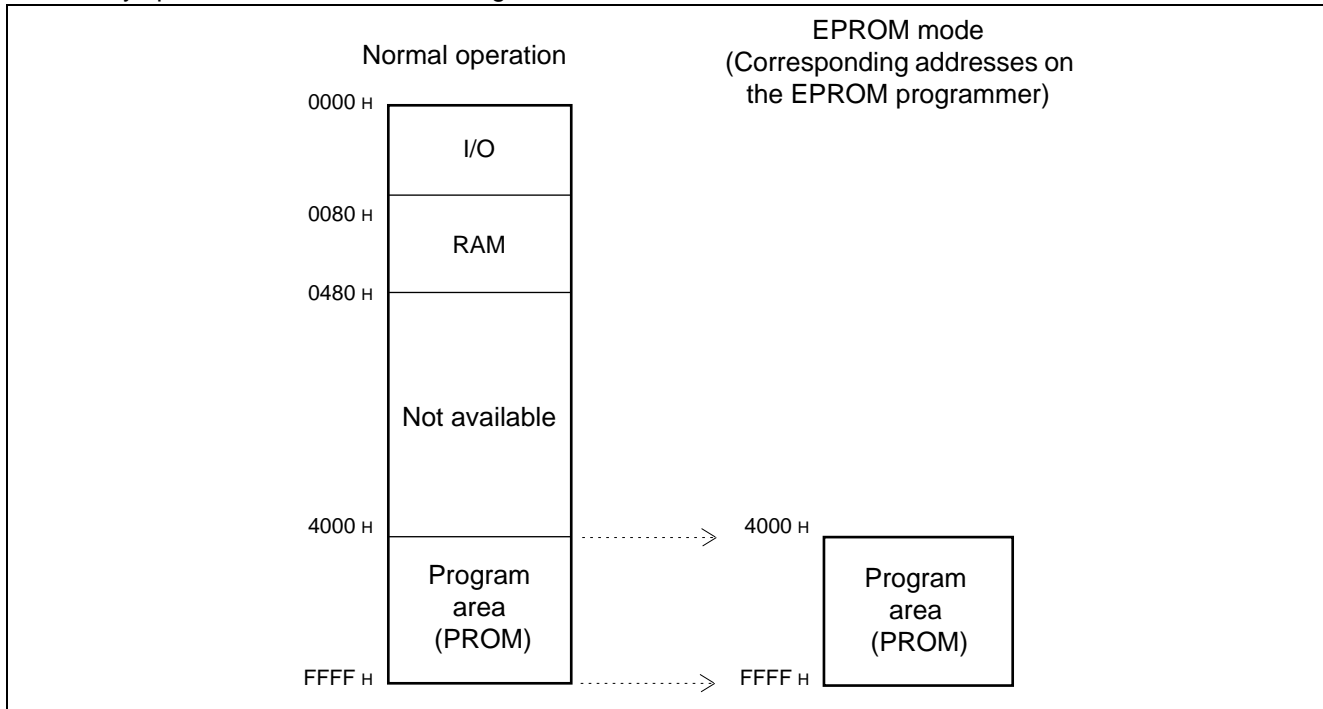
The MB89P568 is an OTPROM version of the MB89567A and MB89567AC.

1. Features

- 48-Kbyte PROM on chip
- Equivalency to the MBM27C1001 in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



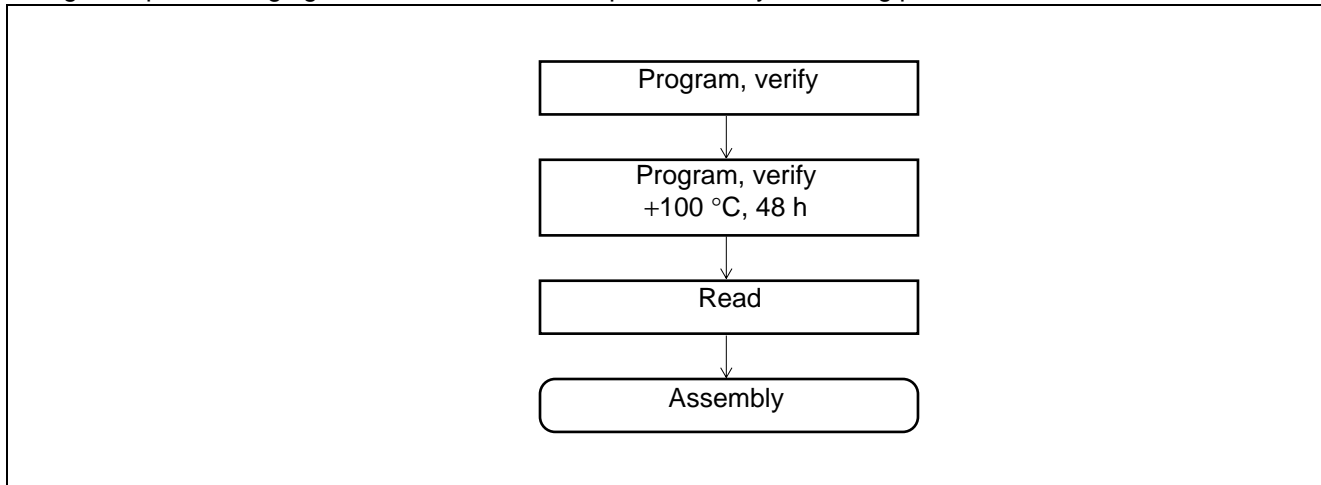
3. Programming to the EPROM

In EPROM mode, the MB89P568 functions equivalent to the MBM27C1001. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- Programming procedure
 - (1) Set the EPROM programmer to the MBM27C1001.
 - (2) Load program data into the EPROM programmer at 4000_H to FFFF_H
 - (3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M05	ROM-80SQF-32DP-8LA
FPT-80P-M06	ROM-80QF-32DP-8LA2
FPT-80P-M11	ROM-80QF2-32DP-8LA2

Inquiry: San Hayato Co., Ltd.: FAX +81-3-5396-9106 (Tokyo)

MB89560A Series

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

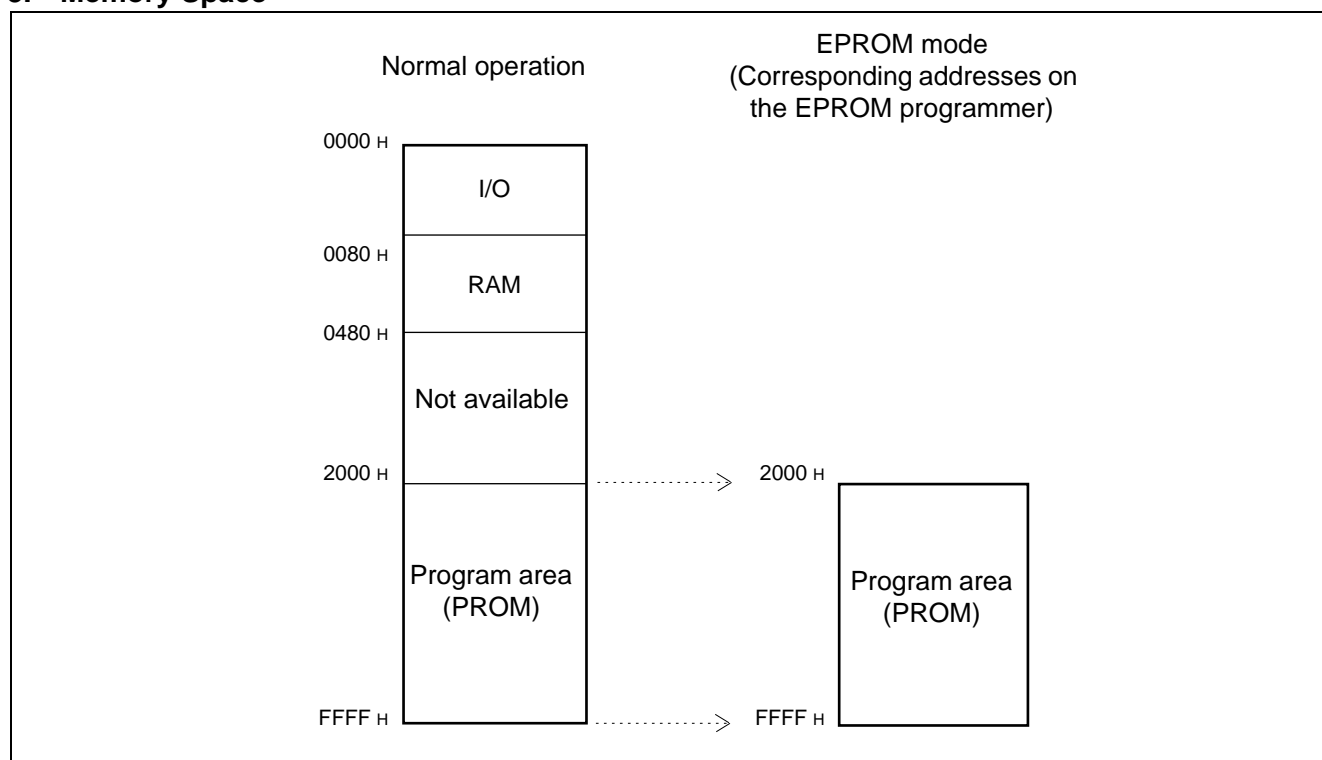
2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: San Hayato Co., Ltd.: FAX +81-3-5396-9106 (Tokyo)

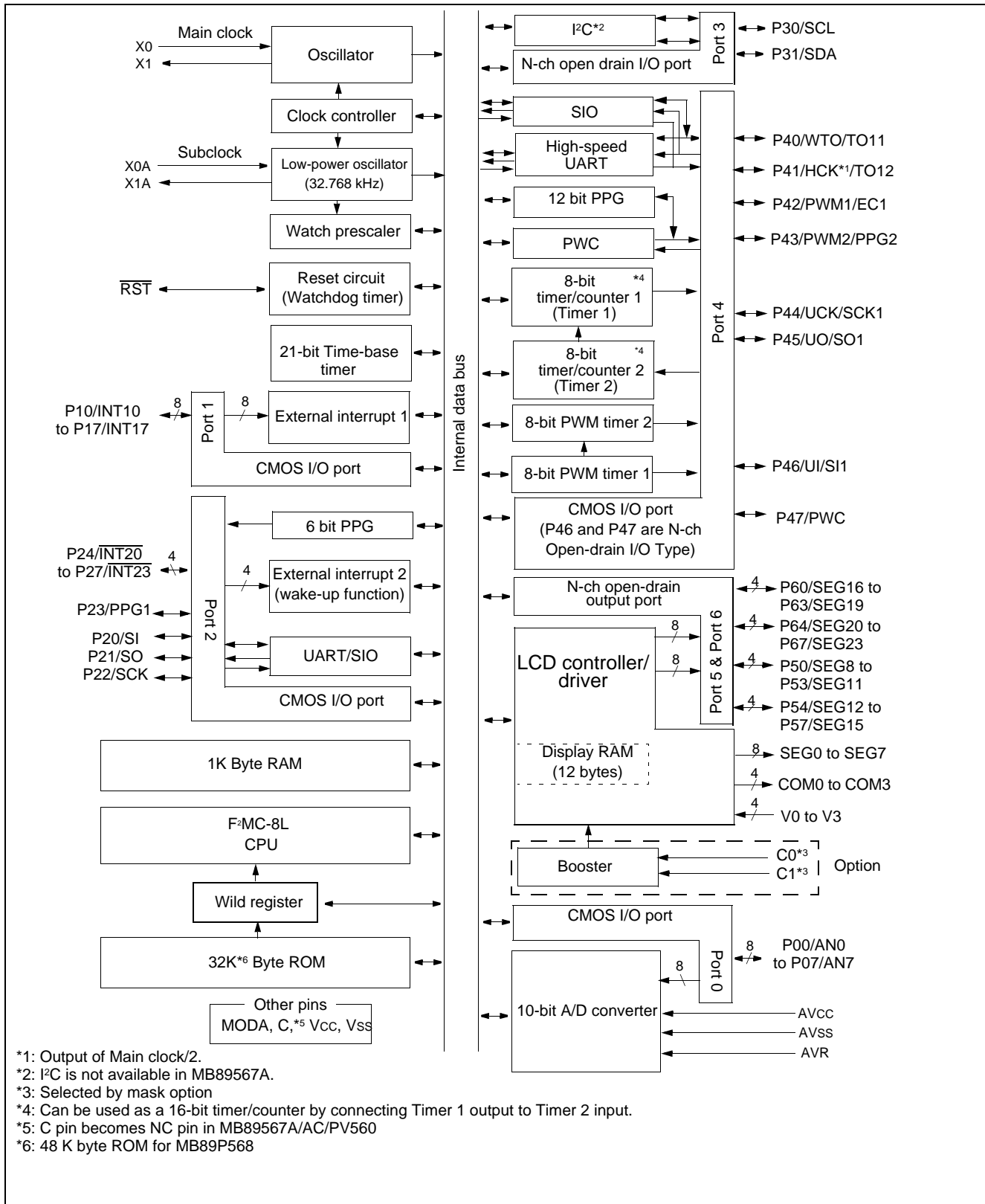
3. Memory Space



4. Programming to EPROM

- (1) Set the EPROM programmer to the MBM27C512.
- (2) Load program data into the EPROM programmer at 2000H to FFFFH.
- (3) Program to 2000H to FFFFH with the EPROM programmer.

■ BLOCK DIAGRAM



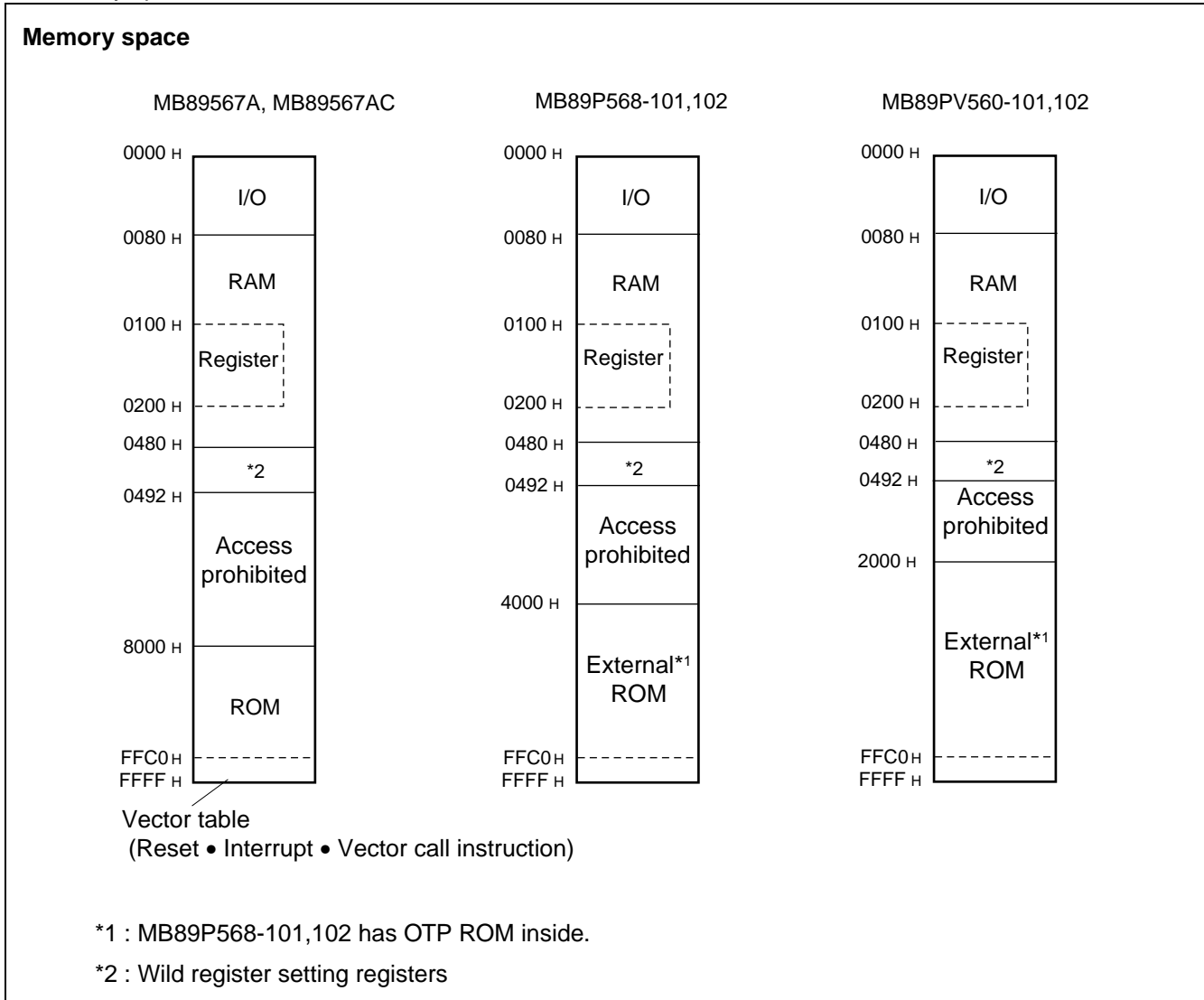
*1: Output of Main clock/2.
 *2: I²C is not available in MB89567A.
 *3: Selected by mask option
 *4: Can be used as a 16-bit timer/counter by connecting Timer 1 output to Timer 2 input.
 *5: C pin becomes NC pin in MB89567A/AC/PV560
 *6: 48 K byte ROM for MB89P568

MB89560A Series

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89560A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89560A series is structured as illustrated below.



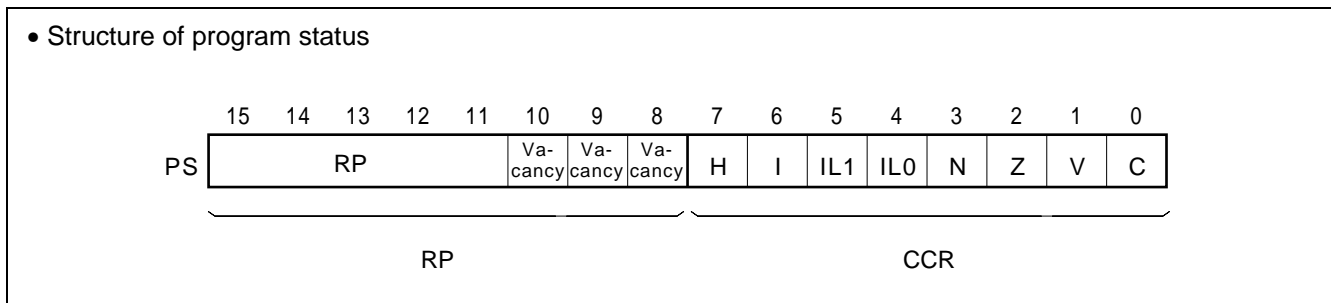
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

- Program counter (PC) : A 16-bit register for indicating specifies instruction storage positions.
- Accumulator (A) : A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register which performs arithmetic operations with the accumulator when the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX) : A 16-bit register for index modification
- Extra pointer (EP) : A 16-bit pointer for indicating a memory address
- Stack pointer (SP) : A 16-bit register for indicating a stack area
- Program status (PS) : A 16-bit register for storing a register pointer, a condition code

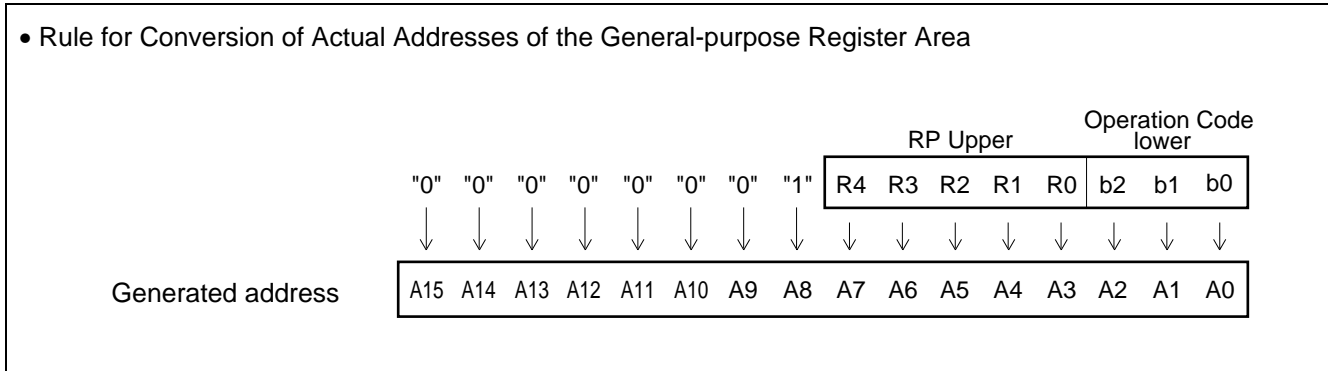
	16 bits		Initial value
PC	←-----→	: Program counter	FFFDH
A		: Accumulator	Undefined
T		: Temporally accumulator	Undefined
IX		: Indexing register	Undefined
EP		: Extra pointer	Undefined
SP		: Stuck pointer	Undefined
PS		: Program status	I Flag = 0, IL1, 0 = 11 other bits are undefined.

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



MB89560A Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↓ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag : Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag : Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag : Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

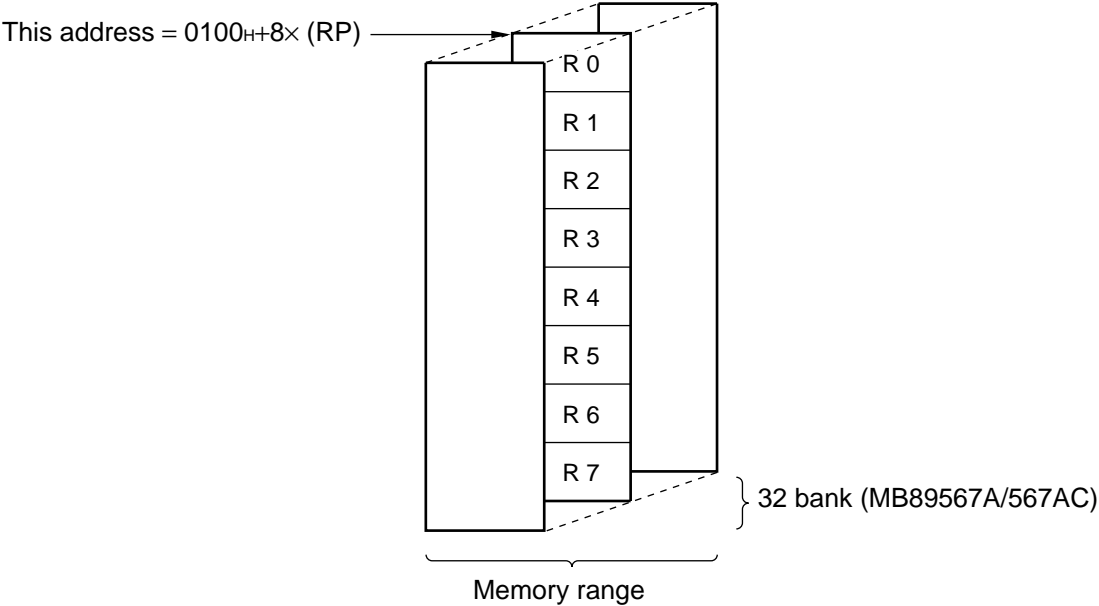
C-flag : Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used. The bank currently in use is indicated by the register bank pointer (RP).

- Register Bank Configuration



MB89560A Series

■ I/O MAP

Address	Register name	Register Description	Read/Write	Initial value
00 _H	PDR0	Port 0 data register	R/W	XXXXXXXX _B
01 _H	DDR0	Port 0 data direction register	W	0000000 _B
02 _H	PDR1	Port 1 data register	R/W	XXXXXXXX _B
03 _H	DDR1	Port 1 data direction register	W	0000000 _B
04 _H to 06 _H	(Vacancy)			
07 _H	SYCC	System clock control register	R/W	XXXMM100 _B
08 _H	STBC	Standby control register	R/W	00010XXX _B
09 _H	WDTC	Watchdog timer control register	W	0XXXXXXXX _B
0A _H	TBTC	Timebase timer control register	R/W	00XXX000 _B
0B _H	WPCR	Watch prescaler control register	R/W	00XX0000 _B
0C _H	PDR2	Port 2 data register	R/W	XXXXXXXX _B
0D _H	DDR2	Port 2 data direction register	R/W	0000000 _B
0E _H	PDR3	Port 3 data register	R/W	XXXXXX11 _B
0F _H	PDR4	Port 4 data register	R/W	XXXXXXXX _B
10 _H	DDR4	Port 4 direction register	R/W	XX000000 _B
11 _H	PDR5	Port 5 data register	R/W	0000000 _B
12 _H	(Vacancy)			
13 _H	PDR6	Port 6 data register	R/W	0000000 _B
14 _H to 19 _H	(Vacancy)			
1A _H	T2CR	Timer2 control register	R/W	X00000X0 _B
1B _H	T2DR	Timer2 data register	R/W	XXXXXXXX _B
1C _H	T1CR	Timer1 control register	R/W	X00000X0 _B
1D _H	T1DR	Timer1 data register	R/W	XXXXXXXX _B
1E _H to 21 _H	(Vacancy)			
22 _H	SMC11	UART1 mode control register 1	R/W	0000000 _B
23 _H	SRC1	UART1 mode data register	R/W	XX011000 _B
24 _H	SSD1	UART1 status/data register	R/W	00100X1X _B
25 _H	SIDR1/SODR1	UART1 data register	R/W	XXXXXXXX _B
26 _H	SMC12	UART1 mode control register 2	R/W	XX100001 _B
27 _H	CNTR1	PWM control register 1	R/W	0000000 _B
28 _H	CNTR2	PWM control register 2	R/W	000X0000 _B
29 _H	CNTR3	PWM control register 3	R/W	X000XXXX _B
2A _H	COMR1	PWM compare register 1	W	XXXXXXXX _B
2B _H	COMR2	PWM compare register 2	W	XXXXXXXX _B
2C _H	PCR1	PWC pulse width control register 1	R/W	000XX000 _B

(Continued)

MB89560A Series

Address	Register name	Register Description	Read/Write	Initial value
2D _H	PCR2	PWC pulse width control register 2	R/W	00000000 _B
2E _H	RLBR	PWC reload buffer register	R/W	XXXXXXXX _B
2F _H	SMC21	UART2/SIO mode control register	R/W	00000000 _B
30 _H	SMC22	UART2/SIO mode control register 2	R/W	00000000 _B
31 _H	SSD2	UART2/SIO status/data register	R/W	00001XXX _B
32 _H	SIDR2/SODR2	UART2/SIO data register	R/W	XXXXXXXX _B
33 _H	SRC2	UART2/SIO rate control register	R/W	XXXXXXXX _B
34 _H	ADC1	A/D control register 1	R/W	X00000X0 _B
35 _H	ADC2	A/D control register 2	R/W	X0000001 _B
36 _H	ADDL	A/D data register L	R/W	XXXXXXXX _B
37 _H	ADDH	A/D data register H	R/W	XXXXXXXX _B
38 _H	RCR21	PPG control register 1(PPG2)	R/W	00000000 _B
39 _H	RCR23	PPG control register 3(PPG2)	R/W	0X000000 _B
3A _H	RCR22	PPG control register 2(PPG2)	R/W	XX000000 _B
3B _H	RCR24	PPG control register 4(PPG2)	R/W	XX000000 _B
3C _H to 3E _H	(Vacancy)			
3F _H	EIC1	External interrupt 1 control register 1	R/W	00000000 _B
40 _H	EIC2	External interrupt 1 control register 2	R/W	00000000 _B
41 _H	EIC3	External interrupt 1 control register 3	R/W	00000000 _B
42 _H	EIC4	External interrupt 1 control register 4	R/W	00000000 _B
43 _H to 50 _H	(Vacancy)			
51 _H	IBSR	I ² C bus status register	R	00000000 _B
52 _H	IBCR	I ² C bus control register	R/W	00000000 _B
53 _H	ICCR	I ² C clock control register	R/W	000XXXXX _B
54 _H	IADR	I ² C address register	R/W	XXXXXXXX _B
55 _H	IDAR	I ² C data register	R/W	XXXXXXXX _B
56 _H	EIE2	External interrupt 2 enable register	R/W	XXXX0000 _B
57 _H	EIF2	External interrupt 2 flag register	R/W	XXXXXXXX0 _B
58 _H	RCR1	PPG control register 1(PPG1)	R/W	00000000 _B
59 _H	RCR2	PPG control register 2(PPG1)	R/W	0X000000 _B
5A _H	CKR	Clock Output control register	R/W	00000000 _B
5B _H	LCR1	LCD controller/driver control register 1	R/W	00010000 _B
5C _H	LCR2	LCD controller/driver control register 2	R/W	00000000 _B
5D _H	LCR3	LCD controller/driver control register 3	R/W	XX000000 _B
5E _H	LDR1	LCD data register 1	R/W	XXXXXXXX _B

(Continued)

MB89560A Series

(Continued)

Address	Register name	Register Description	Read/Write	Initial value
5F _H	(Vacancy)			
60 _H to 6B _H	VRAM	Display RAM	R/W	XXXXXXXX _B
6C _H to 6F _H	(Vacancy)			
70 _H	SMR	Serial I/O mode register	R/W	00000000 _B
71 _H	SDR	Serial I/O data register	R/W	XXXXXXXX _B
72 _H	PURR0	Pull-up resistor register 0	R/W	11111111 _B
73 _H	PURR1	Pull-up resistor register 1	R/W	11111111 _B
74 _H	PURR2	Pull-up resistor register 2	R/W	11111111 _B
75 _H	PURR4	Pull-up resistor register 4	R/W	XX111111 _B
76 _H	(Vacancy)			
77 _H	WREN	Wild register enable register	R/W	XX000000 _B
78 _H	WROR	Wild register data test register	R/W	XX000000 _B
79 _H	ADEN	A/D port input enable register	R/W	11111111 _B
7A _H	(Vacancy)			
7B _H	ILR1	Interrupt level setting register 1	W	11111111 _B
7C _H	ILR2	Interrupt level setting register 2	W	11111111 _B
7D _H	ILR3	Interrupt level setting register 3	W	11111111 _B
7E _H	ILR4	Interrupt level setting register 4	W	11111111 _B
7F _H	ITR	Interrupt test register	Access Prohibited	11111111 _B

Read/write access symbols

- R/W : Readable and writable
- R : Read-only
- W : Write-only

Initial value symbols

- 0 : The initial value of this bit is "0".
- 1 : The initial value of this bit is "1".
- X : The initial value of this bit is undefined.
- M : The initial value of this bit is determined by mask option.

Note : Do not use vacancies.

■ WILD REGISTER I/O MAP

Address	Register name	Register description	Read/Write	Initial value
480 _H	WRARH1	Wild register high-byte address register1	R/W	XXXXXXXX _B
481 _H	WRARL1	Wild register low-byte address register1	R/W	XXXXXXXX _B
482 _H	WRDR1	Wild register data register1	R/W	XXXXXXXX _B
483 _H	WRARH2	Wild register high-byte address register2	R/W	XXXXXXXX _B
484 _H	WRARL2	Wild register low-byte address register2	R/W	XXXXXXXX _B
485 _H	WRDR2	Wild register data register2	R/W	XXXXXXXX _B
486 _H	WRARH3	Wild register high-byte address register3	R/W	XXXXXXXX _B
487 _H	WRARL3	Wild register low-byte address register3	R/W	XXXXXXXX _B
488 _H	WRDR3	Wild register data register3	R/W	XXXXXXXX _B
489 _H	WRARH4	Wild register high-byte address register4	R/W	XXXXXXXX _B
48A _H	WRARL4	Wild register low-byte address register4	R/W	XXXXXXXX _B
48B _H	WRDR4	Wild register data register4	R/W	XXXXXXXX _B
48C _H	WRARH5	Wild register high-byte address register5	R/W	XXXXXXXX _B
48D _H	WRARL5	Wild register low-byte address register5	R/W	XXXXXXXX _B
48E _H	WRDR5	Wild register data register5	R/W	XXXXXXXX _B
48F _H	WRARH6	Wild register high-byte address register6	R/W	XXXXXXXX _B
490 _H	WRARL6	Wild register low-byte address register6	R/W	XXXXXXXX _B
491 _H	WRDR6	Wild register data register6	R/W	XXXXXXXX _B

Read/write access symbols

R/W : Readable and writable
 R : Read-only
 W : Write-only

Initial value symbols

0 : The initial value of this bit is "0".
 1 : The initial value of this bit is "1".
 X : The initial value of this bit is undefined.
 M : The initial value of this bit is determined by mask option.

Note : Do not use vacancies.

MB89560A Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC} AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	MB89567A, MB89567AC, MB89P568 and MB89PV560*1 AVR must not exceed "AVcc + 0.3V".
	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
LCD power voltage	V0 to V3	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	V0 to V3 should not exceed Vcc Without booster
Program voltage	V_{PP}	$V_{SS} - 0.6$	$V_{SS} + 13.0$	V	Only for the MB89P568
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	For pins other than P30, P31, P46, P47, P50 to P57 and P60 to P67
		$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	P50 to P57, P60 to P67 Resister Ladder option
		$V_{SS} - 0.3$	V3	V	P50 to P57, P60 to P67 LCD booster option
		$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	For P30, P31, P46, P47
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	For pins other than P30, P31, P46, P47, P50 to P57 and P60 to P67
		$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	P50 to P57, P60 to P67 Resister Ladder option
		$V_{SS} - 0.3$	V3	V	P50 to P57, P60 to P67 LCD booster option
		$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	For P30, P31, P46, P47
"L" level maximum output current	I_{OL}	—	15	mA	For pins other than P20 to P27
			30	mA	For P20 to P27 only
"L" level average output current	I_{OLAV}	—	4	mA	For pins other than P20 to P27*2
			15	mA	For P20 to P27 only*2
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	60	mA	*2
"H" level maximum output current	I_{OH}	—	- 15	mA	For pins other than P20 to P27, P30, P31, P46, P47, P50 to P57, P60 to P67
			- 30	mA	For P20 to P27 only
"H" level average output current	I_{OHAV}	—	- 4	mA	For pins other than P20 to P27*2
			- 15		For P20 to P27 only*2

(Continued)

MB89560A Series

(Continued)

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level total maximum output current	ΣI_{OH}	—	– 50	mA	
"H" level total average output current	$\Sigma I_{OHA\bar{V}}$	—	– 30	mA	*2
Power consumption	P _D	—	300	mW	
Operating temperature	T _A	– 40	+ 85	°C	
Storage temperature	T _{stg}	– 55	+ 150	°C	

*1 : Use AV_{CC} and V_{CC} set at the same voltage.

Take care so that AVR does not exceed AV_{CC} + 0.3 V, such as when power is turned on.

Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

*2 : Average value (operating current × operating rate)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB89560A Series

2. Recommended Operating Conditions

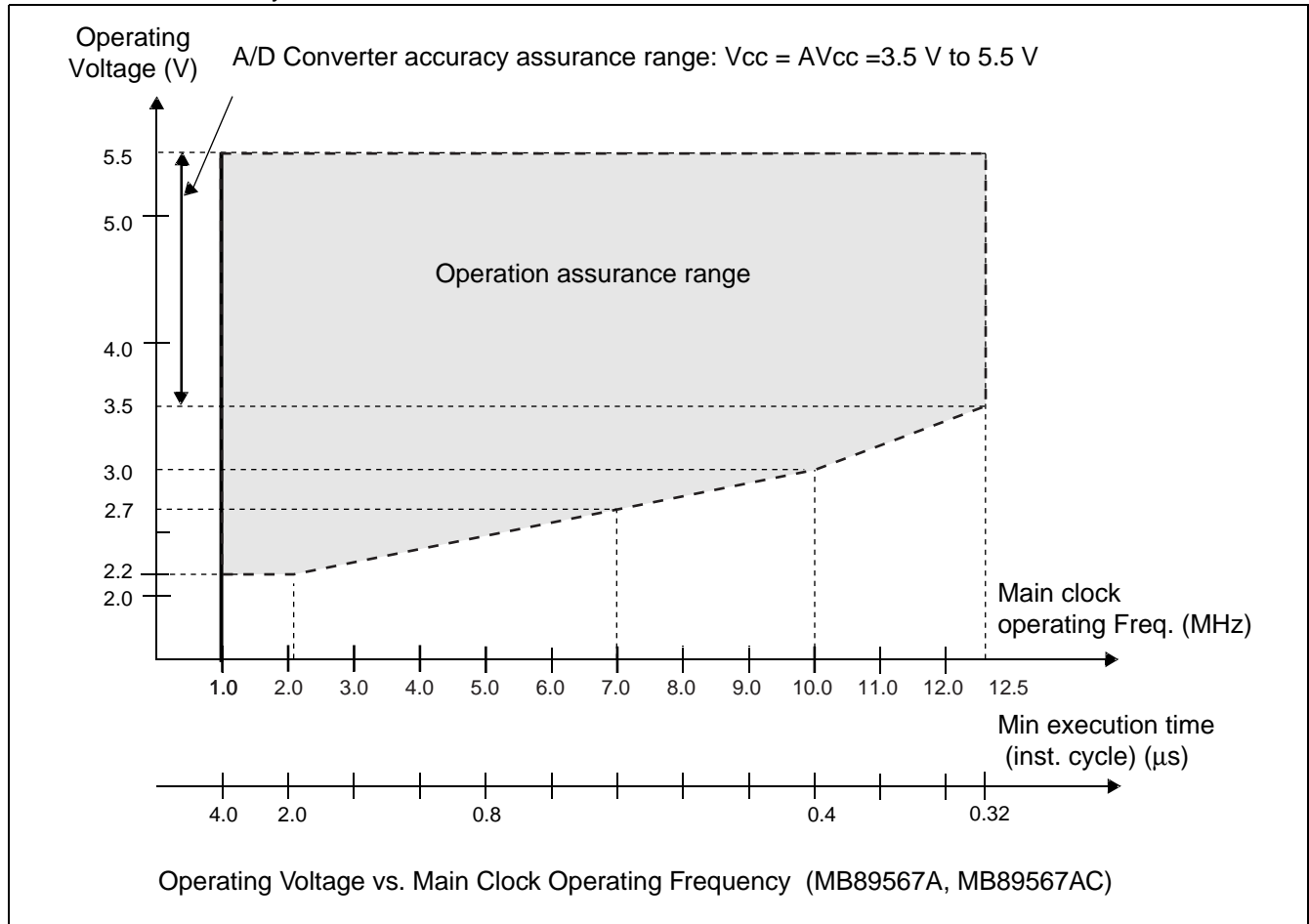
(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V _{CC} AV _{CC}	2.2*	5.5*	V	For MB89567A and MB89567AC
		1.5	5.5	V	Retains the RAM state in stop mode for MB89567A and MB89567AC
		2.7*	5.5*	V	For MB89PV560 and MB89P568
		1.5	5.5	V	Retains the RAM state in stop mode for MB89PV560 and MB89P568
LCD power voltage	V0 to V3	V _{SS}	V _{CC}	V	Liquid crystal power supply range : without booster (The best value is according to the specification of LCD used.)
A/D converter reference input voltage	AVR	3.5	AV _{CC}	V	
Operating temperature	T _A	- 40	+ 85	°C	

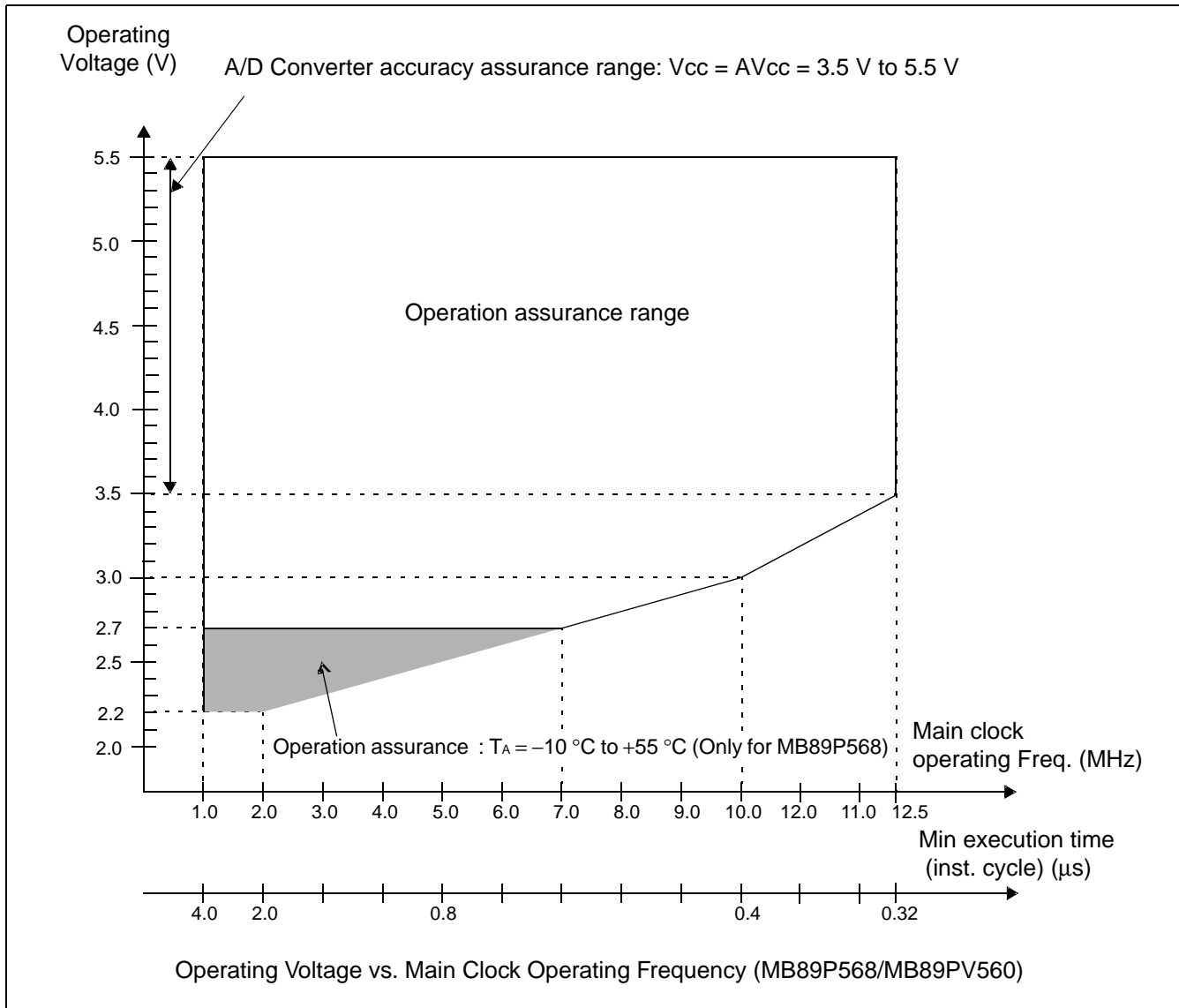
* : These values depend on the operating conditions and the analog assurance range. See Figure “Operating Voltage vs. Main Clock Operating Frequency (MB89567A, MB89567AC)”, “Operating Voltage vs. Main Clock Operating Frequency (MB89P568/MB89PV560)” and “6. A/D Converter Electrical Characteristics.”

MB89560A Series

“Operating Voltage vs. Main Clock Operating Frequency (MB89567A, MB89567AC) and “Operating Voltage vs. Main Clock Operating Frequency (MB89P568/MB89PV560) indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$



MB89560A Series



Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB89560A Series

3. DC Characteristics (power supply voltage : 5.0V)

($AV_{CC} = V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P45, P50 to P57, P60 to P67	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS
	V_{IHS}	\overline{RST} , MODA, INT10 to INT17, INT20 to INT23, SI, SCK, EC1, UCK, SCK1, UI, SI1, PWC	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis
	V_{IHSMB}	SCL, SDA	—	$V_{SS} + 1.4$	—	$V_{SS} + 5.5$	V	SMB input buffer selected
	V_{IH2C}		—	$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	I ² C input buffer selected
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P45, P50 to P57, P60 to P67	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	CMOS
	V_{ILS}	\overline{RST} , MODA, INT10 to INT17, INT20 to INT23, SI, SCK, EC1, UCK, SCK1, UI, SI1, PWC	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis
	V_{ILSMB}	SCL, SDA	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.6$	V	SMB input buffer selected
	V_{IL2C}		—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	I ² C input buffer selected
Open-drain output pin application voltage	V_D	P60 to P67, P50 to P57	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	Resister Ladder option
		P60 to P67, P50 to P57	—	$V_{SS} - 0.3$	—	V3	V	LCD booster option
		P46, P47, P30, P31	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P40 to P45	$I_{OH} = -2.0\text{ mA}$	4.0	—	—	V	
		P20 to P27	$I_{OH} = -15.0\text{ mA}$	4.0	—	—		

(Continued)

MB89560A Series

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L” level output voltage	V _{OL}	P00 to P07, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, $\overline{\text{RST}}$	I _{OL} = 4.0 mA	—	—	0.4	V	
		P20 to P27	I _{OL} = 15.0 mA	—	—	0.4		
Input leakage current (High-Z output leakage current)	I _{LI}	P00 to P07, P10 to P17, P20 to P27, P40 to P45	0.0 V < V _I < V _{CC}	-5	—	+5	μA	Without pull-up Resistor
		P50 to P57, P60 to P67		-5	—	+5	μA	Resistor Ladder option
		P50 to P57, P60 to P67	0.0 V < V _I < V ₃	-5	—	+5	μA	LCD booster option
		MODA	0.0 V < V _I < V _{CC}	-10	—	+10	μA	MB89PV560 MB89P568
Open-drain output leakage current	I _{LIOD}	P50 to P57, P60 to P67	0.0 V < V _I < V _{CC}	—	—	+5	μA	Resistor Ladder option
		P50 to P57, P60 to P67	0.0 V < V _I < V ₃	—	—	+5	μA	LCD booster option
		P30, P31, P46, P47	0.0 V < V _I < V _{SS} + 5.5 V	—	—	+5	μA	
Pull-up resistance	R _{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P45, $\overline{\text{RST}}$	V _I = 0.0 V	25	50	100	kΩ	When pull-up resistor selected except $\overline{\text{RST}}$
Pull-down resistance	R _{MODA}	MODA	V _I = 3.0 V	50	100	200	kΩ	MB89567A/ MB89567AC
Power supply current *1	I _{CC1}	V _{CC}	F _{CH} = 10 MHz, t _{inst} ^{*2} = 0.4 μs, Main clock run mode	—	15	20	mA	MB89PV560 MB89P568
				—	8	13		MB89567A MB89567AC
	I _{CC2}		F _{CH} = 10 MHz, t _{inst} ^{*2} = 6.4 μs, Main clock run mode	—	5	8.5	mA	MB89PV560 MB89P568
				—	1	3		MB89567A MB89567AC
	I _{CCS1}		F _{CH} = 10 MHz, t _{inst} ^{*2} = 0.4 μs, Main clock sleep mode	—	5	7	mA	MB89PV560 MB89P568
				—	2.5	5		MB89567A MB89567AC

(Continued)

MB89560A Series

(Continued)

($AV_{CC} = V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current *1	I _{CCS2}	V _{CC}	F _{CH} = 10 MHz, t _{inst} *2 = 6.4 μs, Sleep mode	—	1.5	3	mA	MB89PV560 MB89P568
				—	0.7	2		MB89567A MB89567AC
	I _{CCL}		F _{CL} = 32.768 kHz, Subclock mode, T _A = +25 °C	—	3	7	mA	MB89PV560 MB89P568
				—	50	85		μA
	I _{CCLS}		F _{CL} = 32.768 kHz, Subclock sleep mode, T _A = +25 °C	—	30	50	μA	MB89PV560 MB89P568
				—	15	30		MB89567A MB89567AC
I _{CCT}	F _{CL} = 32.768 kHz, T _A = +25 °C, Watch mode, Main clock stop mode	—	—	5	15	μA	MB89PV560 MB89P568	
				1.6	15		μA	MB89567A MB89567AC
Power supply current *1	I _{CCH}	V _{CC}	T _A = +25 °C, Subclock stop mode	—	3	10	μA	MB89PV560 MB89P568
					1	10		μA
LCD divided resistance	R _{LCD}	—	Between V _{CC} and V _{SS}	300	500	750	kΩ	
COM0 to COM3 output impedance	R _{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	5	kΩ	
SEG0 to SEG23 output impedance	R _{VSEG}	SEG0 to SEG23		—	—	15	kΩ	
LCD controller/driver leakage current	I _{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG23	—	-1	—	1	μA	
Input capacitance	C _{IN}	Other than AV _{CC} , AV _{SS} , V _{CC} , and V _{SS}	f = 1 MHz	—	10	—	pF	

*1 : The power supply current is measured at the external clock

*2 : For information on t_{inst}, see "5. AC Characteristics (4) Instruction Cycle."

Note : For LCD and port multiplex pin (P50 to P57, P60 to P67), please refer to LCD specification when the port is used, and refer to LCD specification when used as LCD pin.

MB89560A Series

4. DC Characteristics (power supply voltage : 3.0V)

($A_{V_{CC}} = V_{CC} = 3.0V$, $A_{V_{SS}} = V_{SS} = 0.0V$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P45, P50 to P57, P60 to P67	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS
	V_{IHS}	\overline{RST} , MODA, INT10 to INT17, INT20 to INT23, SI,SCK,EC1,UCK, SCK1,UI,SI1,PWC	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis
	V_{IHSMB}	SCL, SDA	—	$V_{SS} + 1.4$	—	$V_{SS} + 5.5$	V	SMB input buffer selected
	V_{IH2C}		—	$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	I ² C input buffer selected
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P45, P50 to P57, P60 to P67	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	CMOS
	V_{ILS}	\overline{RST} , MODA, INT10 to INT17, INT20 to INT23, SI,SCK,EC1,UCK, SCK1,UI,SI1,PWC	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis
	V_{ILSMB}	SCL, SDA	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.6$	V	SMB input buffer selected
	V_{IL2C}		—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	I ² C input buffer selected
Open-drain output pin application voltage	V_D	P60 to P67, P50 to P57	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	Resistor Ladder option
		P60 to P67, P50 to P57	—	$V_{SS} - 0.3$	—	V3	V	LCD booster option
		P46, P47, P30, P31	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P40 to P45	$I_{OH} = -2.0\text{ mA}$	2.4	—	—	V	
		P20 to P27	$I_{OH} = -10\text{ mA}$	2.4	—	—		

(Continued)

MB89560A Series

($AV_{CC} = V_{CC} = 3.0V$, $AV_{SS} = V_{SS} = 0.0V$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L” level output voltage	V_{OL}	P00 to P07, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, \overline{RST}	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
		P20 to P27	$I_{OL} = 10\text{ mA}$	—	—	0.4		
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P40 to P45	$0.0\text{ V} < V_i < V_{CC}$	-5	—	+5	μA	Without pull-up Resister
		P50 to P57, P60 to P67		-5	—	+5	μA	Resister Ladder option
		P50 to P57, P60 to P67	$0.0\text{ V} < V_i < V_3$	-5	—	+5	μA	LCD booster option
		MODA	$0.0\text{ V} < V_i < V_{CC}$	-10	—	+10	μA	MB89PV560 MB89P568
Open-drain output leakage current	I_{LIOD}	P50 to P57, P60 to P67	$0.0\text{ V} < V_i < V_{CC}$	—	—	+5	μA	Resister Ladder option
		P50 to P57, P60 to P67	$0.0\text{ V} < V_i < V_3$	—	—	+5	μA	LCD booster option
		P30, P31, P46, P47	$0.0\text{ V} < V_i < V_{SS} + 5.5\text{ V}$	—	—	+5	μA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P45, \overline{RST}	$V_i = 0.0\text{ V}$	50	100	200	k Ω	When pull-up resistor selected except \overline{RST}
Pull-down resistance	R_{MODA}	MODA	$V_i = 5.0\text{ V}$	25	50	100	k Ω	MB89567A MB89567AC
Power supply current *1	I_{CC1}	V_{CC}	$F_{CH} = 10\text{ MHz}$, $t_{inst}^{*2} = 0.4\text{ }\mu\text{s}$, Main clock run mode	—	6	10	mA	MB89PV560 MB89P568
				—	4	9		MB89567A MB89567AC
	I_{CC2}		$F_{CH} = 10\text{ MHz}$, $t_{inst}^{*2} = 6.4\text{ }\mu\text{s}$, Main clock run mode	—	1.5	3	mA	MB89PV560 MB89P568
				—	0.4	2		MB89567A MB89567AC

(Continued)

MB89560A Series

(Continued)

($AV_{CC} = V_{CC} = 3.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current *1	I _{CCS1}	V _{CC}	F _{CH} = 10 MHz, t _{inst} *2 = 0.4 μs, Main clock sleep mode	—	2	4	mA	MB89PV560 MB89P568
				—	1	3		MB89567A MB89567AC
	I _{CCS2}		F _{CH} = 10 MHz, t _{inst} *2 = 6.4 μs, Main clock sleep mode	—	1	2	mA	MB89PV560 MB89P568
				—	0.3	1.5		MB89567A MB89567AC
	I _{CLL}		F _{CL} = 32.768 kHz, Subclock mode, T _A = +25 °C	—	1	3	mA	MB89PV560 MB89P568
				—	25	60		μA
	I _{CCLS}		F _{CL} = 32.768 kHz, Subclock sleep mode, T _A = +25 °C	—	15	30	μA	MB89PV560 MB89P568
				—	8	25		MB89567A MB89567AC
I _{CCT}	F _{CL} = 32.768 kHz, T _A = +25 °C, Watch mode, Main clock stop mode	—	5	15	μA	MB89PV560 MB89P568		
			1	14		MB89567A MB89567AC		
I _{CCH}	T _A = +25 °C, Subclock stop mode	—	1	5	μA			
LCD divided resistance	R _{LCD}	—	Between V _{CC} and V _{SS}	300	500	750	kΩ	
COM0 to COM3 output impedance	R _{VCOM}	COM0 to COM3	V1 to V3 = 3.0 V	—	—	5	kΩ	
SEG0 to 23 output impedance	R _{VSEG}	SEG0 to SEG23		—	—	15	kΩ	
LCD controller/ driver leakage current	I _{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG23	—	-1	—	1	μA	
Input capacitance	C _{IN}	Other than AV _{CC} , AV _{SS} , V _{CC} , and V _{SS}	f = 1 MHz	—	10	—	pF	

*1 : The power supply current is measured at the external clock

*2 : For information on t_{inst}, see "5. AC Characteristics (4) Instruction Cycle."

Note : For LCD and port multiplex pin (P50 to P57, P60 to P67), please refer to LCD specification when the port is used, and refer to LCD specification when used as LCD pin.

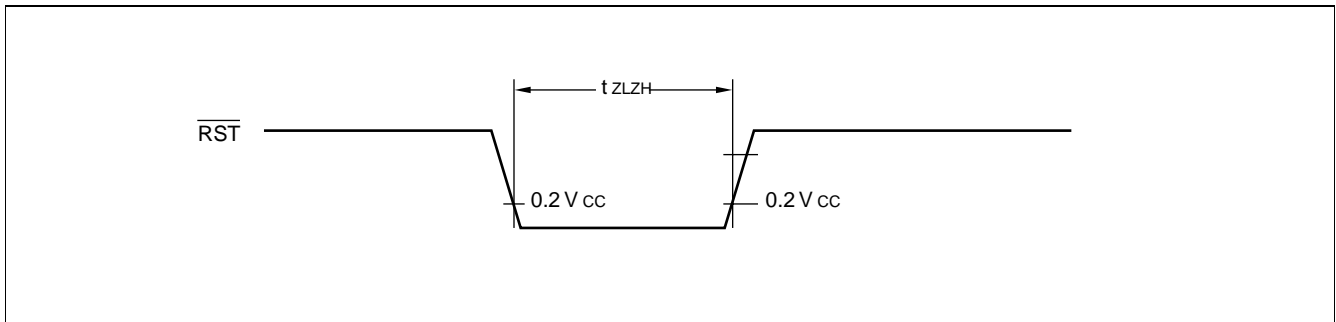
5. AC Characteristics

(1) Reset Timing

($V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{\text{RST}}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

- Notes :
- t_{HCYL} is the oscillation cycle ($1/F_{\text{CH}}$) to input to the X0 pin.
 - If the reset pulse applied to the external reset pin ($\overline{\text{RST}}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{\text{RST}}$) .

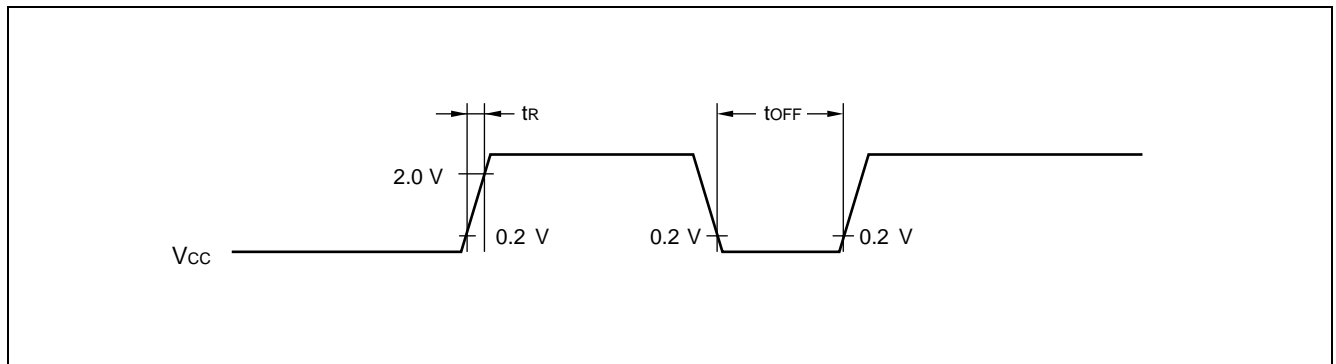


(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{R}	—	0.5	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

- Note : Make sure that power supply rises within the selected oscillation stabilization time.
 For example, when the main clock is operating at 10 MHz (F_{CH}) and the oscillation stabilization time select option has been set to $2^{18}/F_{\text{CH}}$, the oscillation stabilization delay time is 26.2 ms. Therefore, the maximum value of power supply rising time is about 26.2 ms.
 Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



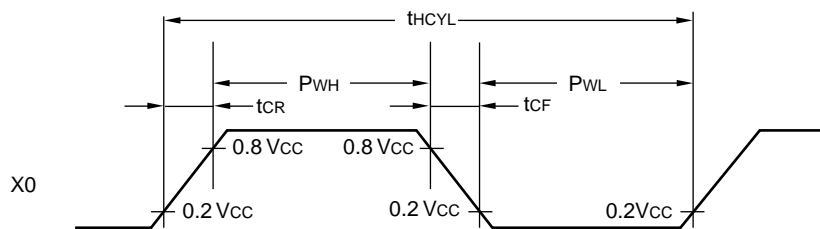
MB89560A Series

(3) Clock Timing

($V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

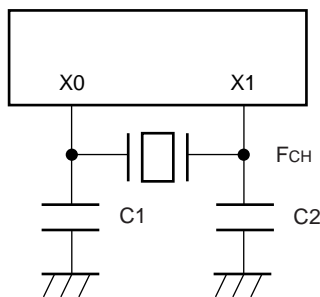
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	1	—	12.5	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	80	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

X0 and X1 Timing and Conditions

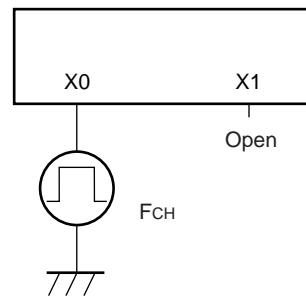


Main Clock Conditions

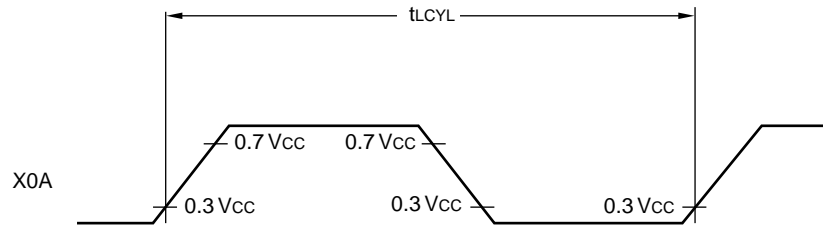
When using a crystal oscillator or ceramic oscillator



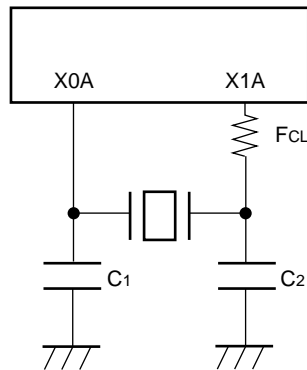
When using an external clock



X0A and X1A Timing



When using a crystal oscillator



Note : External clock is not available.

(4) Instruction Cycle

($A_{VSS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	μs	$t_{inst} = 0.32 \mu\text{s}$ when operating at $F_{CH} = 12.5 \text{ MHz}$ ($4/F_{CH}$)
		$2/F_{CL}$	μs	$t_{inst} = 61.036 \mu\text{s}$ when operating at $F_{CL} = 32.768 \text{ kHz}$

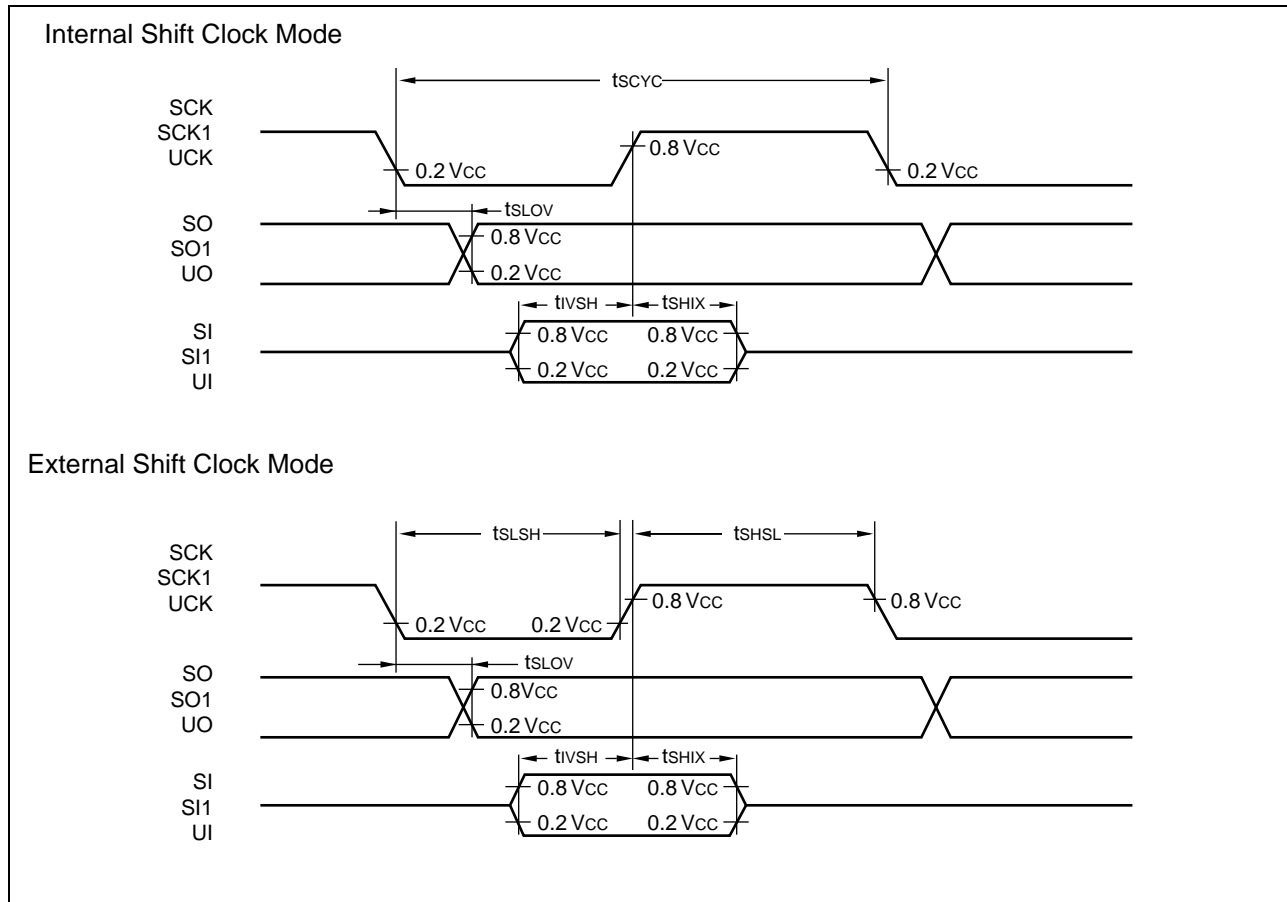
MB89560A Series

(5) Serial I/O Timing

(V_{CC} = 5.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK, SCK1, UCK	Internal shift clock mode	2 t _{inst} *	—	μs	
SCK ↓ → SO time	t _{SLOV}	SCK, SO, SCK1, SO1, UCK, UO		-200	+200	ns	
Valid SI → SCK ↑	t _{IVSH}	SI, SCK, SI1, SCK1, UI, UCK		200	—	ns	
SCK ↑ → valid SI hold time	t _{SHIX}	SCK, SI, SCK1, SI1, UCK, UI		200	—	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK, SCK1, UCK	External shift clock mode	1 t _{inst} *	—	μs	
Serial clock "L" pulse width	t _{LSLH}			1 t _{inst} *	—	μs	
SCK ↓ → SO time	t _{SLOV}	SCK, SO, SCK1, SO1, UCK, UO		0	200	ns	
Valid SI → SCK ↑	t _{IVSH}	SI, SCK, SI1, SCK1, UI, UCK		200	—	ns	
SCK ↑ → valid SI hold time	t _{SHIX}	SCK, SI, SCK1, SI1, UCK, UI		200	—	ns	

* : For information on t_{inst}, see "(4) Instruction Cycle."

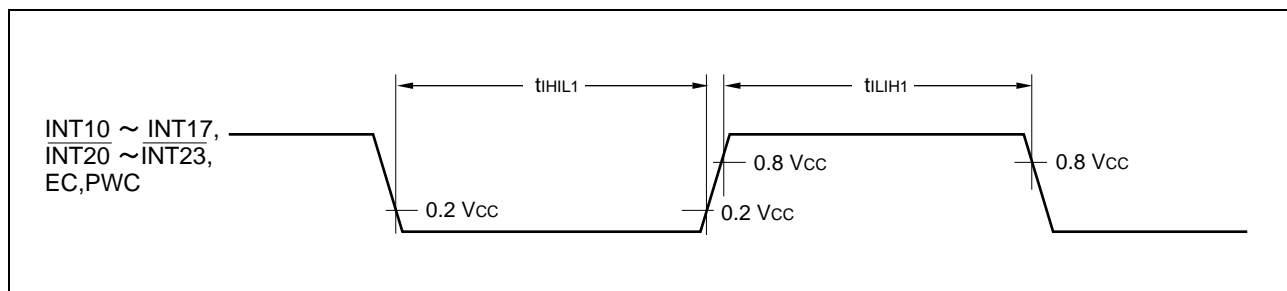


(6) Peripheral Input Timing

($V_{CC} = 5.0V$, $AV_{SS} = V_{SS} = 0.0V$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Peripheral input "H" pulse width 1	t_{LIH1}	INT10 to INT17, INT20 to INT23, EC, PWC	—	$2 t_{inst}^*$	—	μs	
Peripheral input "L" pulse width 1	t_{HIL1}			$2 t_{inst}^*$	—	μs	

* : For information on t_{inst} , see "(4) Instruction Cycle."



MB89560A Series

(7) I²C timing

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Start condition output	t _{STA}	SCL SDA	—	$\frac{1}{4} t_{inst}^{*1} \times M^{*2} \times N^{*3} - 20$	$\frac{1}{4} t_{inst} \times M^{*2} \times N^{*3} + 20$	ns	Master mode
Stop condition output	t _{STO}	SCL SDA	—	$\frac{1}{4} t_{inst} \times (M^{*2} \times N^{*3} + 8) - 20$	$\frac{1}{4} t_{inst} \times (M^{*2} \times N^{*3} + 8) + 20$	ns	Master mode
Start condition detect	t _{STA}	SCL SDA	—	$\frac{1}{4} t_{inst} \times 6 + 40$	—	ns	
Stop condition detect	t _{STO}	SCL SDA	—	$\frac{1}{4} t_{inst} \times 6 + 40$	—	ns	
Re-start condition output	t _{STASU}	SCL SDA	—	$\frac{1}{4} t_{inst} \times (M^{*2} \times N^{*3} + 8) - 20$	$\frac{1}{4} t_{inst} \times (M^{*2} \times N^{*3} + 8) + 20$	ns	Master mode
Re-start condition detect	t _{STASU}	SCL SDA	—	$\frac{1}{4} t_{inst} \times 4 + 40$	—	ns	
SCL output LOW width	t _{LOW}	SCL	—	$\frac{1}{4} t_{inst} \times M^{*2} \times N^{*3} - 20$	$\frac{1}{4} t_{inst} \times M^{*2} \times N^{*3} + 20$	ns	Master mode
SCL output HIGH width	t _{HIGH}	SCL	—	$\frac{1}{4} t_{inst} \times (M^{*2} \times N^{*3} + 8) - 20$	$\frac{1}{4} t_{inst} \times (M^{*2} \times N^{*3} + 8) + 20$	ns	Master mode
SDA output delay	t _{DO}	SDA	—	$\frac{1}{4} t_{inst} \times 4 - 20$	$\frac{1}{4} t_{inst} \times 4 + 20$	ns	
SDA output setup time after interrupt	t _{DOSU}	SDA	—	$\frac{1}{4} t_{inst} \times 4 - 20$	—	ns	*4
SCL input LOW pulse width	t _{LOW}	SCL	—	$\frac{1}{4} t_{inst} \times 6 + 40$	—	ns	
SCL input HIGH pulse width	t _{HIGH}	SCL	—	$\frac{1}{4} t_{inst} \times 2 + 40$	—	ns	
SDA input setup time	t _{SU}	SDA	—	40	—	ns	
SDA hold time	t _{HO}	SDA	—	0	—	ns	

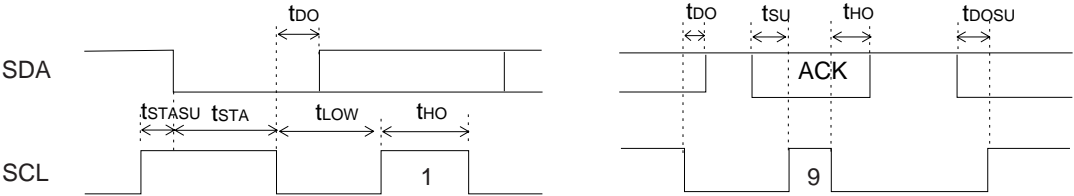
*1 : For information in t_{inst}, see " (4) Instruction Cycle".

*2 : M is defined in the ICCR CS4 and CS3 (bit 4 to bit 3) . For details, please refer to the H/W manual register explanation.

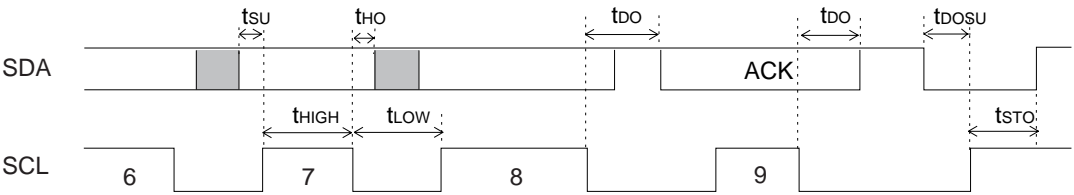
*3 : N is defined in the ICCR CS2 to CS0 (bit 2 to bit 0) .

*4 : When the interrupt period is greater than SCL "L" width, SDA and SCL output (Standard) value is based on hypothesis when rising time is 0 ns.

Data transmit (master/slave)



Data receive (master/slave)



MB89560A Series

6. A/D Converter Electrical Characteristics

(1) For MB89567A/AC A/D Converter

(AV_{CC} = 2.7 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	—	10	bit	1LSB = AVR/1024
Total error			—	—	±3.0	LSB		
Non-linearity error			—	—	±2.5	LSB		
Differential linearity error			—	—	±1.9	LSB		
Zero transition voltage	V _{OT}	—	AVR=AV _{CC}	AV _{SS} - 1.5 LSB	AV _{SS} + 0.5 LSB	AV _{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V _{FST}		AVR - 3.5 LSB	AVR - 1.5 LSB	AVR + 1.5 LSB	mV		
Interchannel disparity	—		—	—	4	LSB	1LSB = AVR/1024	
A/D mode conversion time *3	—	—	—	—	60 t _{inst} *1	—	μs	
A/D Sampling time				—	16 t _{inst} *1	—		
Analog port input current	I _{AIN}	ANO to AN7	—	—	—	10	μA	
Analog input voltage	V _{AIN}	—	—	AV _{SS}	—	AVR	V	
Power supply current	I _A	AV _{CC}	—	—	4	6	mA	when A/D conversion is activated
	I _{AH}	—	T _A = +25 °C	—	1	5	μA	when A/D conversion is stopped
Reference voltage	—	—	—	AV _{SS} +3.5	—	AV _{CC}	V	
Reference voltage supply current	I _R	AVR	A/D is Activated	—	200	—	μA	
	I _{RH}	—	A/D is Stopped	—	—	5	μA	*2

*1 : For information on t_{inst}, see “(4) Instruction Cycle” in “5. AC Characteristics.”

*2 : When A/D conversion is not in operation, and the CPU is in STOP mode.

*3 : Included sampling time

MB89560A Series

(2) For MB89P568/PV560 A/D Converter

(AV_{CC}=3.5 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	—	10	bit	1LSB = AVR/1024
Total error				—	—	±3.0	LSB	
Non-linearity error				—	—	±2.5	LSB	
Differential linearity error				—	—	±1.9	LSB	
Zero transition voltage	V _{OT}	—	AVR=AV _{CC}	AV _{SS} - 1.5 LSB	AV _{SS} + 0.5 LSB	AV _{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V _{FST}			AVR - 3.5 LSB	AVR - 1.5 LSB	AVR + 1.5 LSB	mV	
Interchannel disparity	—			—	—	4	LSB	1LSB = AVR/1024
A/D mode conversion time *3	—	—	—	—	60 t _{inst} *1	—	μs	
A/D Sampling time				—	16 t _{inst} *1	—		
Analog port input current	I _{AIN}	AN0 to AN7	—	—	—	10	μA	
Analog input voltage	V _{AIN}			AV _{SS}	—	AVR	V	
Power supply current	I _A	AV _{CC}	—	—	4	6	mA	when A/D conversion is activated
	I _{AH}		T _A = +25 °C	—	1	5	μA	when A/D conversion is stopped
Reference voltage	—	AVR	—	AV _{SS} + 3.5	—	AV _{CC}	V	
Reference voltage supply current	I _R		A/D is Activated	—	400	—	μA	
	I _{RH}		A/D is Stopped	—	—	5	μA	*2

*1 : For information on t_{inst}, see “(4) Instruction Cycle” in “5. AC Characteristics.”

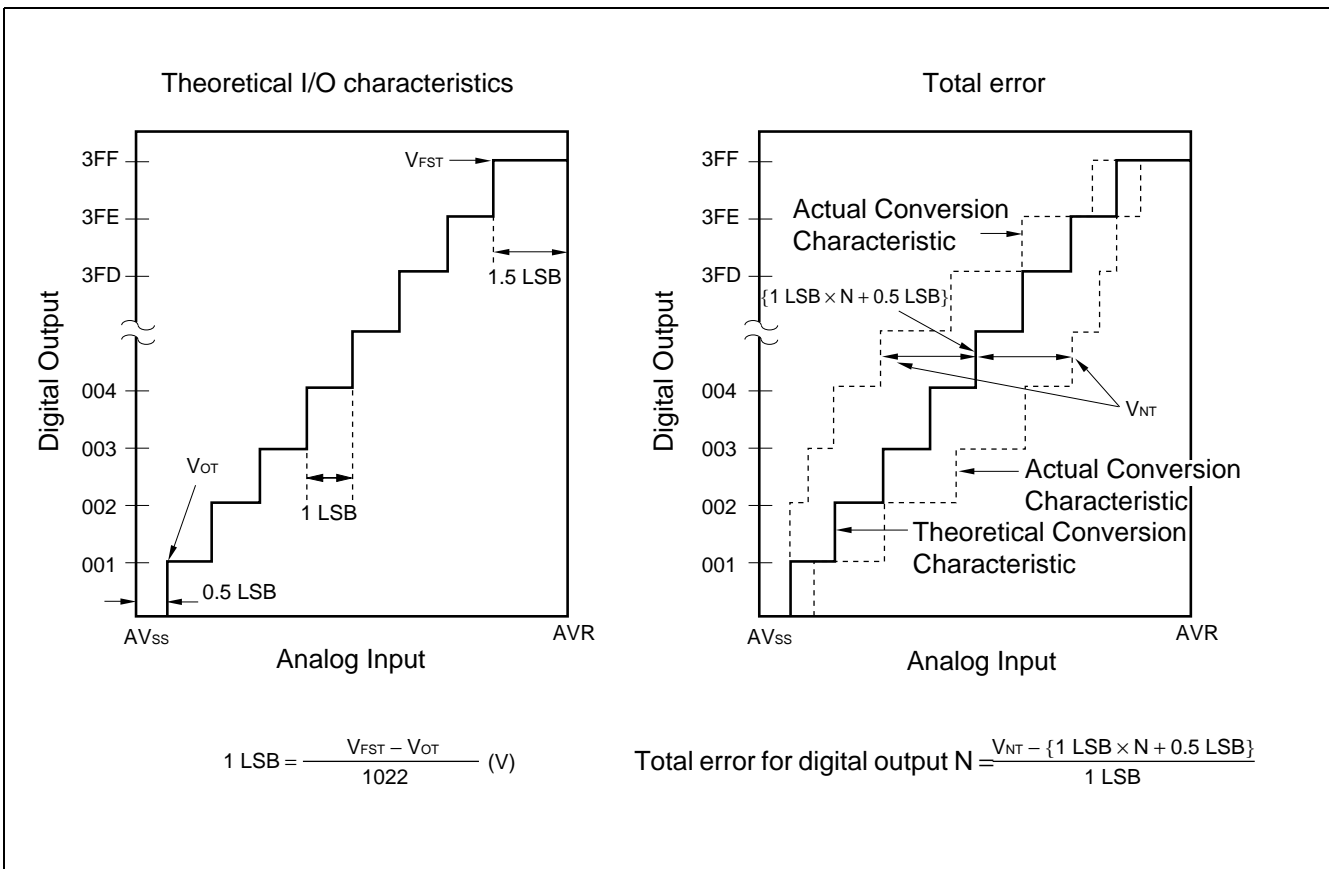
*2 : When A/D conversion is not in operation, and the CPU is in STOP mode.

*3 : Included sampling time

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(3) A/D Converter Glossary

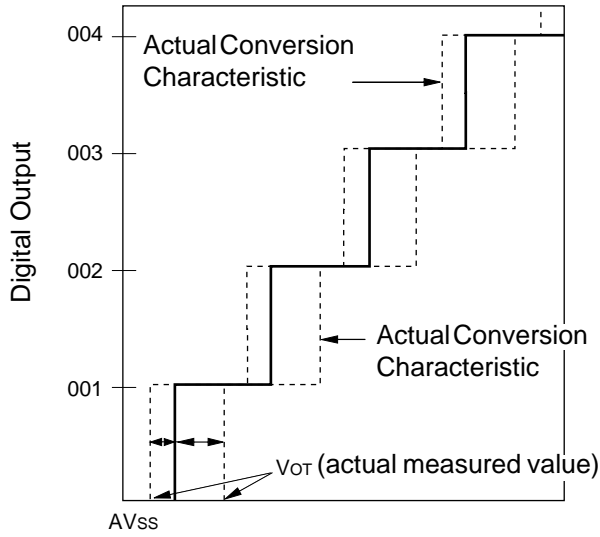
- Resolution
Analog changes that are identifiable with the A/D converter.
- Linearity error
The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



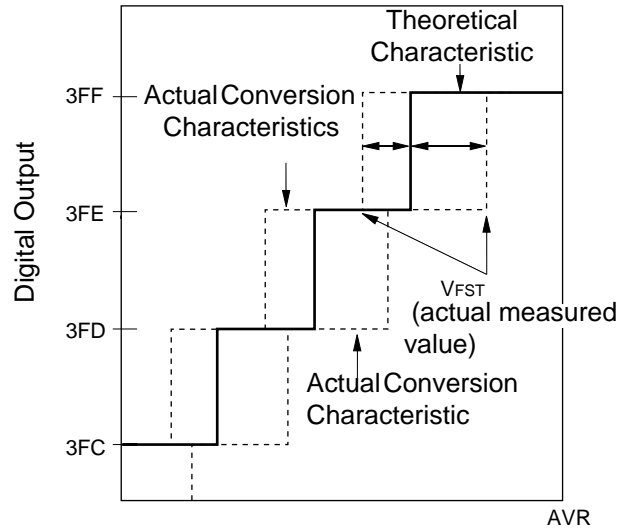
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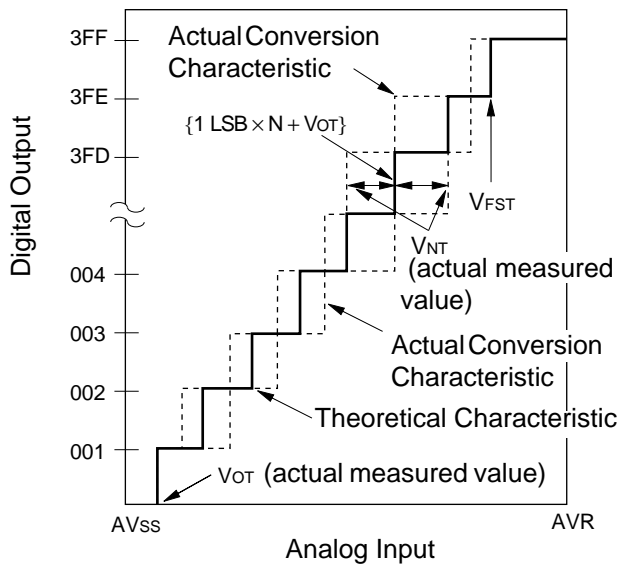
Zero transition error



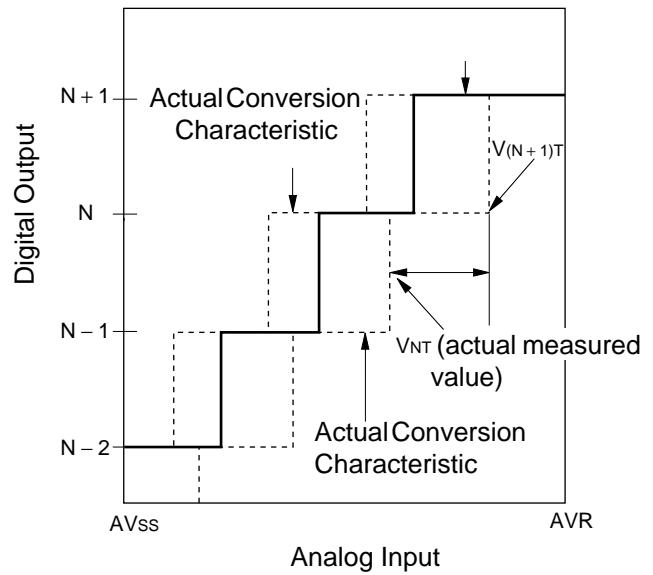
Full-scale transition error



Linearity error



Differential linearity error



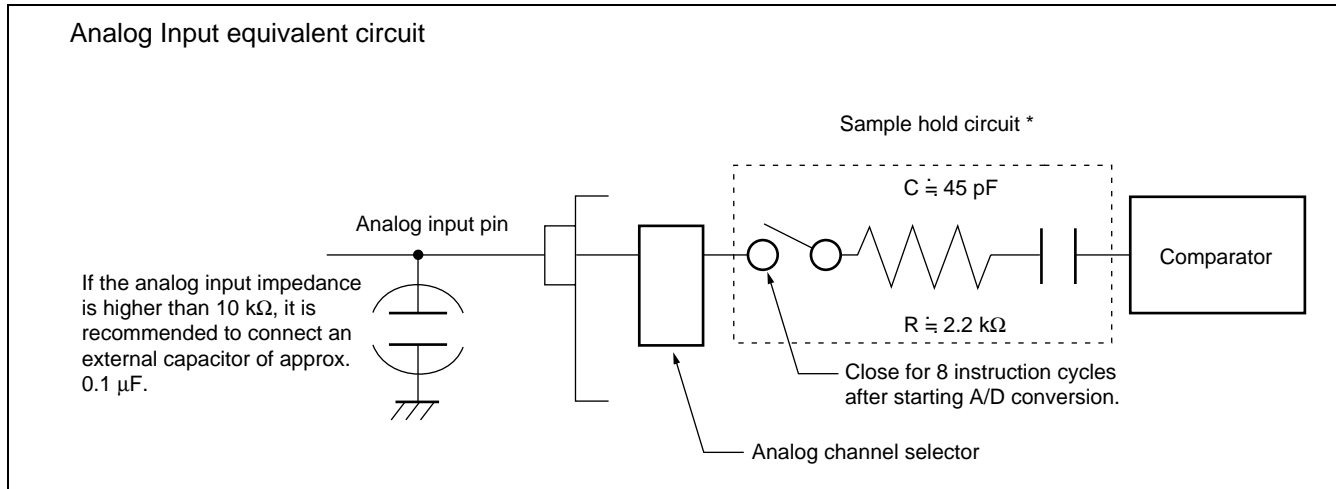
$$\text{Linearity error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + 0.5 \text{ LSB}\}}{1 \text{ LSB}}$$

$$\text{Differential linearity error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

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(4) Precautions

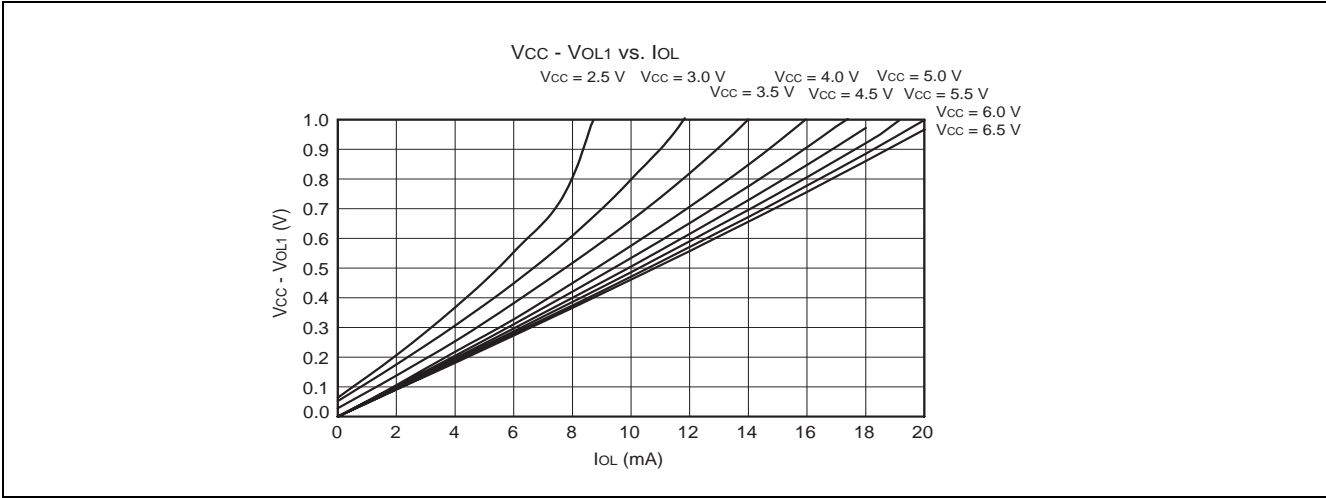
- The smaller the $|AVR - AV_{SS}|$ is, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions :
Output impedance of the external circuit < Approx. $10\text{ k}\Omega$
- If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient.



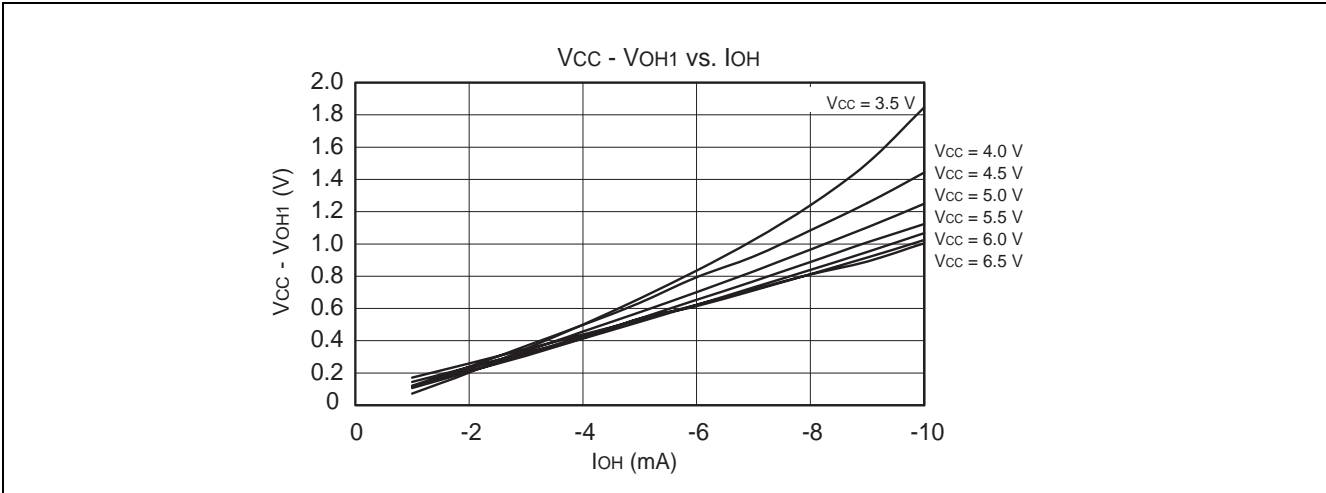
- * : The value of R and C at the sample hold circuit depends on the following.
- MB89567A/MB89567AC : $R \approx 2.2\text{ k}\Omega$, $C \approx 45\text{ pF}$
- MB89P568/MB89PV560 : $R \approx 1.4\text{ k}\Omega$, $C \approx 64\text{ pF}$

EXAMPLE CHARACTERISTICS

(1) "L" Level Output Voltage

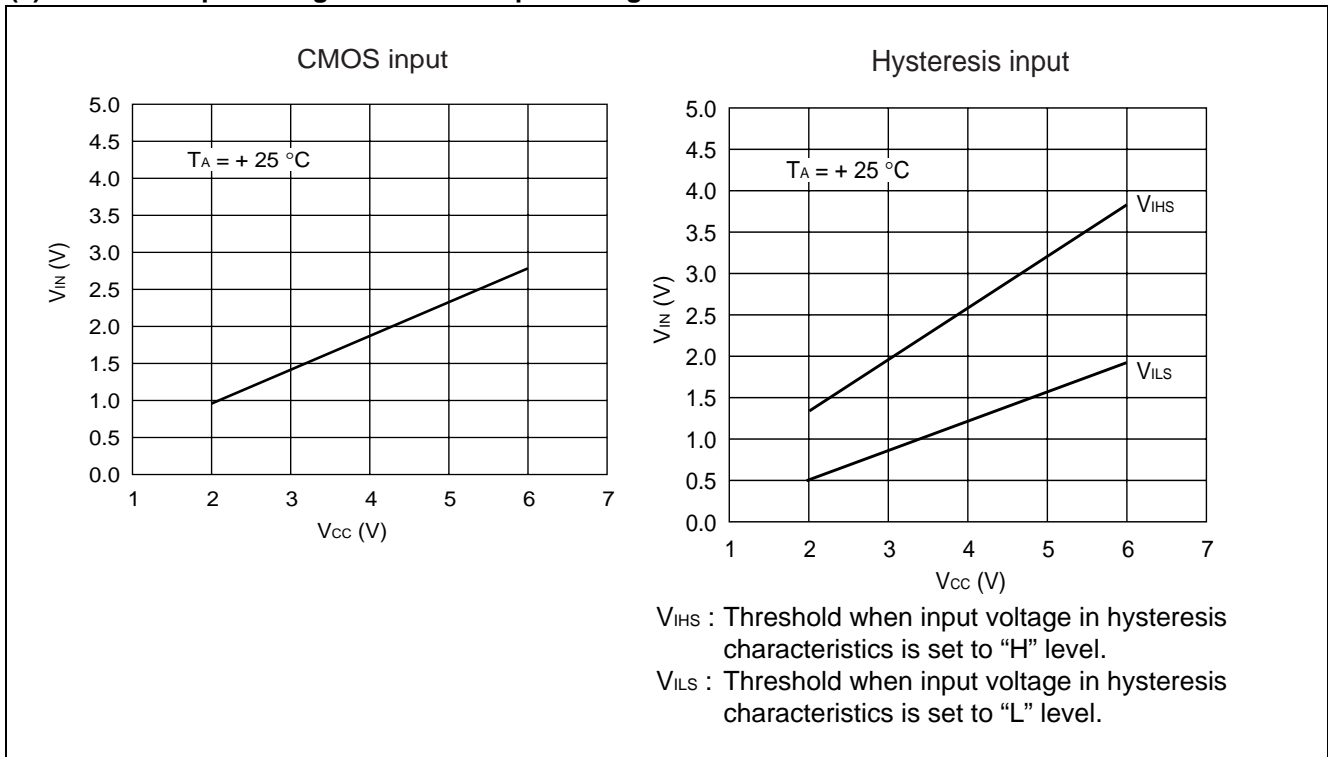


(2) "H" Level Output Voltage

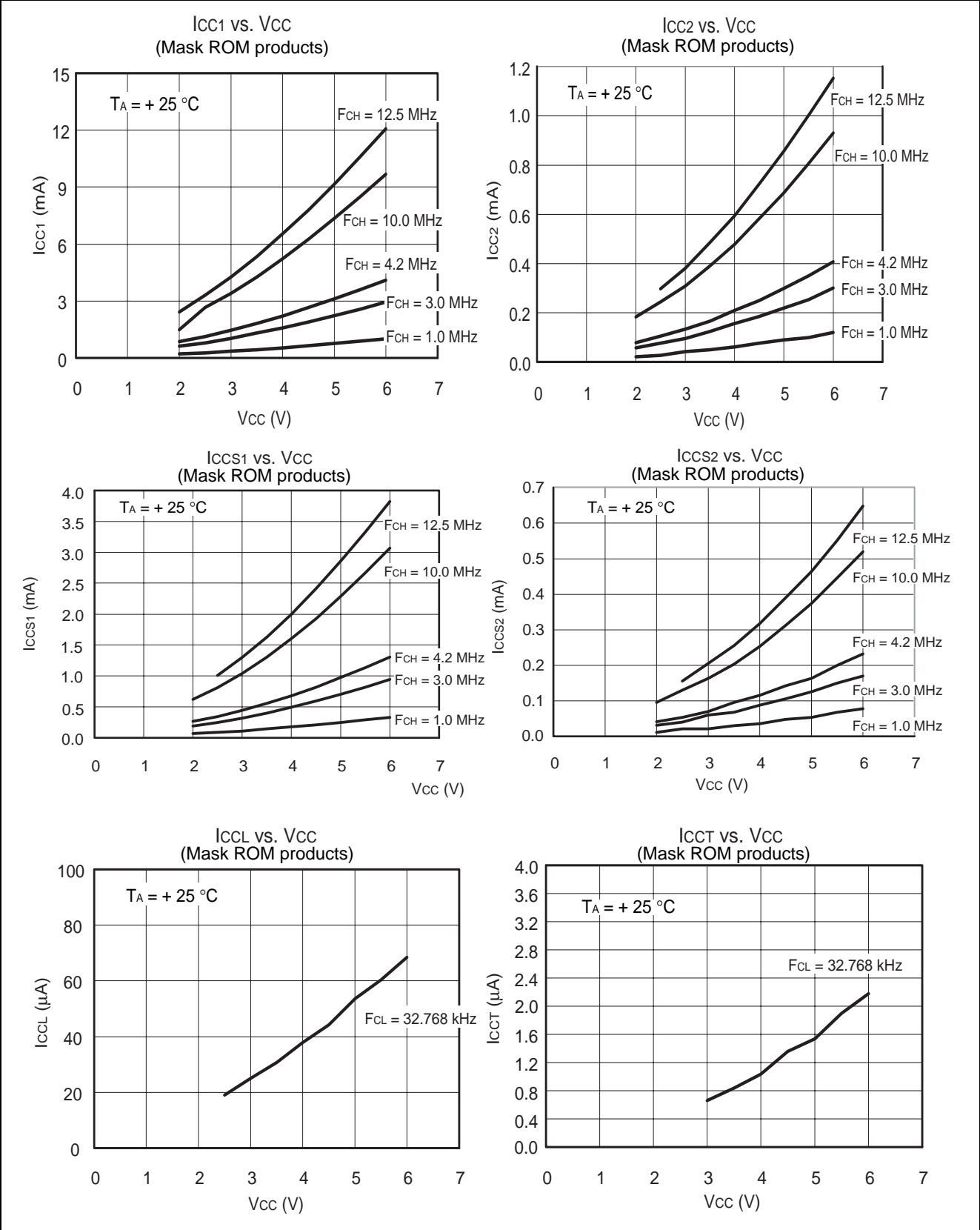


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(3) "H" Level Input Voltage / "L" Level Input Voltage



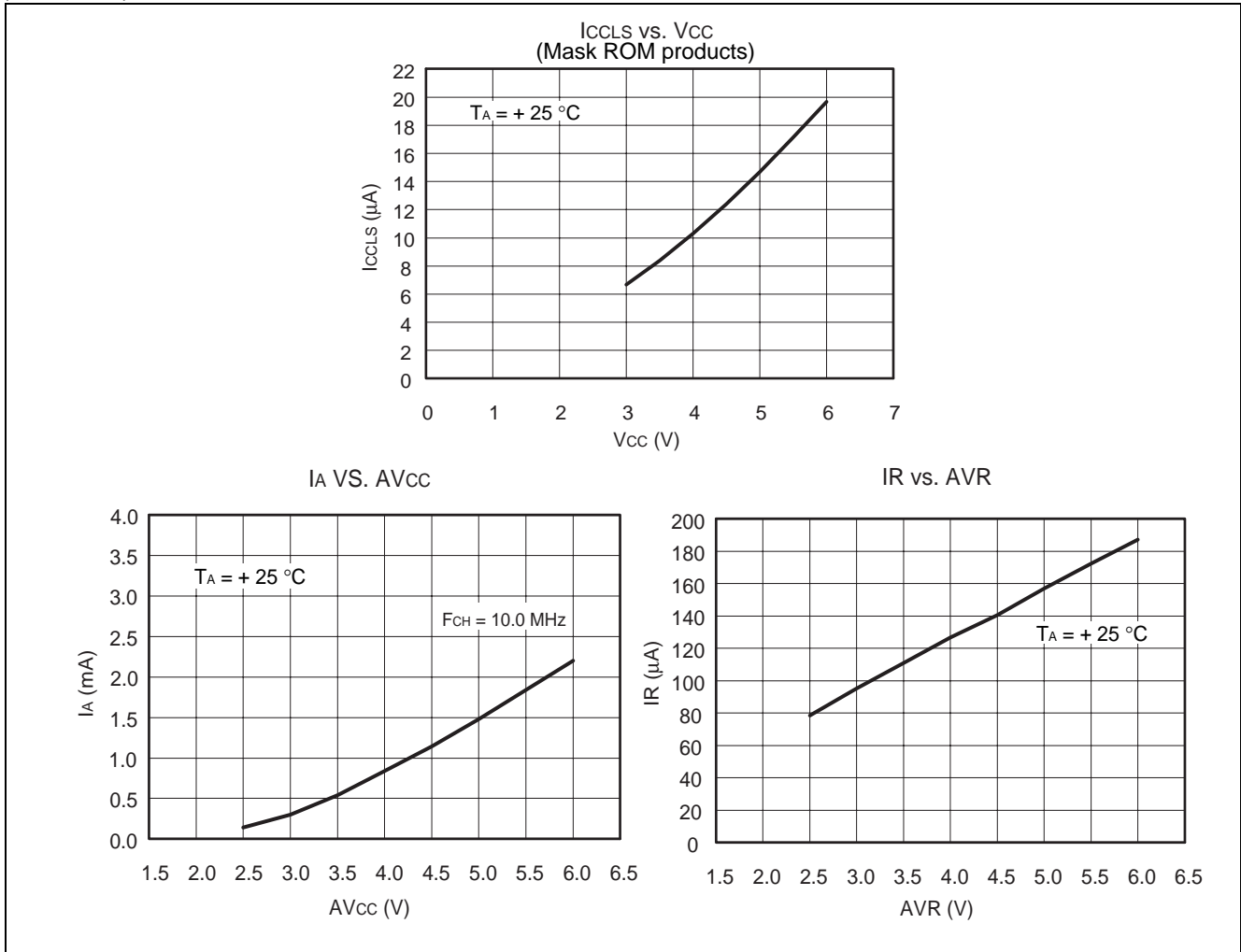
(4) Power Supply Current (External Clock)



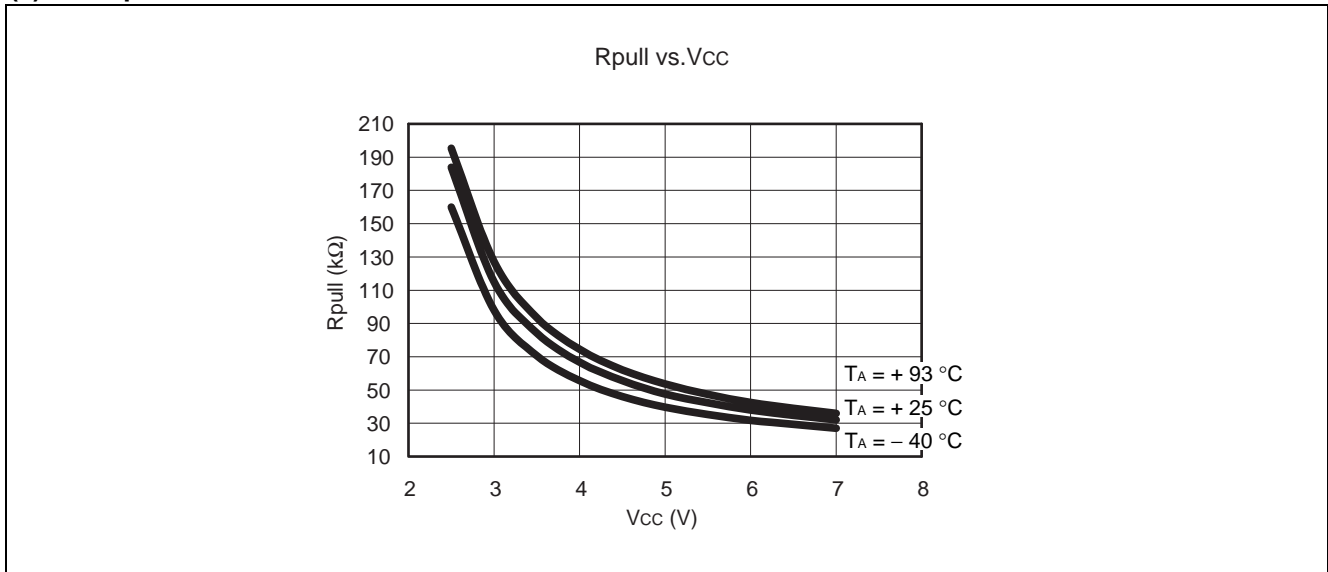
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MB89560A Series

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(5) Pull-up Resistance



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■ MASK OPTIONS

No.	Model	MB89567A MB89567AC	MB89P568	MB89PV560
	Specification method	Specify when ordering mask.	Setting unavailable.	Setting unavailable.
1	Main clock oscillation stabilization delay time initial value* selection ($F_{CH} = 10 \text{ MHz}$) <ul style="list-style-type: none"> • 01: $2^{14}/F_{CH}$ (Approx. 1.6 ms) • 10: $2^{17}/F_{CH}$ (Approx. 13.1 ms) • 11: $2^{18}/F_{CH}$ (Approx. 26.2 ms) 	Selectable	$2^{18}/F_{CH}$ (Approx. 26.2 ms)	$2^{18}/F_{CH}$ (approx. 26.2 ms)
2	LCD driving power supply <ul style="list-style-type: none"> • On-chip voltage booster • Internal voltage divider (external divider resistors can be used) 	Selectable	-101 Internal voltage divider -102 On-chip voltage booster	-101 Internal voltage divider -102 On-chip voltage booster

■ ORDERING INFORMATION

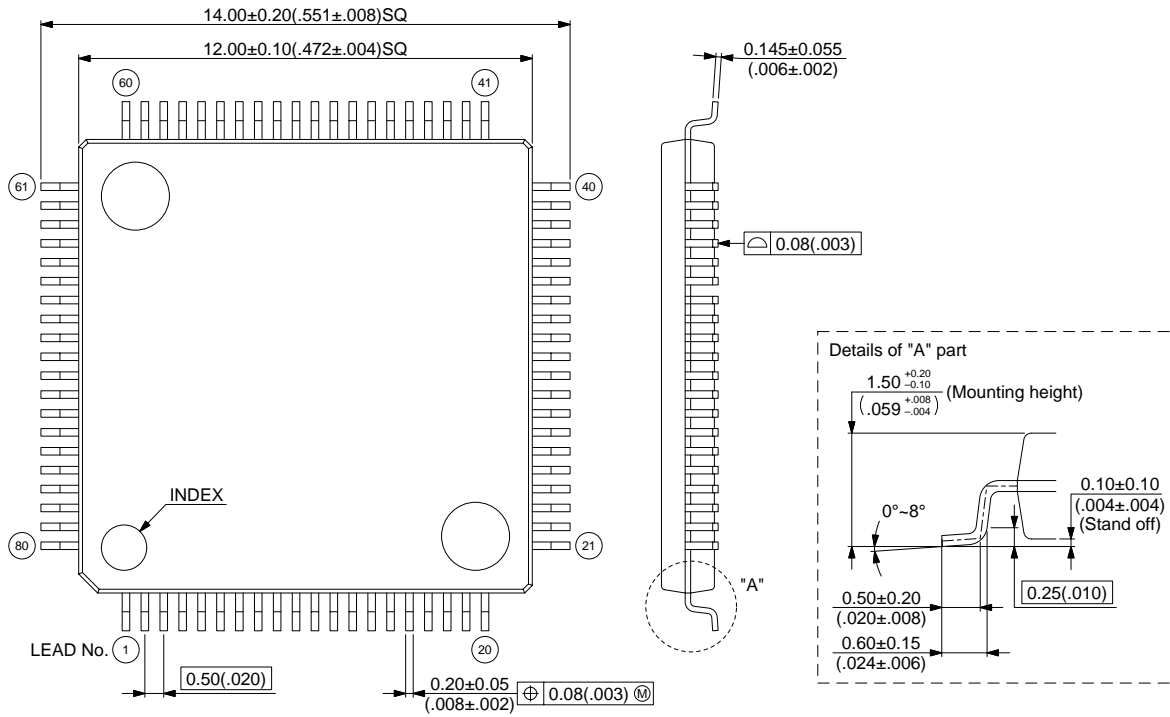
Part number	Package	Remarks
MB89567APFV MB89567ACPFV MB89P568PFV-101	80-pin Plastic LQFP (FPT-80P-M05)	Without Booster Resistor divider
MB89567APFV MB89567ACPFV MB89P568PFV-102		With Booster
MB89567APF MB89567ACPF MB89P568PF-101	80-pin Plastic QFP (FPT-80P-M06)	Without Booster Resistor divider
MB89567APF MB89567ACPF MB89P568PF-102		With Booster
MB89567APFM MB89567ACPFM MB89P568PFM-101	80-pin Plastic LQFP (FPT-80P-M11)	Without Booster Resistor divider
MB89567APFM MB89567ACPFM MB89P568PFM-102		With Booster
MB89PV560CF-101	80-pin Ceramic MQFP (MQP-80C-P01)	Without Booster Resistor divider
MB89PV560CF-102		With Booster

MB89560A Series

■ PACKAGE DIMENSIONS

80-pin plastic LQFP
(FPT-80P-M05)

*Pins width and pins thickness include plating thickness.



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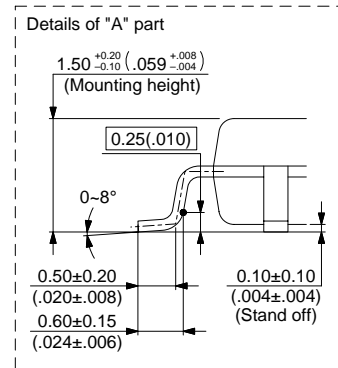
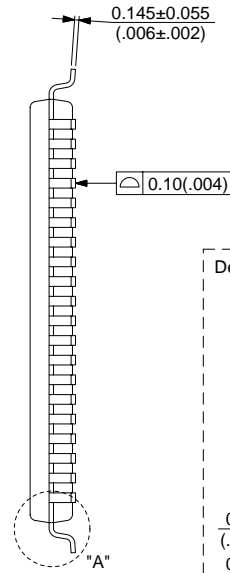
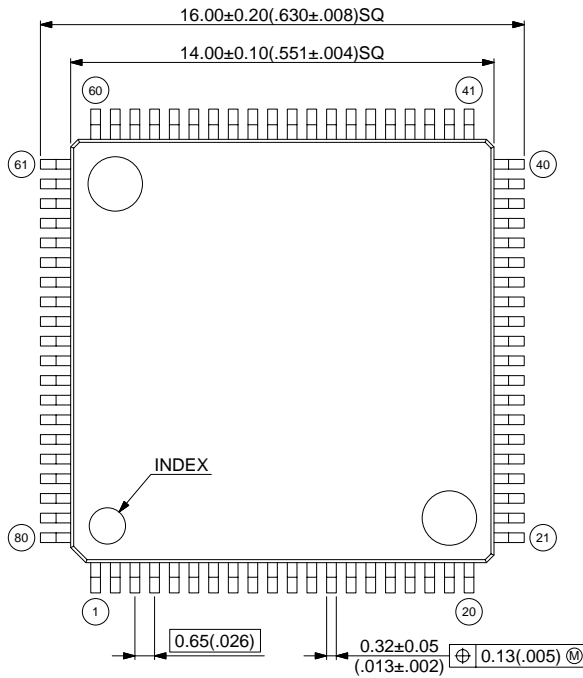
Dimensions in mm (inches)

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MB89560A Series

80-pin plastic LQFP
(FPT-80P-M11)

*Pins width and pins thickness include plating thickness.



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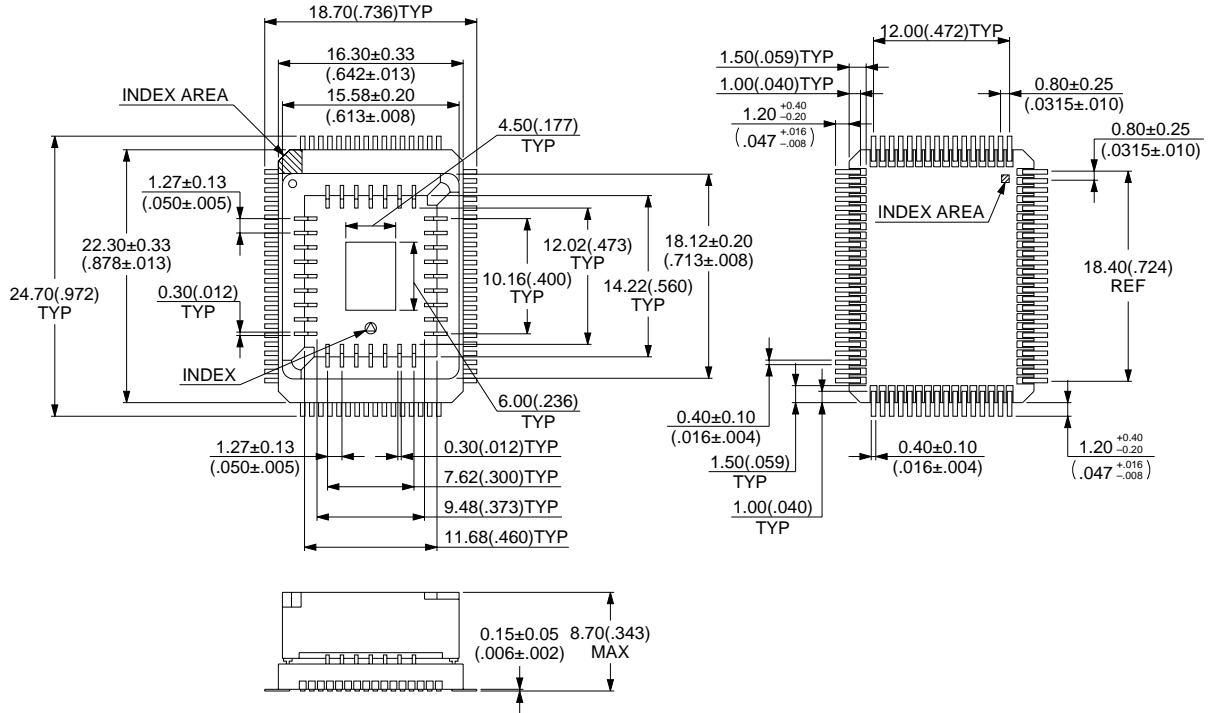
Dimensions in mm (inches)

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MB89560A Series

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80-pin ceramic
(MQP-80C-P01)



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Dimensions in mm (inches)

MB89560A Series

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