GLT440M04

1M X 4 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Apr. 2002 (Rev. 2.2)

Features :

* 1,048,576 words by 4 bits organization.
* Fast access time and cycle time
* Low power dissipation.
* Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh.
* 1,024 refresh cycles per 16ms.
* Available in 300 mil 20/26pin TSOPII.
* 2.5V±0.2V Vcc Power Supply voltage.
* All inputs and Outputs are LVTTL compatible.
* Extended Data-Out (EDO) Page access cycle.
* Self-refresh Capability.

Description :

The GLT440M04 is a high-performance CMOS dynamic random access memory containing 4,194,304 bits organized in a x4 configuration. The GLT440M04 offers page cycle access with Extended Data Output. The GLT440M04 has 10 row- and 10 column-addresses, and accepts 1024-cycle refresh in 16 ms.

The GLT440M04 provides EDO PAGE MODE operation which allows for fast data access within a row-address defined boundary, up to 1024 x 4 bits with cycle times as short as 25ns.

HIGH PERFORMANCE	**60**	**70**
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	25 ns	30 ns
Min. Read/Write Cycle Time, (t_{RC})	104 ns	124 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	15 ns	20 ns

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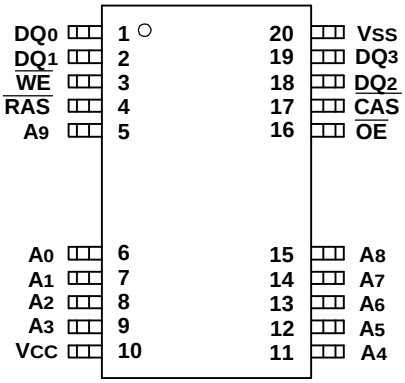
Santa Clara, CA 95051, U.S.A.

G-Link Technology Corporation,Taiwan
6F, No. 24-2, Industry E. RD. IV, Science Based
Industrial Park, Hsin Chu, Taiwan.

Pin Configuration :

GLT440M04
300mil 20/26 TSOPII



Pin Descriptions:

Name	Function
A_0 - A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_3	Data Inputs / Outputs
V_{CC}	+2.5V Power Supply
V_{SS}	Ground
NC	No Connection

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Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....0°C to +70°C
For Extended Temperature ……-25°C to +85°C
Storage Temperature(plastic).....-55°C to +150°C
Voltage Relative to V_{SS}.....-0.5V to + 4.6V
Short Circuit Output Current.....20mA
Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can aversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=2.5V±0.2V, V_{SS}=0V

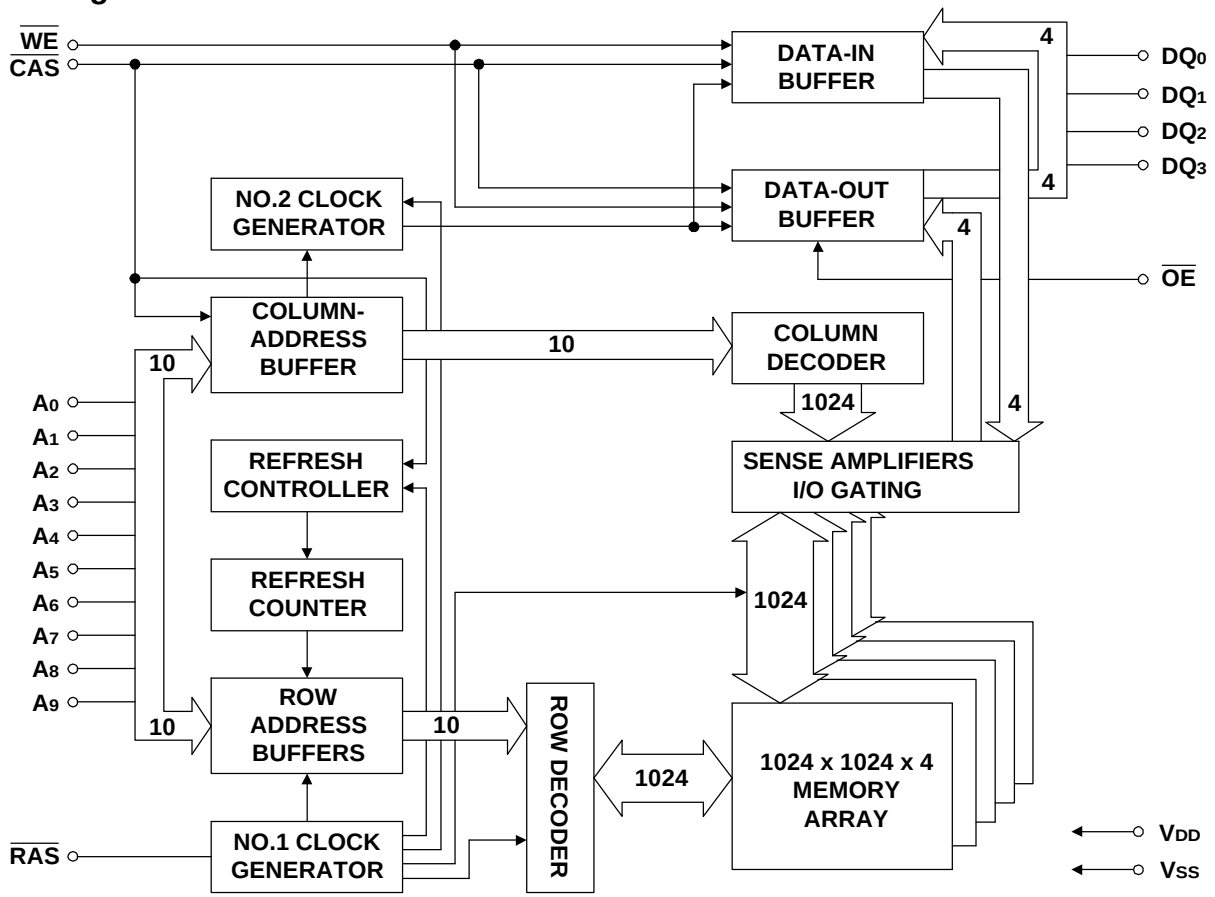
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$,, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200µs and then, execute eight $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table:

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESS		DATA-IN/OUT
						t_R	t_C	DQ0-DQ3
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out,Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out,Data-In
READ-WRITE	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out,Data-In
$\overline{RAS}$ -ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, -25°C to 85°C V_{CC}=2.5V±0.2V, V_{SS}=0V, unless otherwise specified..

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$0V \le V_{IN} \le V_{CC}+0.3V$ (All other pins not under test=0V)		-5		+5	µA	
I_{LO}	Output Leakage Current (for High-Z State)	$0V \le V_{out} \le V_{CC}$ Output is disabled (Hiz)		-5		+5	µA	
I_{CC1}	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC}$ (min.)	t_{RAC} = 60ns t_{RAC} = 70ns			80 70	mA	1,2
I_{CC2}	Standby Current	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\ge V_{SS}$				1	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$ -Only	$\overline{RAS}$ cycling, $\overline{CAS}$ at V_{IH} $t_{RC} = t_{RC}$ (min.)	t_{RAC} = 60ns t_{RAC} = 70ns			80 70	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{CAS}$ address cycling:$t_{PC}=t_{PC}$(min.)	t_{RAC} = 60ns t_{RAC} = 70ns			80 70	mA	1,2
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{CAS}$ address cycling: $t_{RC}=t_{RC}$ (min.)	t_{RAC} = 60ns t_{RAC} = 70ns			80 70	mA	2
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS} \ge V_{CC}$-0.2V, $\overline{CAS} \ge V_{CC}$-0.2V, All other inputs V_{SS}				200	µA	
I_{CC7}	Self refresh Current	$\overline{RAS} = \overline{CAS}$ =0.2V, $\overline{WE} = \overline{OE} = A_0$~$A_9$=$V_{CC}$-0.2V or 0.2V DQ_0~DQ_3=V_{CC}-0.2V,0.2V or Open				200	µA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		V_{CC}+0.3	V	4
V_{OL}	Output Low Voltage	I_{OL} = 2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2mA		1.8			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified ICC(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
3. Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to –0.9V for a period not to exceed 10ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.
4. Specified V_{IH}(max.) is steady state operation . During transitions V_{IH}(max.) may overshoot to V_{CC}+0.9V for a period not to exceed 10ns. All AC parameters are measured with V_{IL}(min.) ≥ V_{SS} and VIH(max.) ≤ V_{CC} .

AC Characteristics

T_A = 0°C to 70°C , -25°C to 85°C V_{CC} = 2.5 V ± 0.2V, VIH/VIL = 2.0/0.8 V, V_{OH}/V_{OL} = 1.6/0.6V

An initial pause of 200 µs and 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles are required after power-up.

		60		70			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Notes**
Read or Write Cycle Time	t_{RC}	104		124		ns	
Read Modify Write Cycle Time	t_{RWC}	140		170		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70	ns	1,2,3
Access Time from $\overline{CAS}$	t_{CAC}		15		20	ns	1,5,7
Access Time from Column Address	t_{AA}		30		35	ns	1,5,6
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	3		3		ns	3
$\overline{CAS}$ to Output High-Z	t_{CEZ}	3	15	3	20	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	50		50		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10k	15	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	10		15		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30		35		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	45		50		ns	
Read Command Set-Up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		ns	8,9
Write Command Hold Time	t_{WCH}	10		15		ns	
Write Command Pulse Width	t_{WP}	10		15		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15		20		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	10		15		ns	

AC Characteristics

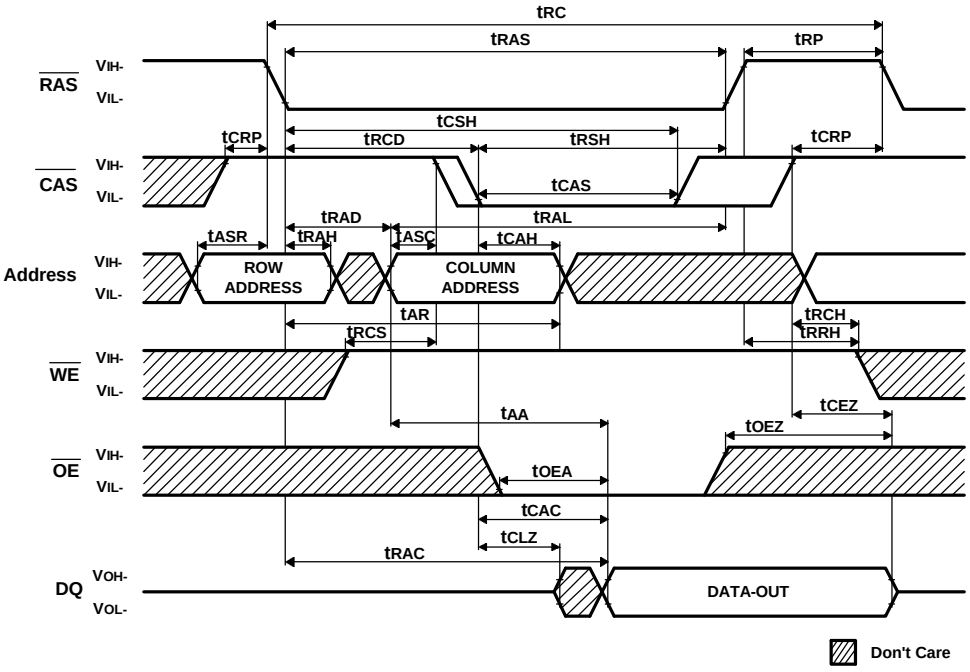
Parameter	Symbol	60		70		Unit	Notes
		Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		ns	10
Data Hold Time	t_{DH}	10		15		ns	10
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	45		50		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	79		94		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	34		44		ns	
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	49		59		ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay	t_{CPWD}	54		64		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ Before $\overline{RAS}$ counter test cycle)	t_{CPT}	20		25		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		35		40	ns	
EDO Page Mode Cycle Time	t_{PC}	25		30		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	56		71		ns	
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	10		10		ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode Only)	t_{RASP}	60	200k	70	100k	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	
Access Time from $\overline{OE}$	t_{OEA}		15		20	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	15		20		ns	
$\overline{OE}$ to Output Low-Z	t_{OLZ}	3		3		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	3	15	3	20	ns	
$\overline{WE}$ to Data Delay	t_{WED}	15		20		ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15		20		ns	
Data Output Hold after $\overline{CAS}$ low	t_{DOH}	5		5		ns	
$\overline{RAS}$ to Output High-Z	t_{REZ}	3	15	3	20	ns	
$\overline{WE}$ to Output High-Z	t_{WEZ}	3	15	3	20	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5		5		ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5		5		ns	
$\overline{WE}$ Puts width (EDO mixed read write cycle)	t_{WPE}	5		5		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CSR}	5		5		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CHR}	10		15		ns	

Parameter	Symbol	60		70		Unit	Notes
		Min.	Max.	Min.	Max.		
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{WRP}	10		10		ns	
$\overline{WE}$ to $\overline{RAS}$ hold time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{WRH}	10		10		ns	
Transition Time	t_T	2	50	2	50	ns	11
Refresh Period (1,024 cycles)	t_{REF}		16		16	ms	
Refresh Period (L-Version)	t_{REF}		128		128	ms	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ Before $\overline{RAS}$ Self refresh)	t_{RASS}	100		100		µs	
$\overline{RAS}$ precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Self refresh)	t_{RPS}	110		130		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Self refresh)	t_{CHS}	-50		-50		ns	

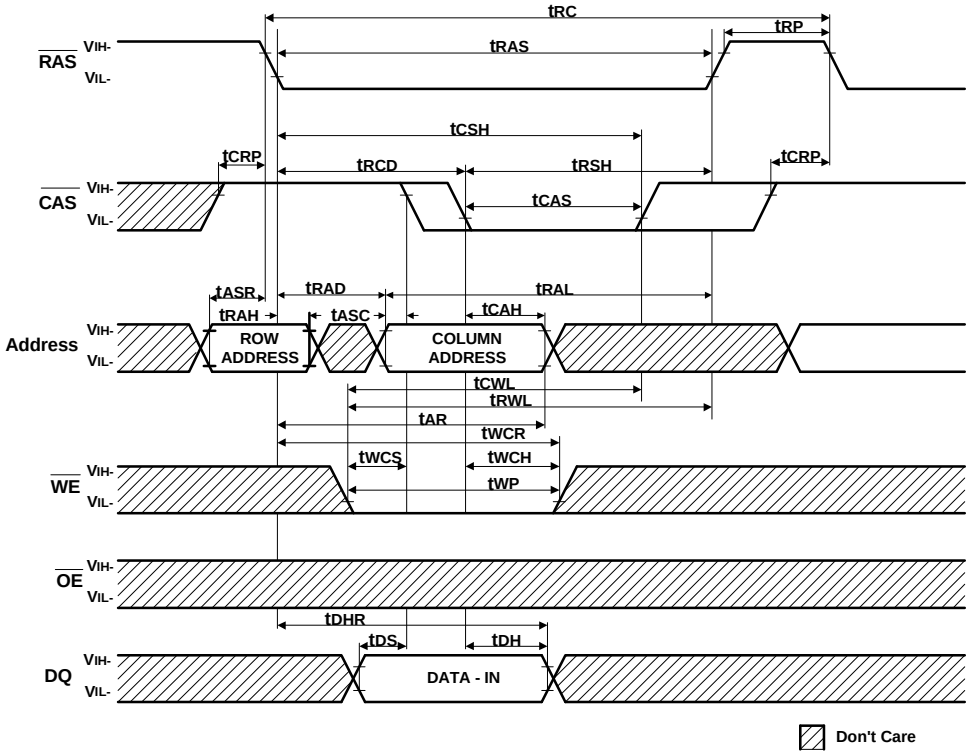
Notes:

1. Measure with a load equivalent to one TTL input and 100 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), access time will be controlled by t_{CAC}.
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA}, t_{CAC} and t_{CPA}.
6. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
7 Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
11. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 2 ns.

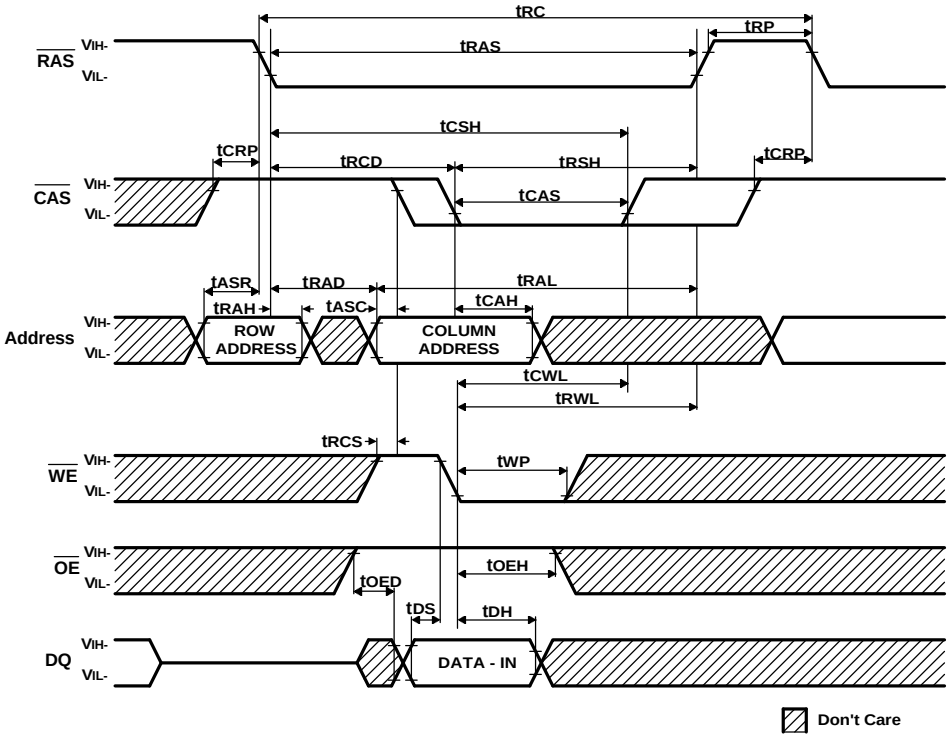
Read Cycle



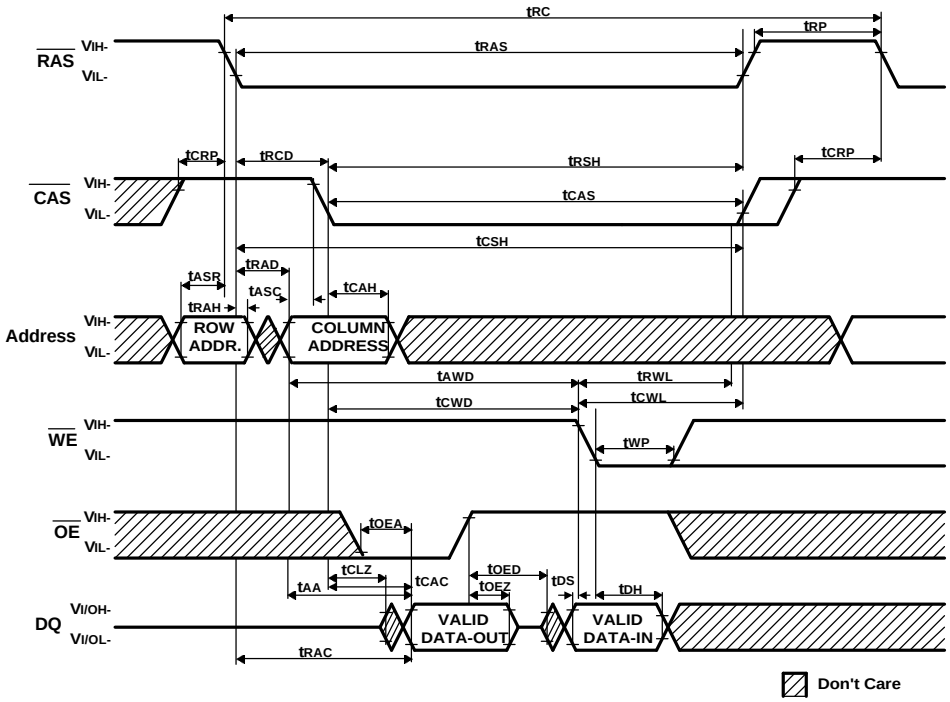
Early Write Cycle NOTE : D_{OUT} = OPEN



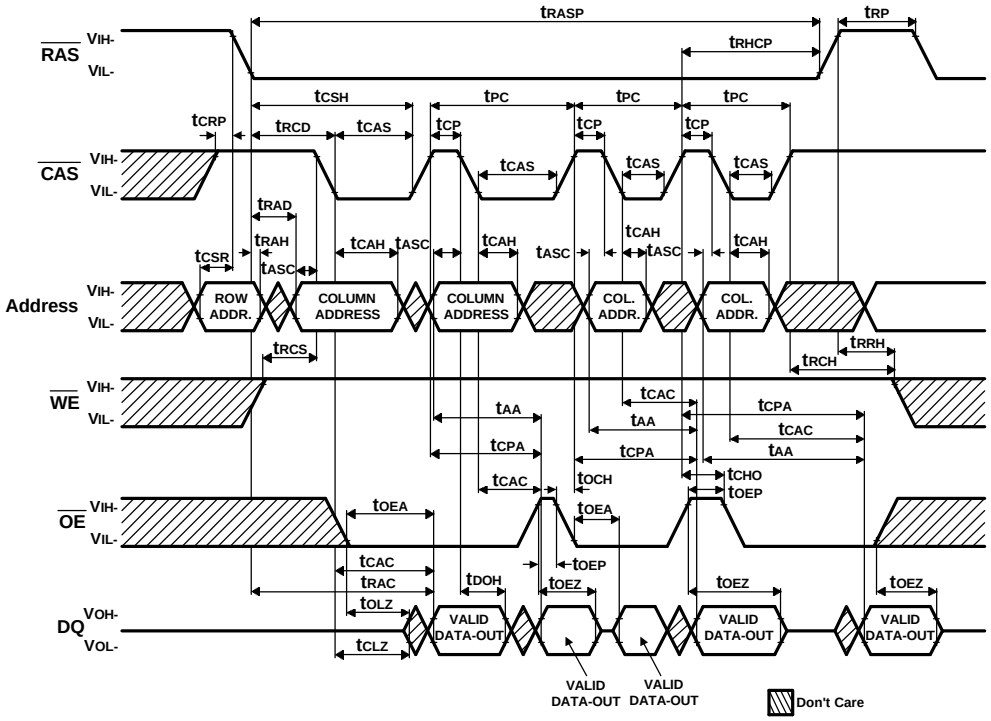
$\overline{OE}$ Controlled Write Cycle NOTE : D_{OUT} = OPEN



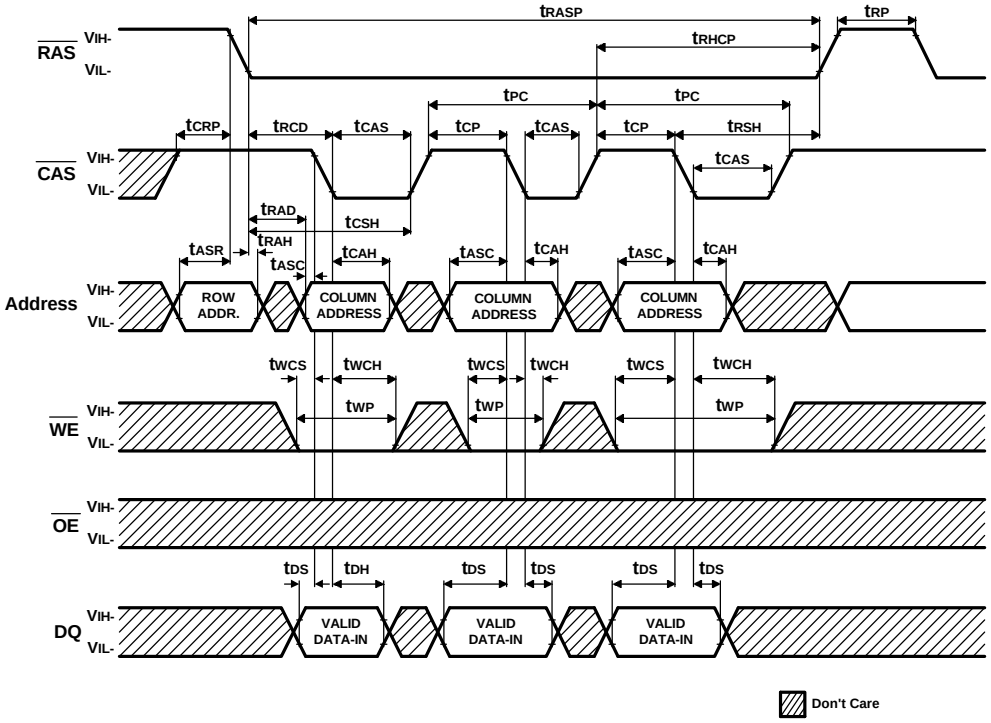
Read - Modify - Write Cycle



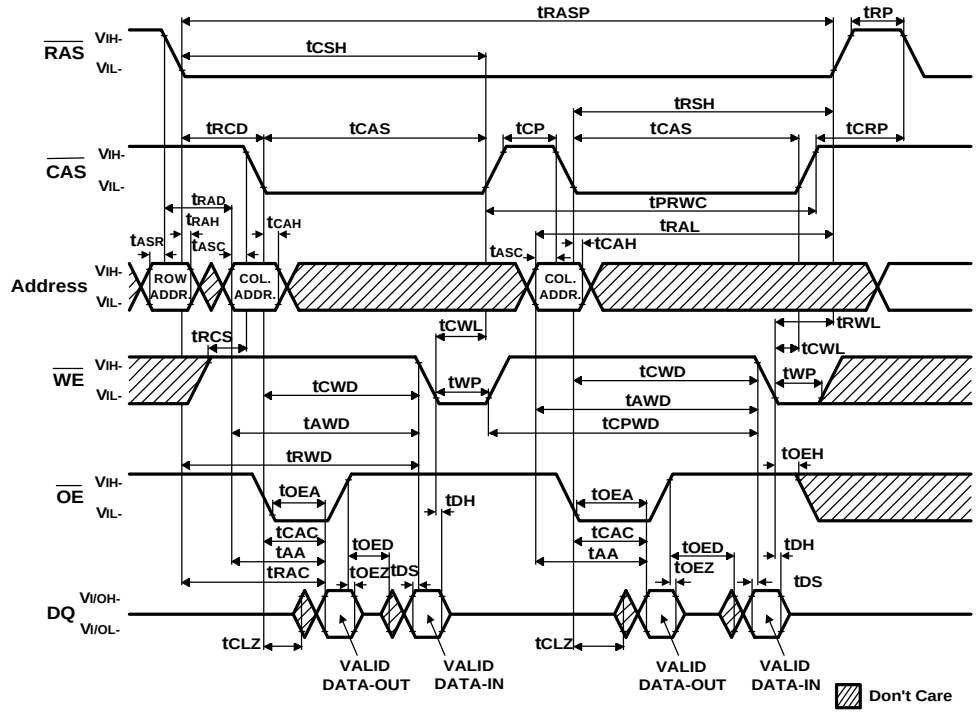
EDO Page Mode Read Cycle NOTE : D_{OUT} = OPEN



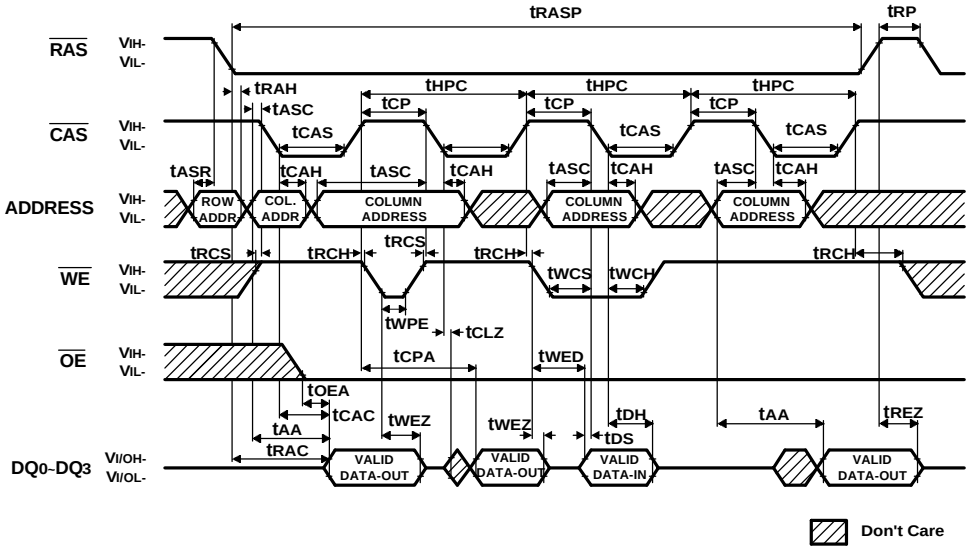
EDO Page Mode Early Write Cycle NOTE : D_{OUT} = OPEN



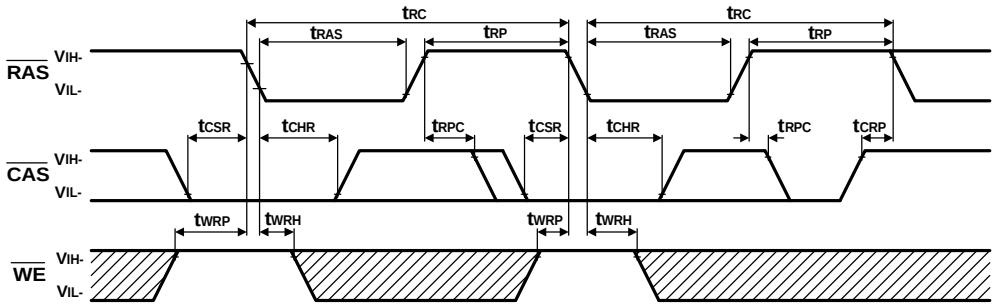
EDO Page Mode Read - Modify - Write Cycle NOTE : D_{OUT} = OPEN



EDO Page Read And Write Mixed Ccycle

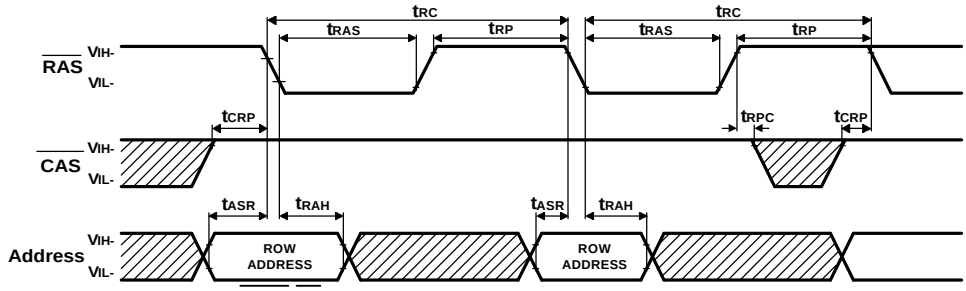


$\overline{\text{CAS}}$ - Before - $\overline{\text{RAS}}$ Refresh Cycle



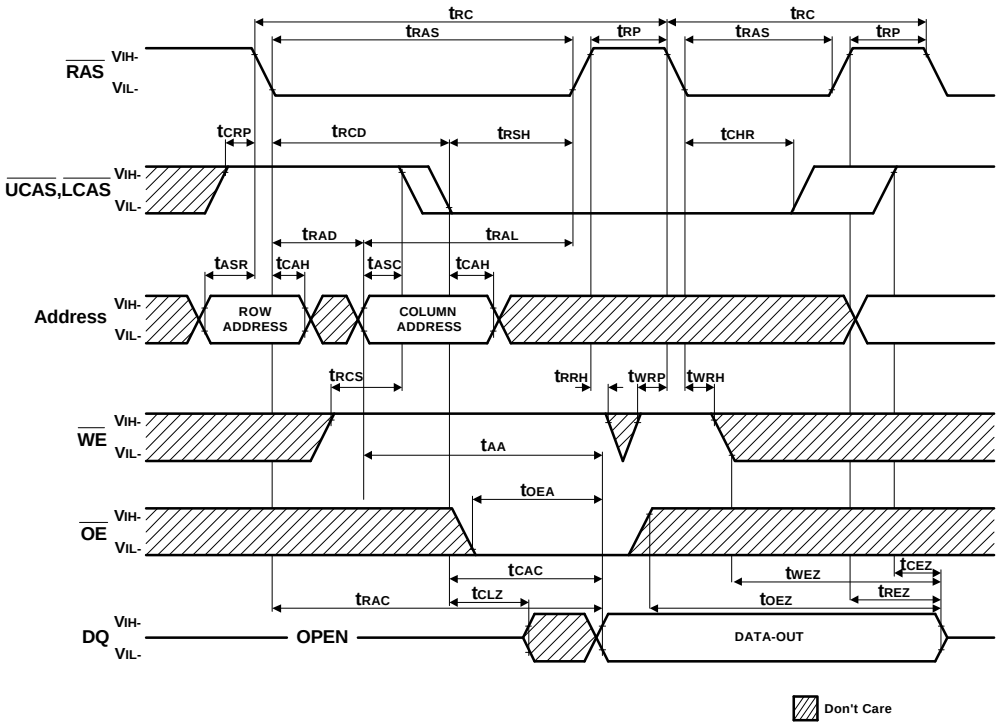
Remark Address, $\overline{\text{OE}}$: Don't care DQ : Hi - Z

$\overline{\text{RAS}}$-Only Refresh Cycle

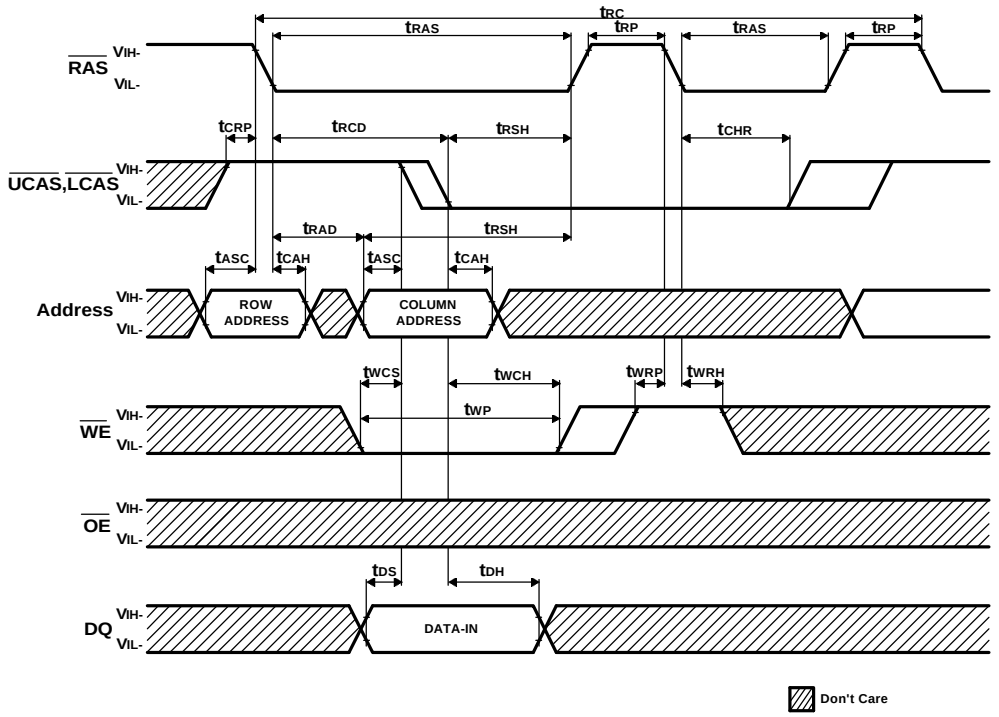


Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care DQ : Hi - Z

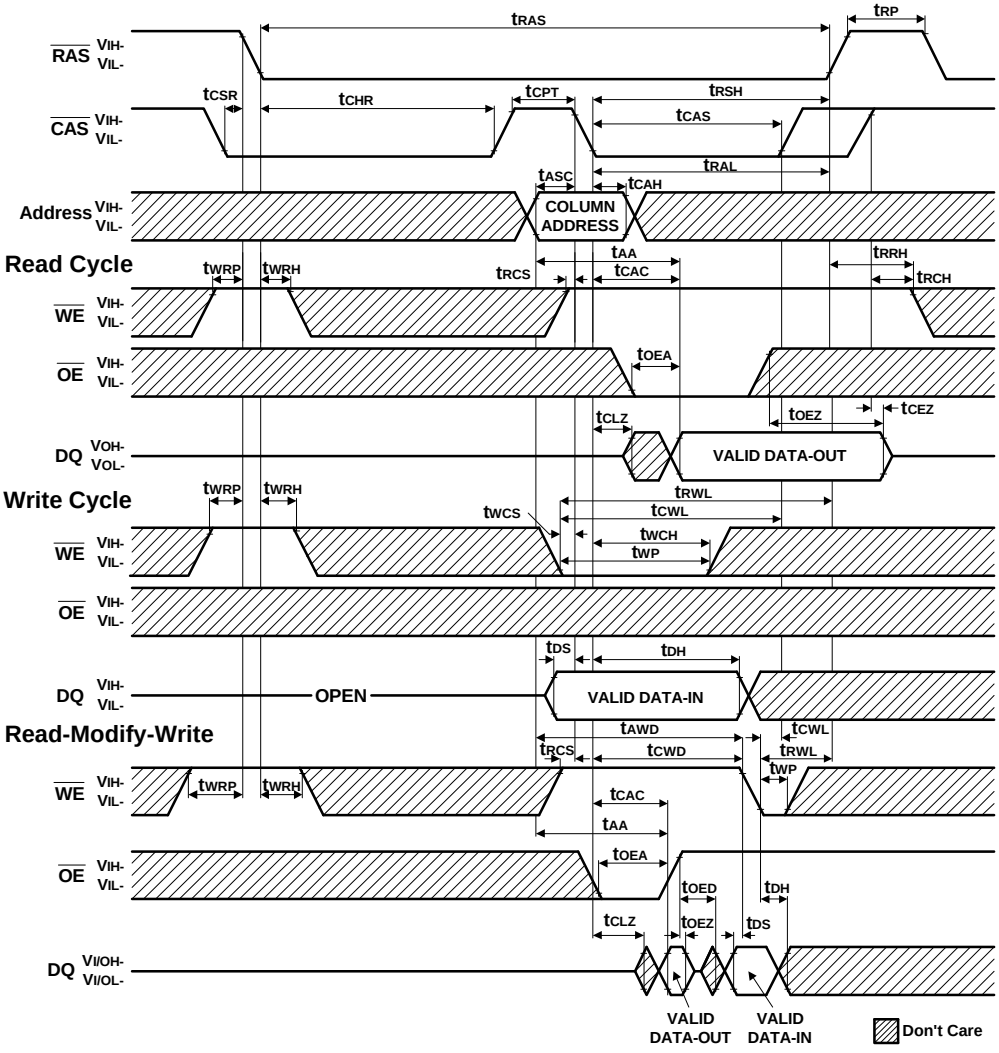
Hidden Refresh Cycle (Read)



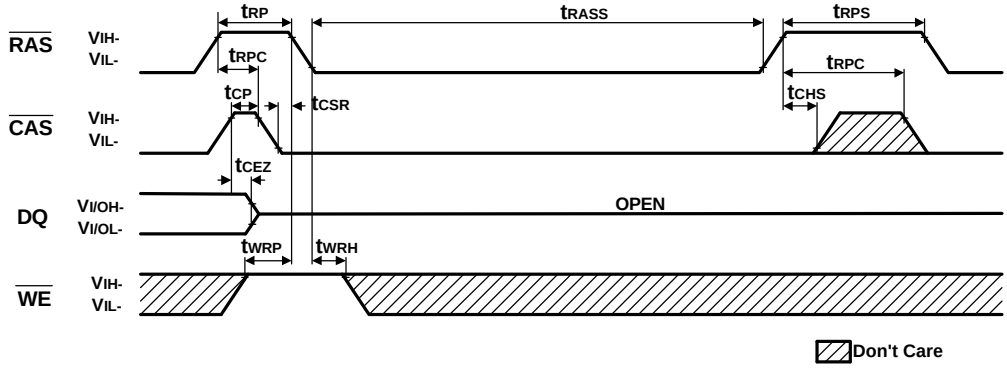
Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN



$\overline{CAS}$-Before $\overline{RAS}$ Refresh Counter Test Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Self Refresh Cycle

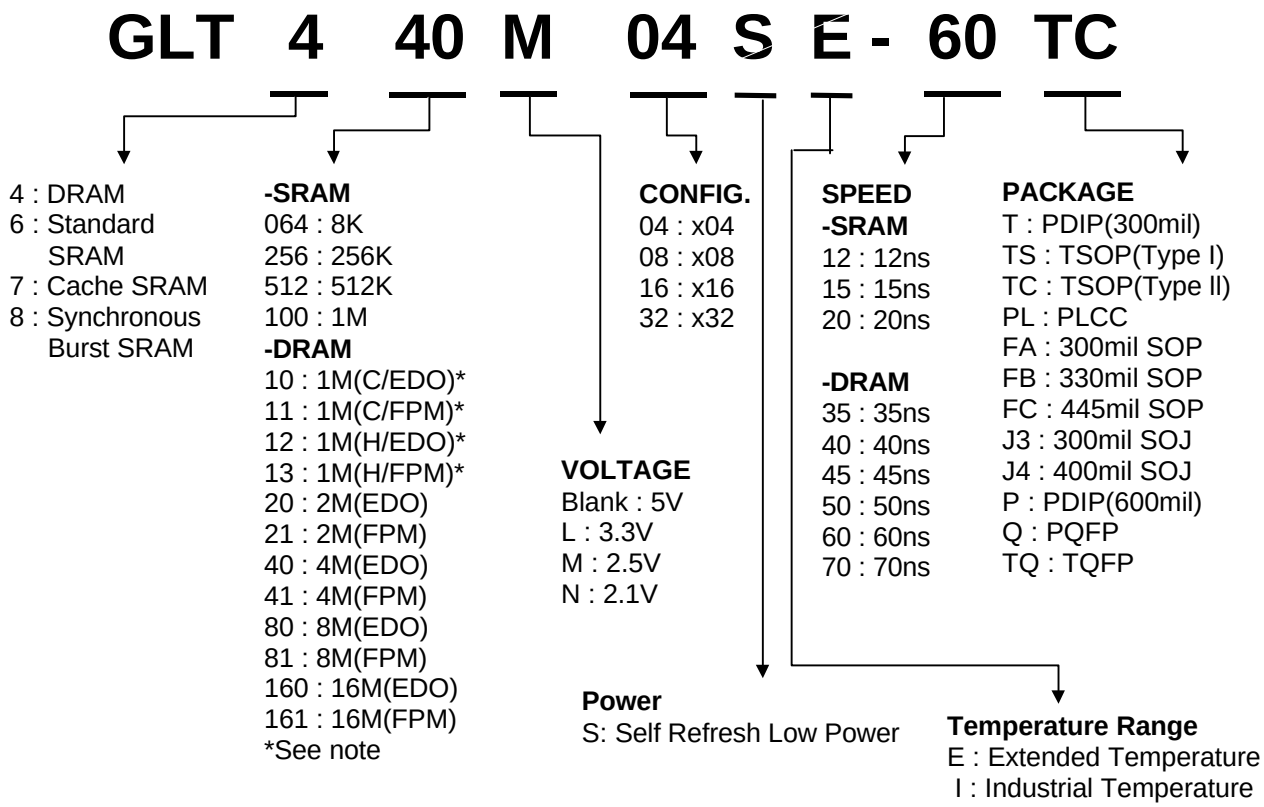


NOTE : $\overline{OE}$, Address = Don't Care

Ordering Information

Part Number	*SPEED*	*POWER*	*FEATURE*	*TEMPERATURE*	*PACKAGE*
GLT440M04-60TC	**60ns**	**Normal**	**EDO**	**Commercial**	**TSOPII 300mil 20/26L**
GLT440M04-70TC	**70ns**	**Normal**	**EDO**	**Commercial**	**TSOPII 300mil 20/26L**
GLT440M04E-60TC	**60ns**	**Normal**	**EDO**	**Extended**	**TSOPII 300mil 20/26L**
GLT440M04E-70TC	**70ns**	**Normal**	**EDO**	**Extended**	**TSOPII 300mil 20/26L**
GLT440M04S-60TC	**60ns**	**Self Refresh Low Power**	**EDO**	**Commercial**	**TSOPII 300mil 20/26L**
GLT440M04S-70TC	**70ns**	**Self Refresh Low Power**	**EDO**	**Commercial**	**TSOPII 300mil 20/26L**
GLT440M04SE-60TC	**60ns**	**Self Refresh Low Power**	**EDO**	**Extended**	**TSOPII 300mil 20/26L**
GLT440M04SE-70TC	**70ns**	**Self Refresh Low Power**	**EDO**	**Extended**	**TSOPII 300mil 20/26L**

Parts Numbers (Top Mark) Definition :



Note : C➞CDROM , H➞HDD.
Example :

1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

300mil 20/26 Lead Thin Small Outline Package (TSOP) TYPE II

Unit : Inch