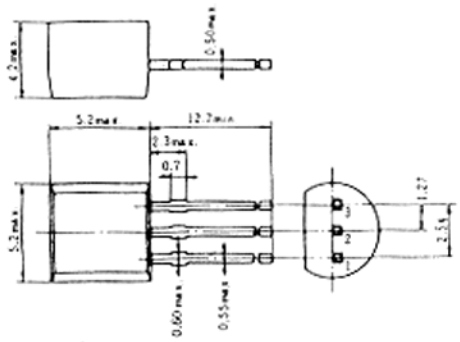
HITACHI

2SK187

SILICON N-CHANNEL JUNCTION FET

LOW FREQUENCY LOW NOISE AMPLIFIER



1. Drain
2. Gate
3. Source

(Dimensions in mm)

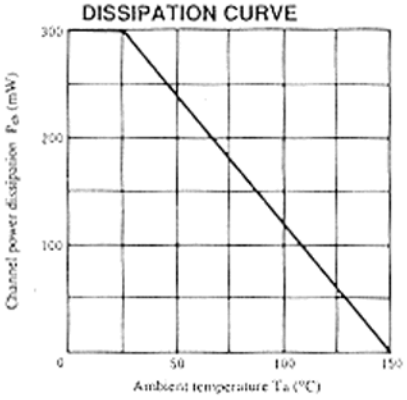
(JEDEC TO-92)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	2SK187	Unit
Gate to source voltage	V_{GSS}	–40	V
Drain to source voltage	V_{DSX}*	40	V
Drain current	I_D	30	mA
Gate current	I_G	10	mA
Channel power dissipation	P_{ch}	300	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

* Value at V_{GS} = –2V

MAXIMUM CHANNEL POWER DISSIPATION CURVE



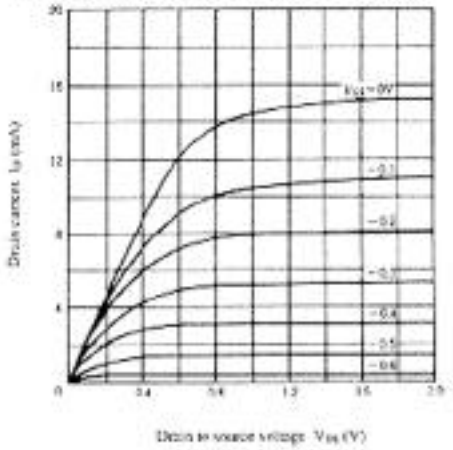
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to source breakdown voltage	$V_{(BR)GSS}$	I_G = –100μA, V_{DS} = 0	–40	—	—	V
Drain to source breakdown voltage	$V_{(BR)DSX}$	I_D = 100μA, V_{GS} = –2V	40	—	—	V
Gate cutoff current	I_{GSS}	V_{GS} = –30V, V_{DS} = 0	—	—	–10	nA
Drain current	I_{DSS}*	V_{DS} = 10V, V_{GS} = 0	2.5	—	20	mA
Gate to source cutoff voltage	$V_{GS(off)}$	V_{DS} = 10V, I_D = 10μA	–0.13	—	–1.5	V
Forward transfer admittance	$\lvert y_{fs} \rvert$	V_{DS} = 10V, I_D = 3mA, f = 1kHz	18	21	—	mS
Drain to source saturation voltage	$V_{DS(sat)}$	V_{GS} = 0V, I_D = 1mA	—	0.07	—	V
Input capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0, f = 1MHz	—	41	—	pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 10V, V_{GS} = 0, f = 1MHz	—	8.0	—	pF
Noise voltage referred to input	e_n	V_{DS} = 10V, I_D = 3mA, R_g = 0, f = 1kHz	—	1.0	—	nV/√Hz
Output noise voltage	V_N	See Test Circuit	—	—	8.5	mV

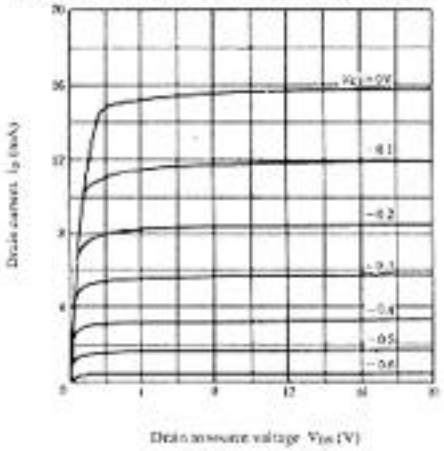
* The 2SK187 is grouped by I_{DSS} as follows.

C	D	E	F
2.5 to 5	4 to 8	6 to 12	10 to 20

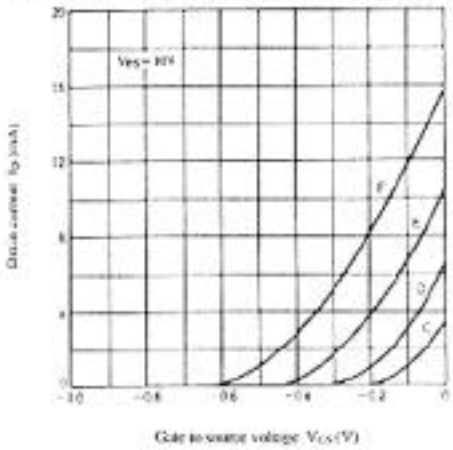
TYPICAL OUTPUT CHARACTERISTICS(1)



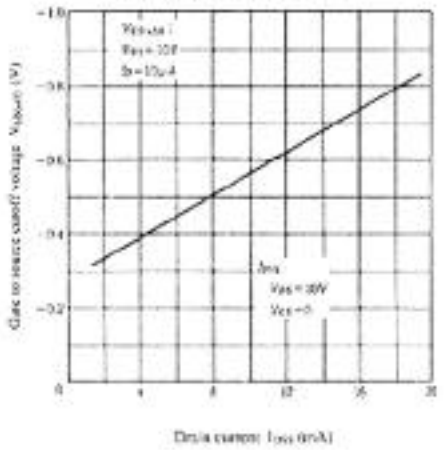
TYPICAL OUTPUT CHARACTERISTICS(2)



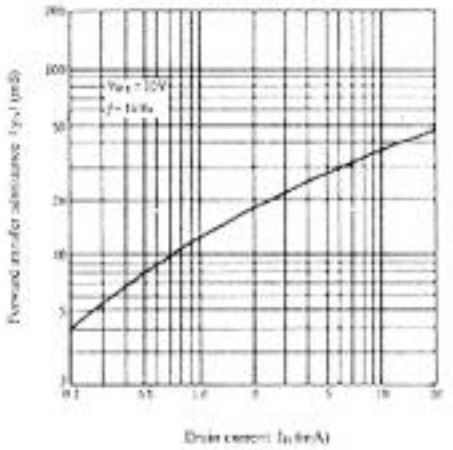
TYPICAL TRANSFER CHARACTERISTICS



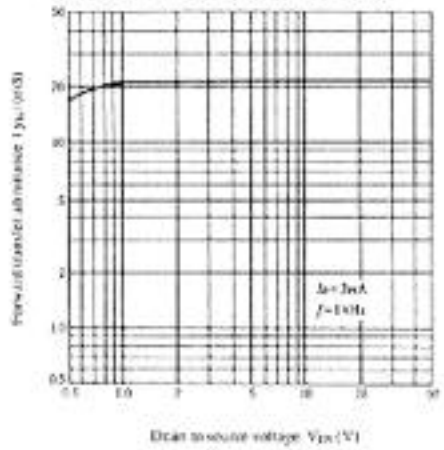
GATE TO SOURCE CUT-OFF VOLTAGE VS. DRAIN CURRENT



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT

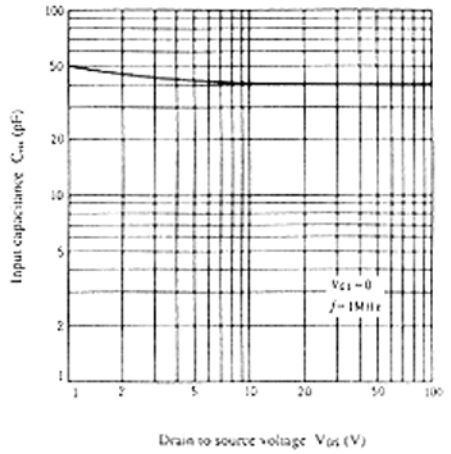


FORWARD TRANSFER ADMITTANCE VS. DRAIN TO SOURCE VOLTAGE

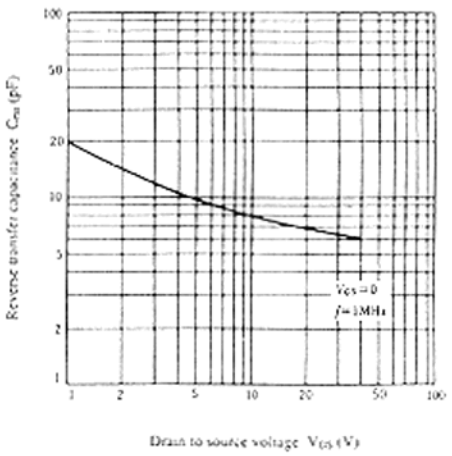


2SK187

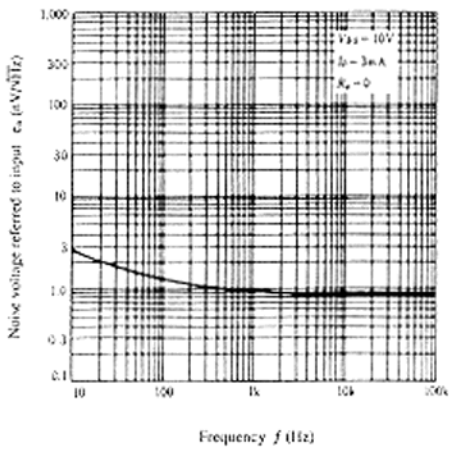
INPUT CAPACITANCE VS. DRAIN TO SOURCE VOLTAGE



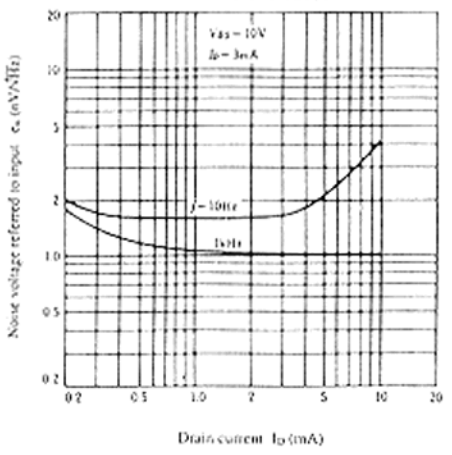
REVERSE TRANSFER CAPACITANCE VS. DRAIN TO SOURCE VOLTAGE



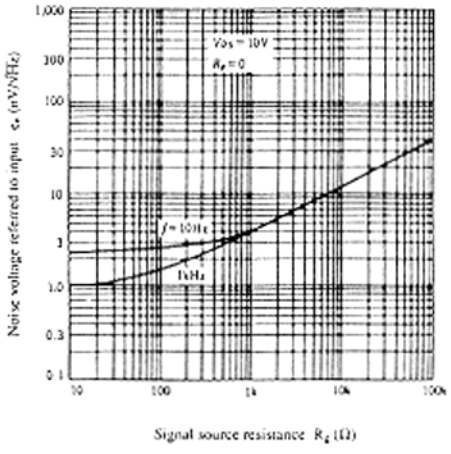
NOISE VOLTAGE REFERRED TO INPUT VS. FREQUENCY



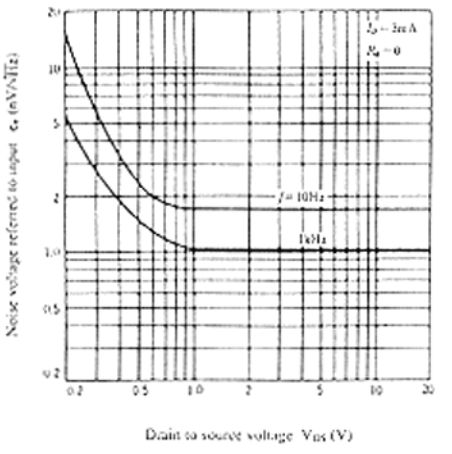
NOISE VOLTAGE REFERRED TO INPUT VS. DRAIN CURRENT



NOISE VOLTAGE REFERRED TO INPUT VS. SIGNAL SOURCE RESISTANCE



NOISE VOLTAGE REFERRED TO INPUT VS. DRAIN TO SOURCE VOLTAGE



V_N TEST CIRCUIT