

# 2SK2725

Silicon N Channel MOS FET  
High Speed Power Switching

# HITACHI

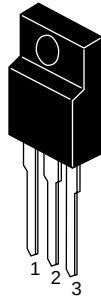
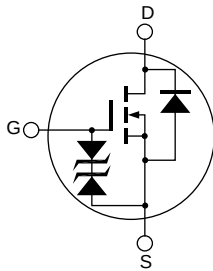
ADE-208-452 B  
3rd. Edition

## Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Avalanche ratings

## Outline

TO-220CFM



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings (Ta = 25°C)

| Item                                      | Symbol                   | Ratings     | Unit |
|-------------------------------------------|--------------------------|-------------|------|
| Drain to source voltage                   | V <sub>DSS</sub>         | 500         | V    |
| Gate to source voltage                    | V <sub>GSS</sub>         | ±30         | V    |
| Drain current                             | I <sub>D</sub>           | 5           | A    |
| Drain peak current                        | I <sub>D(pulse)</sub> *1 | 20          | A    |
| Body to drain diode reverse drain current | I <sub>DR</sub>          | 5           | A    |
| Avalanche current                         | I <sub>AP</sub> *3       | 5           | A    |
| Avalanche energy                          | E <sub>AR</sub> *3       | 1.38        | mJ   |
| Channel dissipation                       | Pch*2                    | 30          | W    |
| Channel temperature                       | Tch                      | 150         | °C   |
| Storage temperature                       | Tstg                     | −55 to +150 | °C   |

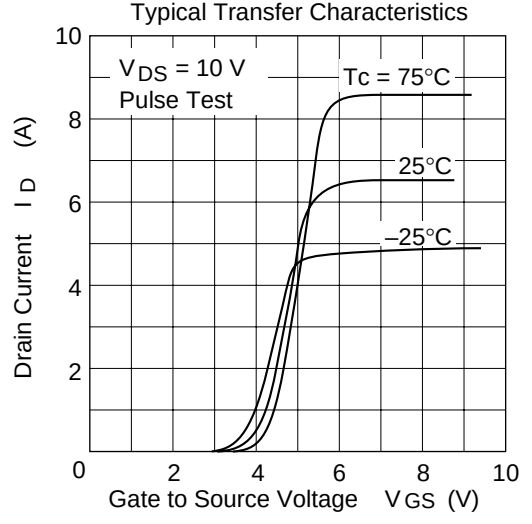
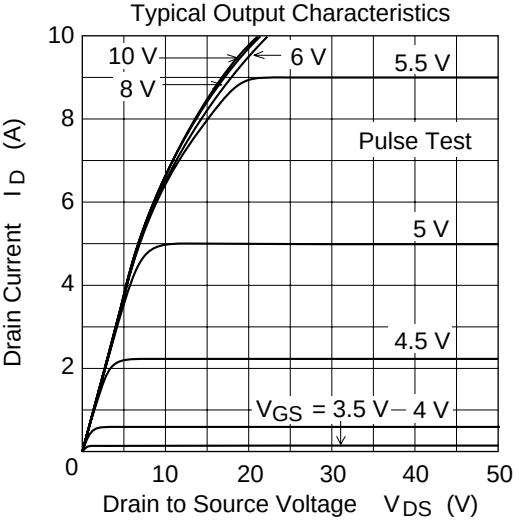
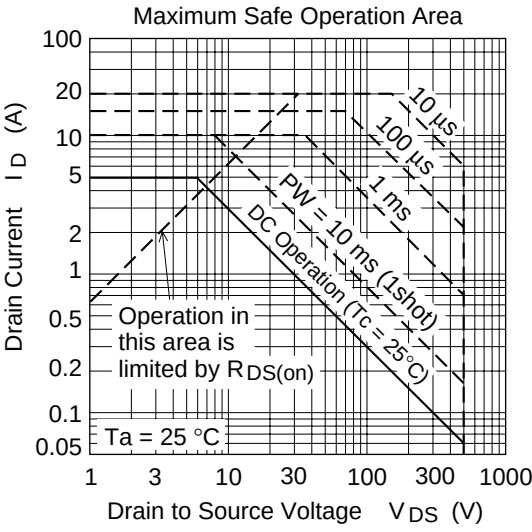
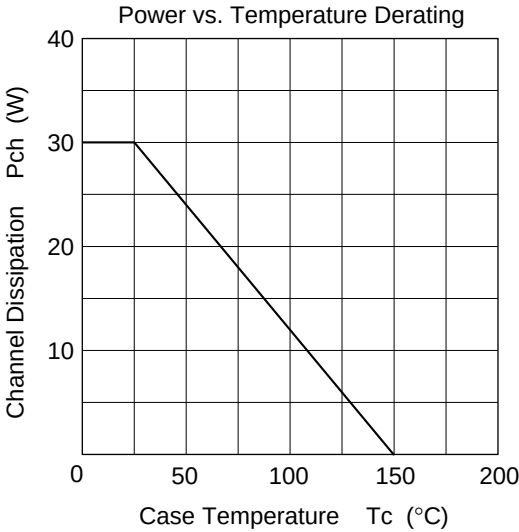
Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %  
2. Value at Tc = 25°C  
3. Value at Tch = 25°C, Rg ≥ 50Ω

**Electrical Characteristics** (Ta = 25°C)

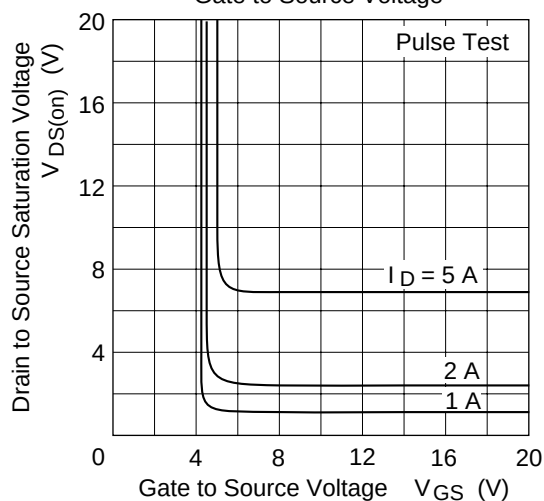
| Item                                       | Symbol        | Min | Typ  | Max | Unit | Test Conditions                                                         |
|--------------------------------------------|---------------|-----|------|-----|------|-------------------------------------------------------------------------|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 500 | —    | —   | V    | $I_D = 10\text{mA}$ , $V_{GS} = 0$                                      |
| Gate to source breakdown voltage           | $V_{(BR)GSS}$ | ±30 | —    | —   | V    | $I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$                               |
| Gate to source leak current                | $I_{GSS}$     | —   | —    | ±10 | μA   | $V_{GS} = \pm 25\text{V}$ , $V_{DS} = 0$                                |
| Zero gate voltage drain current            | $I_{DSS}$     | —   | —    | 10  | μA   | $V_{DS} = 500\text{V}$ , $V_{GS} = 0$                                   |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 2.5 | —    | 3.5 | V    | $I_D = 1\text{mA}$ , $V_{DS} = 10\text{V}^{*1}$                         |
| Static drain to source on state resistance | $R_{DS(on)}$  | —   | 1.2  | 1.6 | Ω    | $I_D = 3\text{A}$ , $V_{GS} = 10\text{V}^{*1}$                          |
| Forward transfer admittance                | $ y_{fs} $    | 2.5 | 4.5  | —   | S    | $I_D = 3\text{A}$ , $V_{DS} = 10\text{V}^{*1}$                          |
| Input capacitance                          | $C_{iss}$     | —   | 630  | —   | pF   | $V_{DS} = 10\text{V}$                                                   |
| Output capacitance                         | $C_{oss}$     | —   | 250  | —   | pF   | $V_{GS} = 0$                                                            |
| Reverse transfer capacitance               | $C_{rss}$     | —   | 55   | —   | pF   | $f = 1\text{MHz}$                                                       |
| Total gate charge                          | $Q_g$         | —   | 13.5 | —   | nc   | $V_{DD} = 400\text{V}$                                                  |
| Gate to source charge                      | $Q_{gs}$      | —   | 3.5  | —   | nc   | $V_{GS} = 10\text{V}$                                                   |
| Gate to drain charge                       | $Q_{gd}$      | —   | 5.0  | —   | nc   | $I_D = 5\text{A}$                                                       |
| Turn-on delay time                         | $t_{d(on)}$   | —   | 11   | —   | ns   | $V_{GS} = 10\text{V}$ , $I_D = 3\text{A}$                               |
| Rise time                                  | $t_r$         | —   | 45   | —   | ns   | $R_L = 10\Omega$                                                        |
| Turn-off delay time                        | $t_{d(off)}$  | —   | 40   | —   | ns   |                                                                         |
| Fall time                                  | $t_f$         | —   | 50   | —   | ns   |                                                                         |
| Body to drain diode forward voltage        | $V_{DF}$      | —   | 0.95 | —   | V    | $I_D = 5\text{A}$ , $V_{GS} = 0$                                        |
| Body to drain diode reverse recovery time  | $t_{rr}$      | —   | 200  | —   | ns   | $I_F = 5\text{A}$ , $V_{GS} = 0$<br>$di_F/dt = 100\text{A}/\mu\text{s}$ |

Note: 1. Pulse test

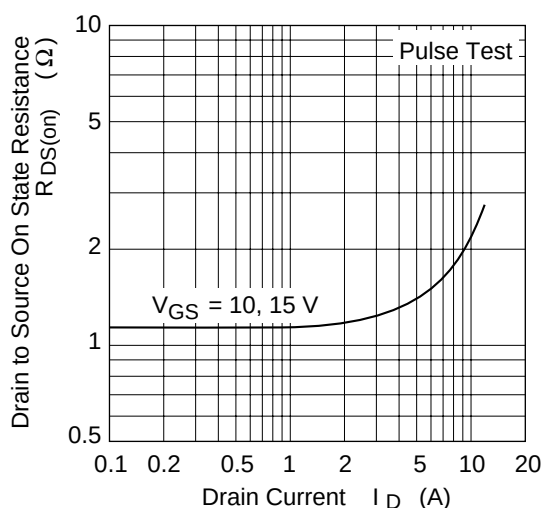
Main Characteristics



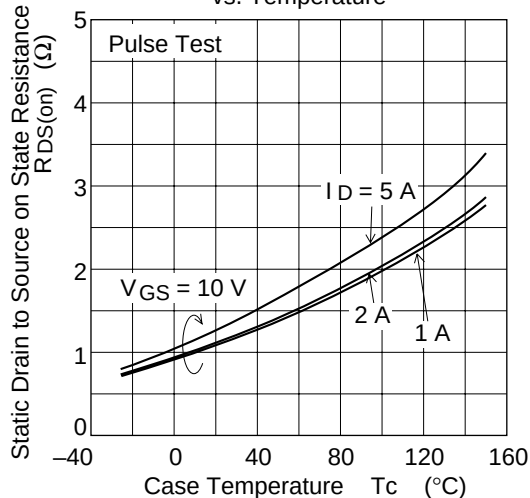
Drain to Source Saturation Voltage vs.  
Gate to Source Voltage



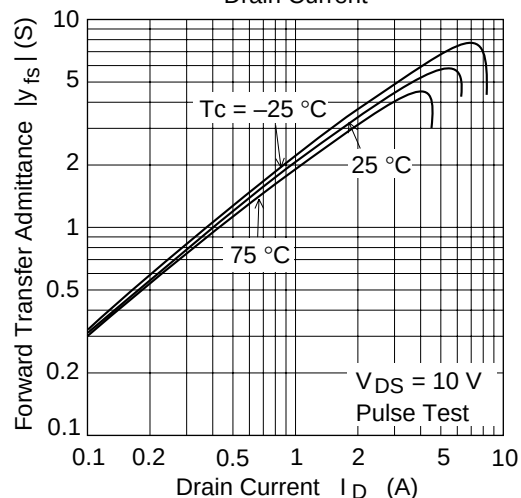
Static Drain to Source on State Resistance  
vs. Drain Current



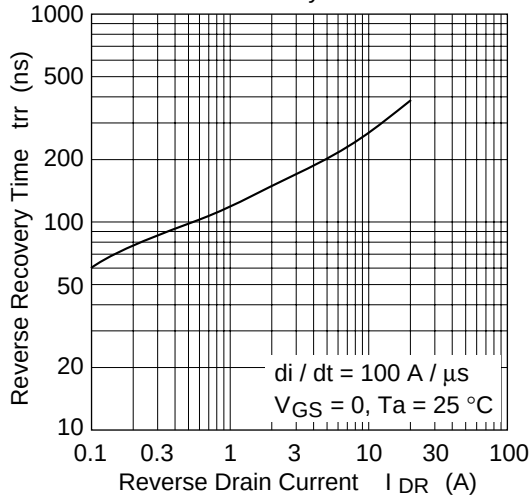
Static Drain to Source on State Resistance  
vs. Temperature



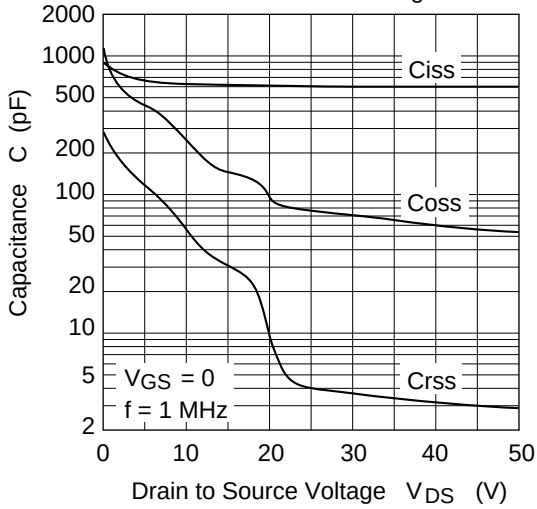
Forward Transfer Admittance vs.  
Drain Current



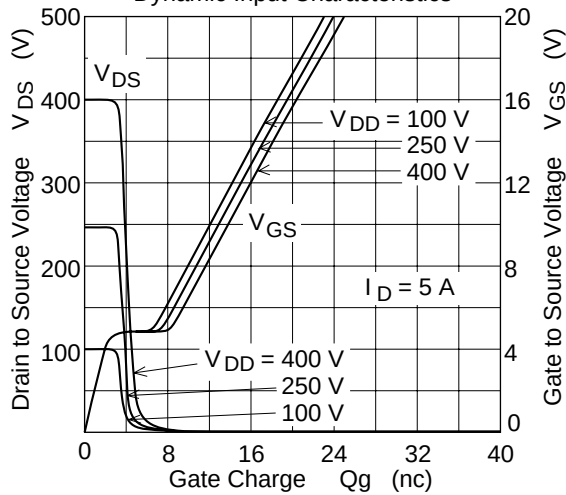
Body to Drain Diode Reverse Recovery Time



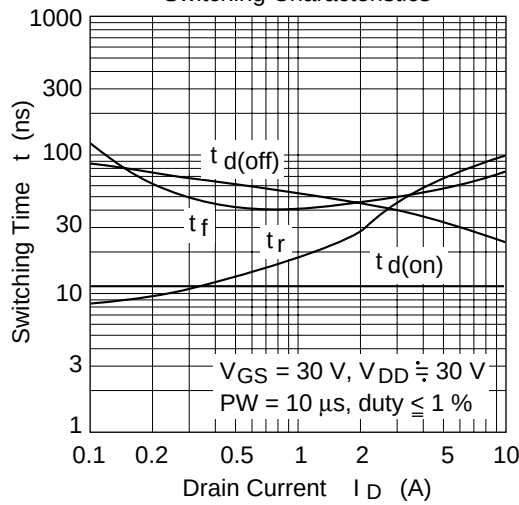
Typical Capacitance vs. Drain to Source Voltage

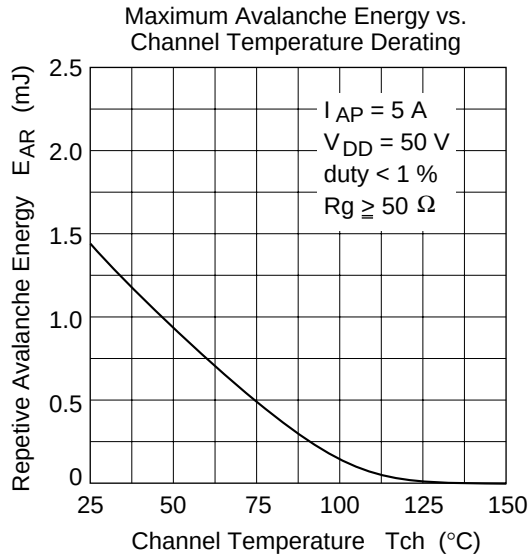
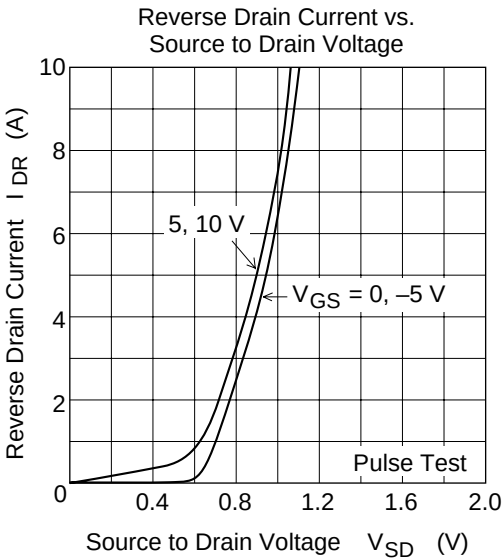


Dynamic Input Characteristics

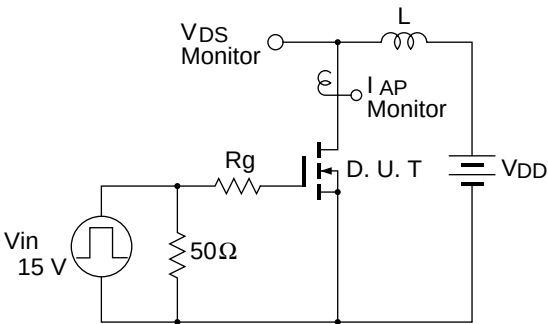


Switching Characteristics

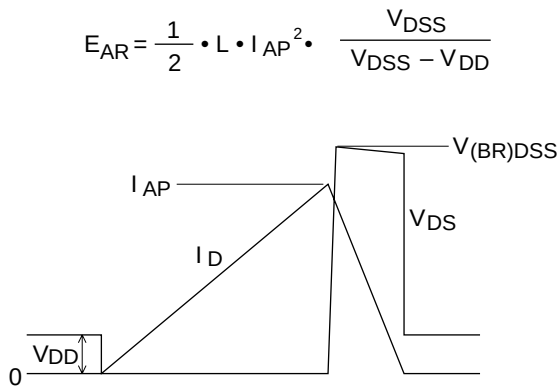


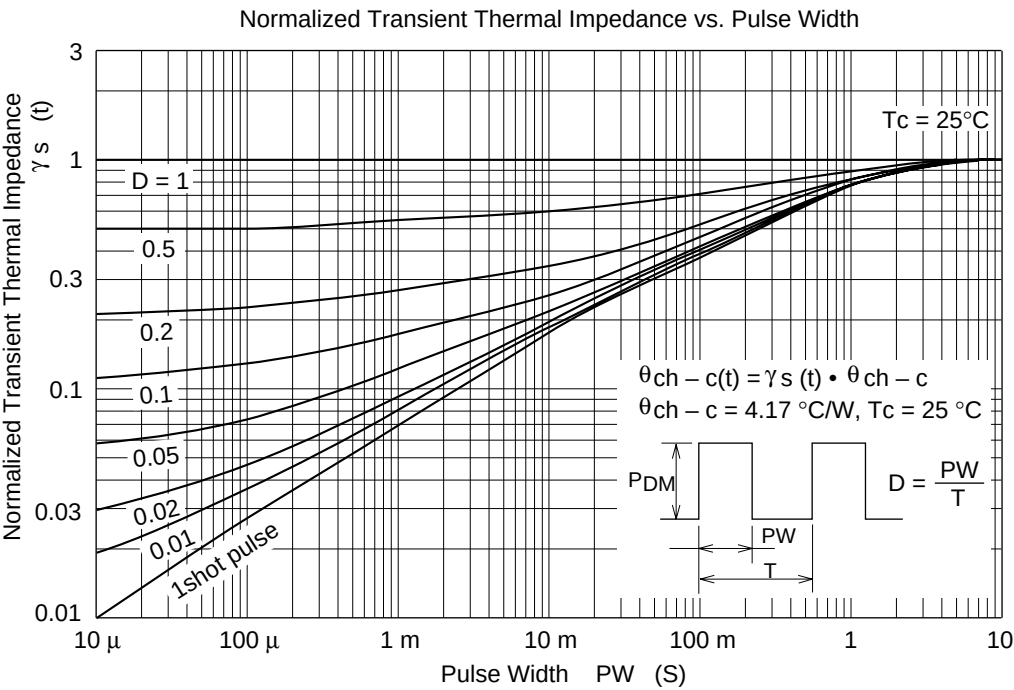


Avalanche Test Circuit

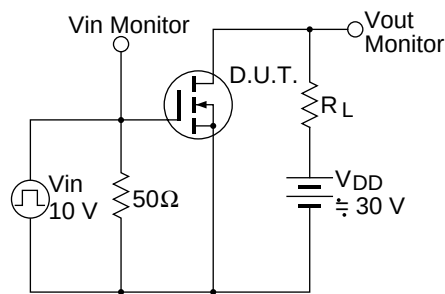


Avalanche Waveform

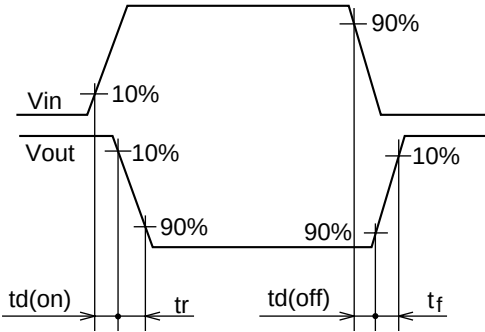




Switching Time Test Circuit



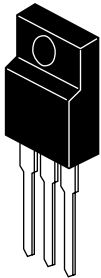
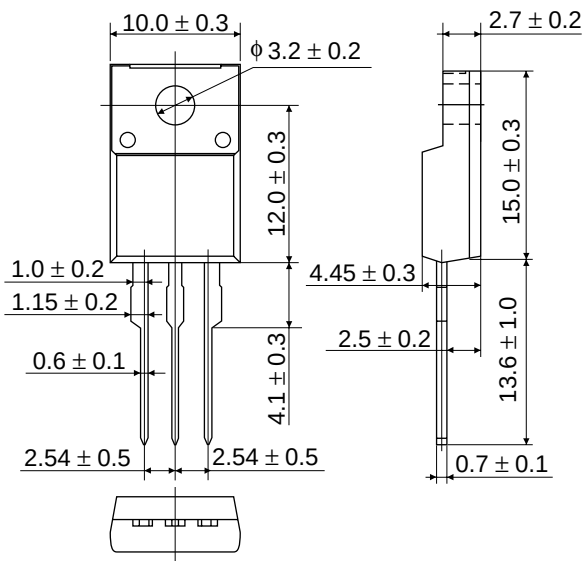
Switching Time Waveforms





Package Dimensions

Unit: mm



| Hitachi Code | TO-220CFM |
|--------------|-----------|
| EIAJ         | —         |
| JEDEC        | —         |

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