HD404054 Series/HD404094 Series

HITACHI

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Description

The HD404054 Series and HD404094 Series are HMCS400-series microcomputers designed to increase program productivity with large-capacity memory. Each microcomputer has three timers, one serial interface, comparator, input capture circuit.

The HD404054 Series includes three chips: the HD404052 with 2-kword ROM; the HD404054 with 4-kword ROM; and the HD4074054 with 4-kword PROM (ZTAT™ version). Also, the HD404094 Series includes three chips: the HD404092 with 2-kword ROM; the HD404094 with 4-kword ROM; and the HD4074094 with 4-kword PROM (ZTAT™ version).

The HD4074054 and HD4074094 are PROM version (ZTAT™ microcomputers). Program can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The ZTAT™version is 27256-compatible.)

Features

- The differences between HD404054 Series and HD404094 Series

	HD404054 Series	HD404094 Series
I/O pins	10 large-current output pins: Six 15-mA sinks and four 10-mA sources	• 6 largecurrent output pins: Two 15-mA sinks and four 10-mA sources • 4 intermediate voltage output pins

- 27 I/O pins and 8 dedicated input pins
- Three timer/counters
- Eight-bit input capture circuit
- Two timer outputs (including two PWM outputs)
- One event counter inputs (including one double-edge function)
- One clock-synchronous 8-bit serial interface
- Comparator (2 channels)
- Built-in oscillators
  — Main clock: Ceramic or crystal oscillator (an external clock is also possible)

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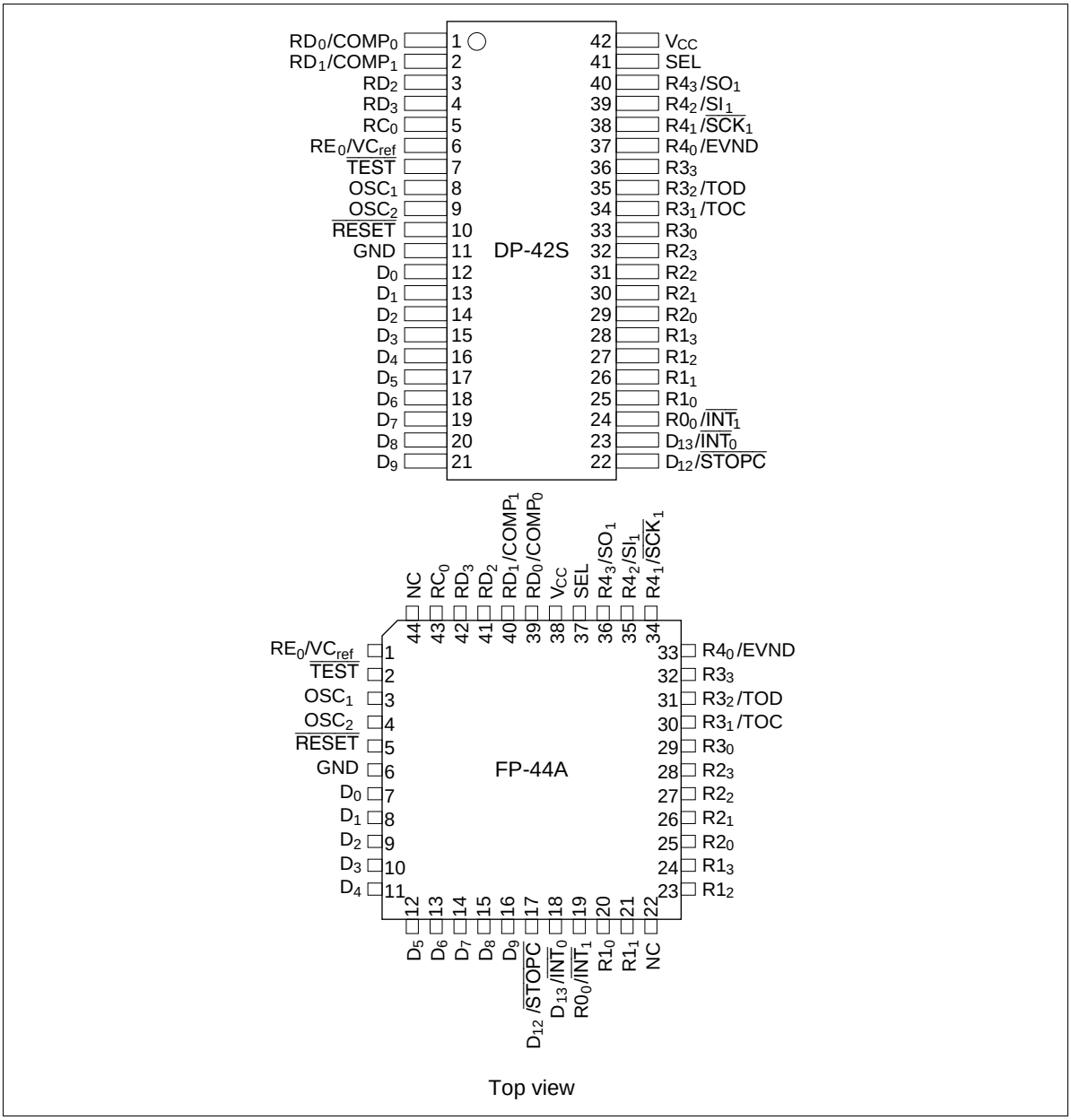
- Six interrupt sources
  - — Two by external sources
  - — Four by internal sources
- Subroutine stack up to 16 levels, including interrupts
- Two low-power dissipation modes
  - — Standby mode
  - — Stop mode
- One external input for transition from stop mode to active mode
- Instruction cycle time: 1 µs (f_{OSC} = 4 MHz at 1/4 division ratio)
  - — 1/4, or 1/32 division ratio can be selected by hardware
- Two operating modes
  - — MCU mode
  - — MCU/PROM mode (HD4074054, HD4074094)

Ordering Information

	Product Name				
Type	**HD404054 Series**	**HD404094 Series**	**ROM (words)**	**RAM (digit)**	**Package**
Mask ROM	HD404052H	HD404092H	2,048	512	FP-44A
	HD404052S	HD404092S			DP-42S
	HD40A4052H				FP-44A
	HD40A4052S				DP-42S
	HD404054H	HD404094H	4,096		FP-44A
	HD404054S	HD404094S			DP-42S
	HD40A4054H				FP-44A
	HD40A4054S				DP-42S
ZTAT™	HD4074054H	HD4074094H	4,096		FP-44A
	HD4074054S	HD4074094S			DP-42S

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi, Ltd.

Pin Arrangement

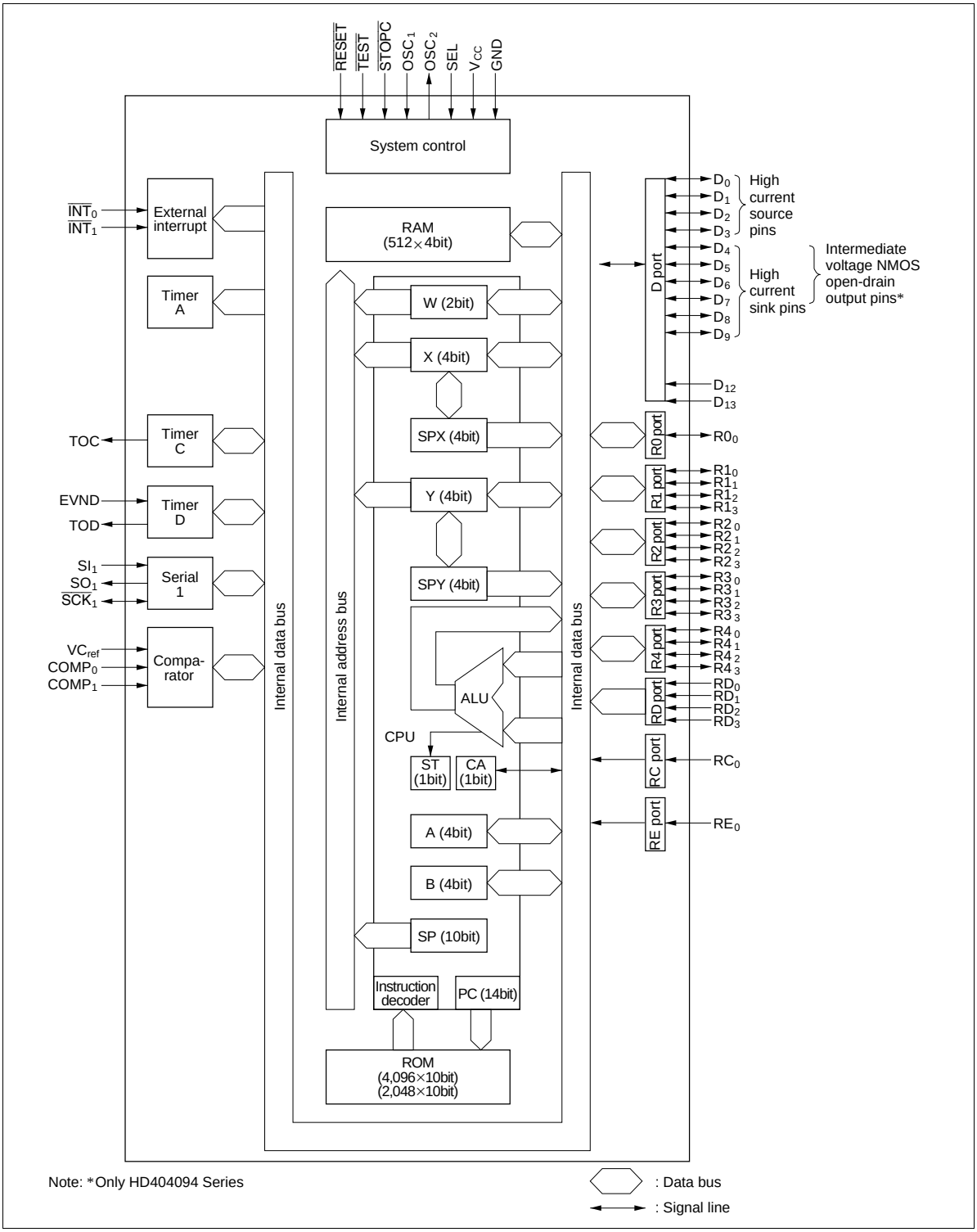


Pin Description

Item	Symbol	Pin Number DP-42S	Pin Number FP-44A	I/O	Function
Power supply	V_{CC}	42	38		Applies power voltage
	GND	11	6		Connected to ground
Test	$\overline{TEST}$	7	2	I	Used for factory testing only: Connect this pin to V_{CC}
Reset	$\overline{RESET}$	10	5	I	Resets the MCU
Oscillator	OSC_1	8	3	I	
	OSC_2	9	4	O	
Port	D_0–D_9	12–21	7–16	I/O*	Input/output pins addressed by individual bits; pins D_0–D_3 are high-current source pins that can each supply up to 10 mA. The HD404054 Series: pins D_4–$D_9$are high-current sink pins that can each supply up to 15mA. The HD404094 Series: D_4–D_7 are intermediate voltage (12 V) NMOS open-drain pins, and D_8, D_9 are high-current sink pins that can each supply up to 15 mA.
	D_{12},D_{13}	22, 23	17, 18	I	Input pins addressable by individual bits
	$R0_0$–$R4_3$	24–40	19–36	I/O	Input/output pins addressable in 4-bit units
	RD_0–RD_3, RC_0, RE_0	1–6	39–43,1	I	Input pins addressable in 4-bit units
Interrupt	$\overline{INT}_0$, $\overline{INT}_1$	23, 24	18, 19	I	Input pins for external interrupts
Stop clear	$\overline{STOPC}$	22	17	I	Input pin for transition from stop mode to active mode
Serial	$\overline{SCK}_1$	38	34	I/O	Serial clock input/output pin
	SI_1	39	35	I	Serial receive data input pin
	SO_1	40	36	O	Serial transmit data output pin
Timer	TOC, TOD	34, 35	30, 31	O	Timer output pins
	EVND	37	33	I	Event count input pins
Comparator	$COMP_0$, $COMP_1$	1, 2	39, 40	I	Analog input pins for voltage comparator
	VC_{ref}	6	1		Reference voltage pin for inputting the threshold voltage of the analog input pin.
Division rate	SEL	41	37	I	Input pin for selecting system clock division rate after $\overline{RESET}$ input or after stop mode cancellation. 1/4 division rate: Connect it to V_{CC} 1/32 division rate: Connect it to GND

Note: * D_4–D_7 of the HD404094 Series are output pins.

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$07FF (HD404052, HD40A4052, HD404092), $0000–$0FFF (HD404054, HD40A4054, HD4074054, HD404094, HD4074094)): Used for program coding.

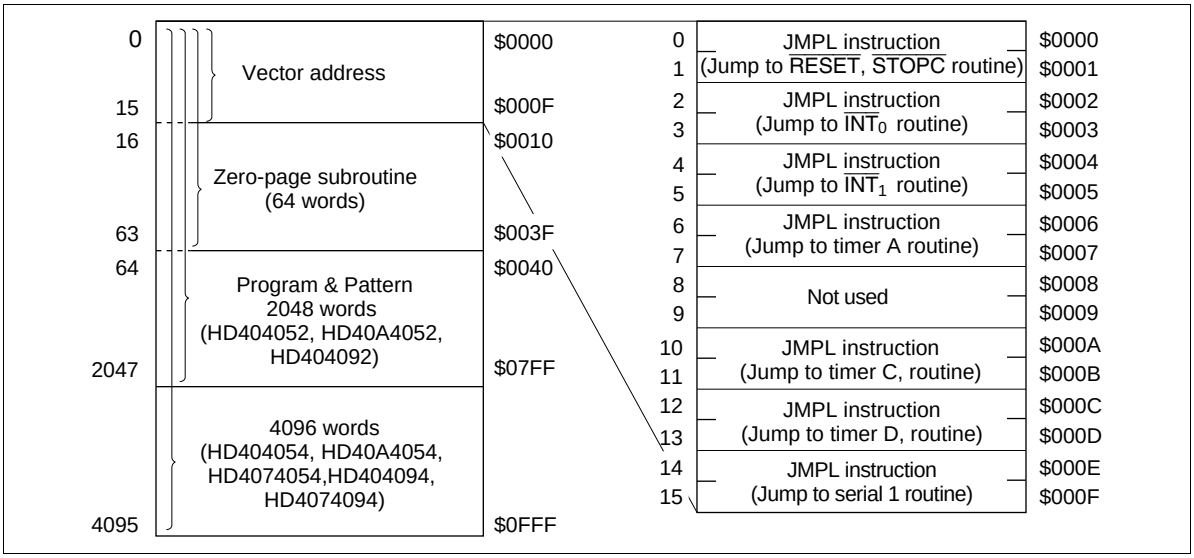


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 512-digit × 4-bit RAM area consisting of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special register area, and register flag area are mapped onto the same RAM memory space as a RAM-mapped register area outside the above areas. The RAM memory map is shown in figure 2 and described as follows.

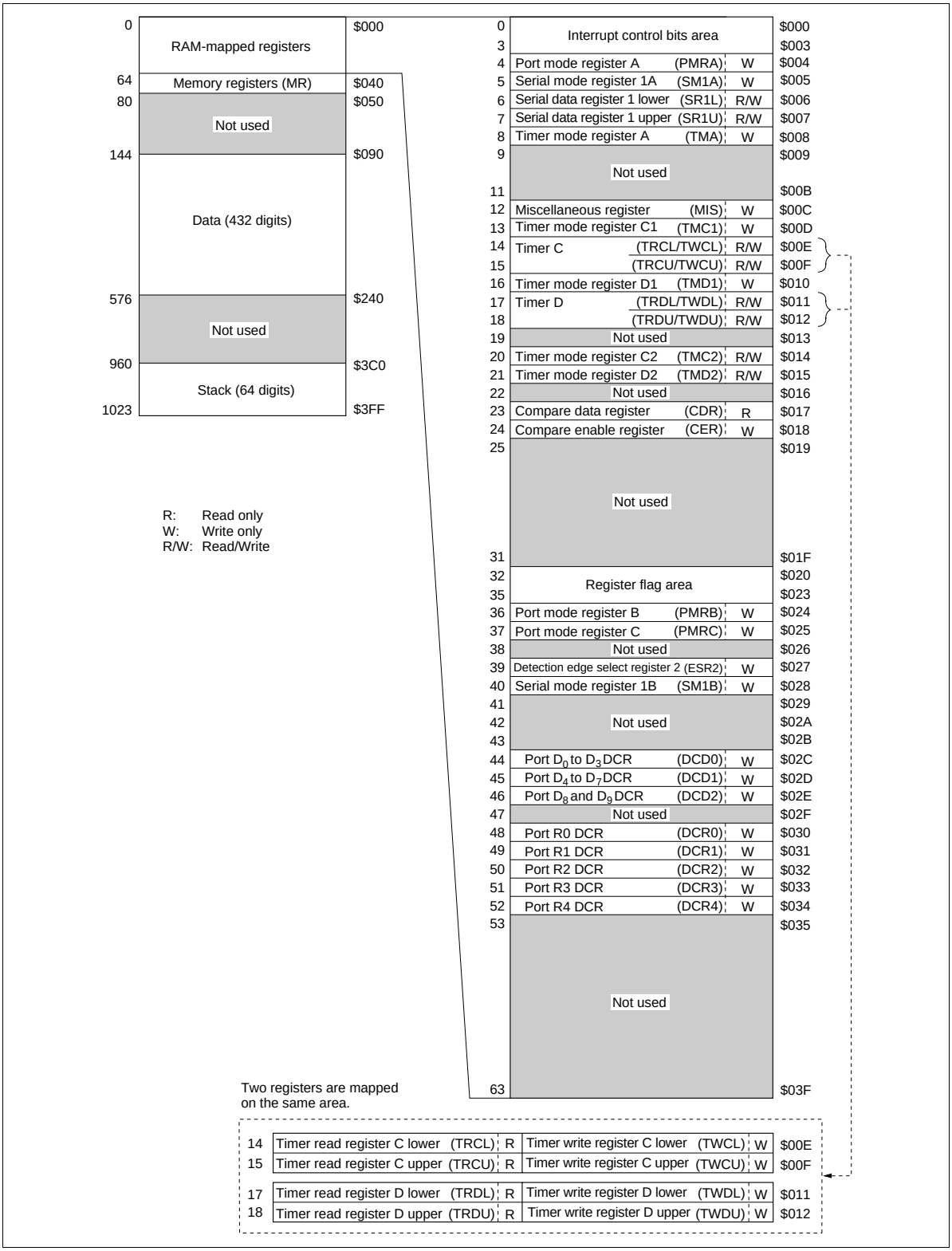


Figure 2 RAM Memory Map

RAM-Mapped Register Area ($000–$03F):

- Interrupt Control Bits Area ($000–$003)

  This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- Special Function Register Area ($004–$018, $024–$034)

  This area is used as mode registers and data registers for external interrupts, serial interface 1, timer/counters, voltage comparator, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- Register Flag Area ($020–$023)

  This area is used for the WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

Memory Register (MR) Area ($040–$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

Data Area ($090–$23F): 432 digits from $090 to $23F.

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

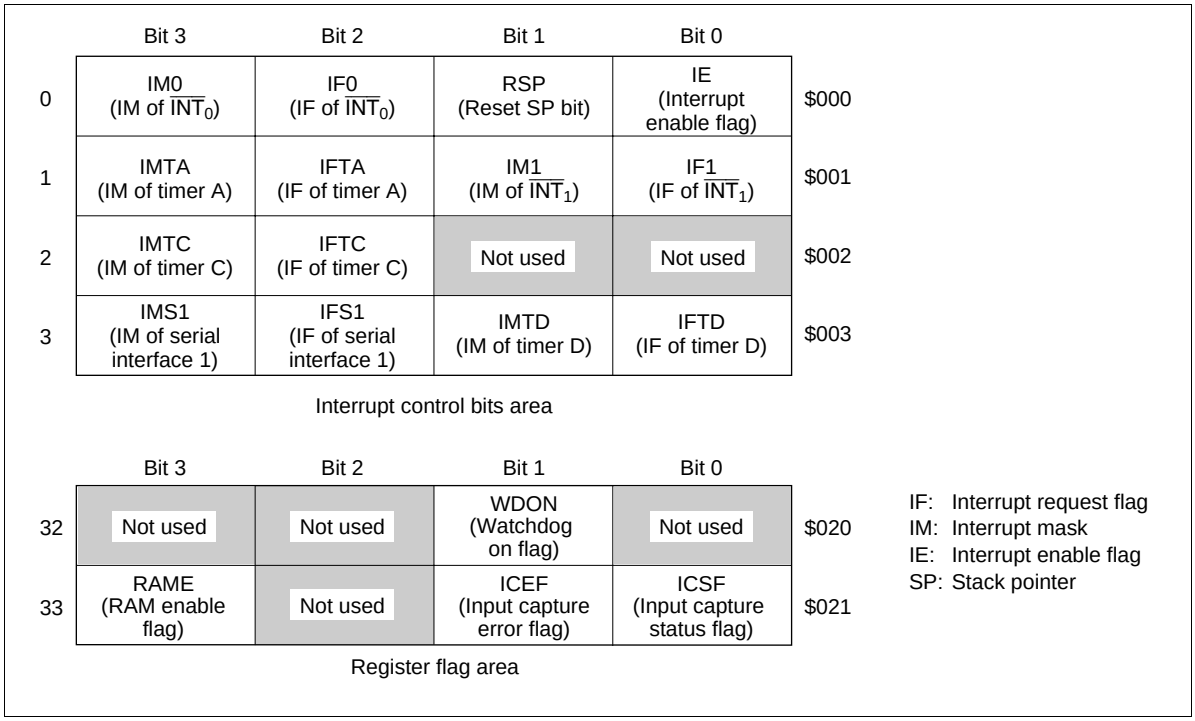


Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by $\overline{STOPC}$ enable for stop mode cancellation.
If the TM or TDM instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

	Bit 3	Bit 2	Bit 1	Bit 0
$000 $003	Interrupt control bits area			
PMRA $004			$R4_2/SI_1$	$R4_3/SO_1$
SM1A $005	$R4_1/\overline{SCK}_1$	Serial transmit clock speed selection 1		
SR1L $006	Serial data register 1 (lower digit)			
SR1U $007	Serial data register 1 (upper digit)			
TMA $008		Clock source selection (timer A)		
MIS $00C	*2	SO_1 PMOS control		
TMC1 $00D	*1	Clock source selection (timer C)		
TRCL/TWCL $00E	Timer C register (lower digit)			
TRCU/TWCU $00F	Timer C register (upper digit)			
TMD1 $010	*1	Clock source selection (timer D)		
TRDL/TWDL $011	Timer D register (lower digit)			
TRDU/TWDU $012	Timer D register (upper digit)			
$013				
TMC2 $014		Timer-C output mode selection		
TMD2 $015	*3	Timer-D output mode selection		
$016				
CDR $017	Result of each analog input comparison			
CER $018	*4		*5	
$020 $023	Register flag area			
PMRB $024				$R0_0/\overline{INT}_1$
PMRC $025	$D_{13}/\overline{INT}_0$	$D_{12}/\overline{STOPC}$	$R4_0$/EVND	
$026				
ESR2 $027	EVND detection edge selection			
SM1B $028			*6	*7
DCD0 $02C	Port D_3 DCR	Port D_2 DCR	Port D_1 DCR	Port D_0 DCR
DCD1 $02D	Port D_7 DCR	Port D_6 DCR	Port D_5 DCR	Port D_4 DCR
DCD2 $02E			Port D_9 DCR	Port D_8 DCR
DCR0 $030				Port $R0_0$ DCR
DCR1 $031	Port $R1_3$ DCR	Port $R1_2$ DCR	Port $R1_1$ DCR	Port $R1_0$ DCR
DCR2 $032	Port $R2_3$ DCR	Port $R2_2$ DCR	Port $R2_1$ DCR	Port $R2_0$ DCR
DCR3 $033	Port $R3_3$ DCR	Port $R3_2$ DCR	Port $R3_1$ DCR	Port $R3_0$ DCR
DCR4 $034	Port $R4_3$ DCR	Port $R4_2$ DCR	Port $R4_1$ DCR	Port $R4_0$ DCR
$03F				

: Not used

Notes:
1. Auto-reload on/off
2. Pull-up MOS control
3. Input capture selection
4. Comparator switch
5. Port/comparator selection
6. SO_1 output level control in idle states
7. Serial clock source selection 1

Figure 5 Special Function Register Area

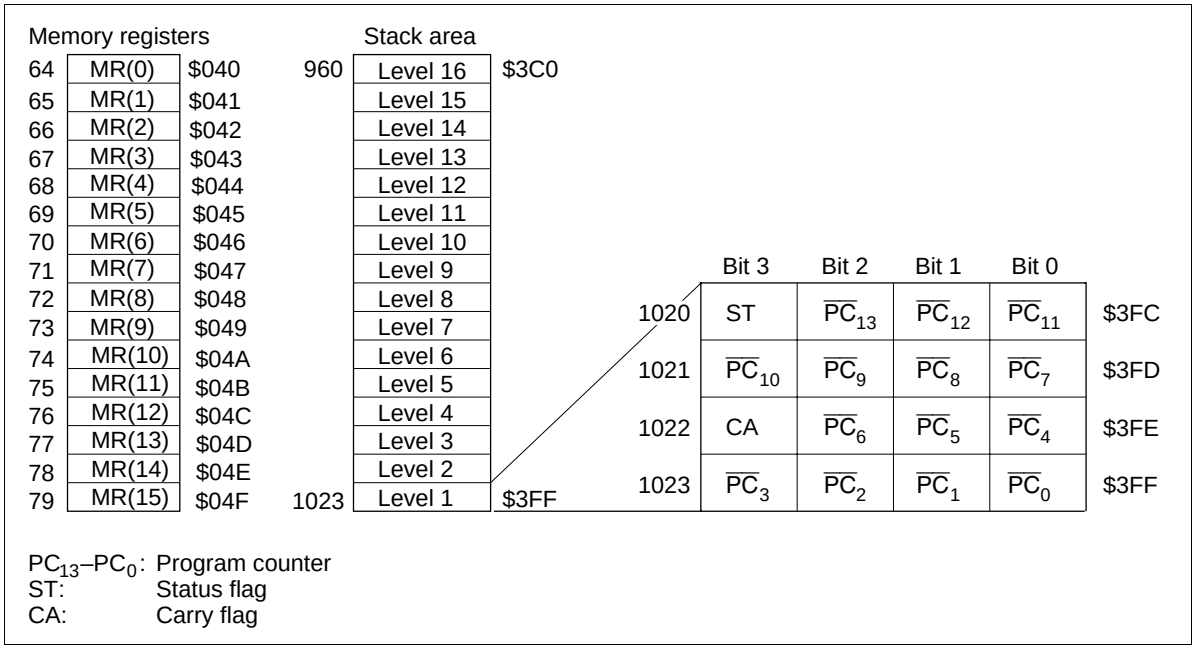


Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 7 and described below.

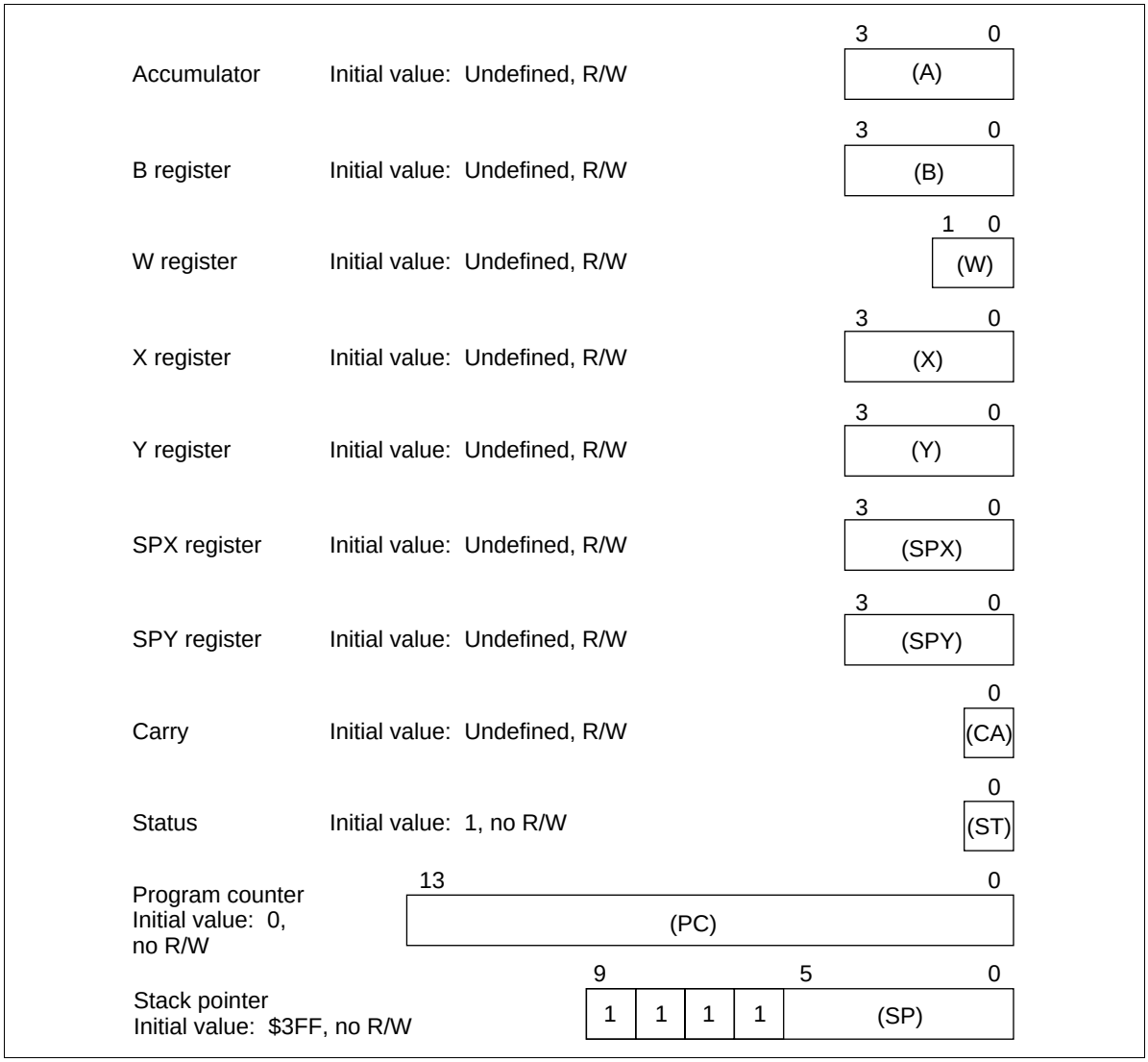


Figure 7 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold the results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction-but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): 14-bit binary counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is popped from the stack. The top four bits of the SP are fixed at 1111, so a stack can be used up to 16 levels.

The SP can be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the $\overline{\text{RESET}}$ pin. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ must be high for at least one t_{RC} to enable the oscillator to stabilize. During operation, $\overline{\text{RESET}}$ must be high for at least two instruction cycles.

Initial values after MCU reset are listed in table 1.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0 – DCD2)	All bits 0	Turns output buffer off (to high impedance)
		(DCR0– DCR4)	All bits 0	
	Port mode register A	(PMRA)	- - 00	Refer to description of port mode register A
	Port mode register B	(PMRB)	- - - 0	Refer to description of port mode register B
	Port mode register C bits 3, 2, 1	(PMRC3, PMRC2, PMRC1)	000 -	Refer to description of port mode register C
	Detection edge select register 2	(ESR2)	00 - -	Disables edge detection
Timer/ counters, serial interface	Timer mode register A	(TMA)	- 000	Refer to description of timer mode register A
	Timer mode register C1	(TMC1)	0000	Refer to description of timer mode register C1
	Timer mode register C2	(TMC2)	- 000	Refer to description of timer mode register C2
	Timer mode register D1	(TMD1)	0000	Refer to description of timer mode register D1
	Timer mode register D2	(TMD2)	0000	Refer to description of timer mode register D2
	Serial mode register 1A	(SM1A)	0000	Refer to description of serial mode register 1A
	Serial mode register 1B	(SM1B)	- - X0	Refer to description of serial mode register 1B
	Prescaler S	(PSS)	$000	—
	Timer counter A	(TCA)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer counter D	(TCD)	$00	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Timer write register D	(TWDU,	$X0	—
	Octal counter	TWDL)	000	—
Comparator	Compare enable register	(CER)	0 - 00	Refer to description of voltage comparator

Item		Abbr.	Initial Value	Contents
Bit register	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Input capture status flag	(ICSF)	0	Refer to description of timer D
	Input capture error flag	(ICEF)	0	Refer to description of timer D
Others	Miscellaneous register	(MIS)	00 - -	Refer to description of operating modes, and oscillator circuit

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist

Item	Abbr.	Status After Cancellation of Stop Mode by $\overline{\text{STOPC}}$ Input	Status After Cancellation of Stop Mode by MCU Reset	Status After all Other Types of Reset
Carry flag	(CA)	Pre-stop-mode values are not guaranteed; values must be initialized by program		Pre-MCU-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)			
B register	(B)			
W register	(W)			
X/SPX register	(X/SPX)			
Y/SPY register	(Y/SPY)			
Serial data register	(SRL, SRU)			
RAM		Pre-stop-mode values are retained		
RAM enable flag	(RAME)	1	0	0
Port mode register 1 bit 2	(PMRC12)	Pre-stop-mode values are retained	0	0

Interrupts

The MCU has 6 interrupt sources: Two external signals ($\overline{\text{INT}_0}$, $\overline{\text{INT}_1}$), Three timer/counters (timers A, C, and D), and one serial interface (serial 1).

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations \$000 to \$003 and \$020 to \$021 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 6 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 9 and an interrupt processing flowchart is shown in figure 10. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
$\overline{\text{RESET}}$, $\overline{\text{STOPC}}$*	—	$0000
$\overline{\text{INT}}_0$	1	$0002
$\overline{\text{INT}}_1$	2	$0004
Timer A	3	$0006
Not used	4	$0008
Timer C	5	$000A
Timer D	6	$000C
Serial 1	7	$000E

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.

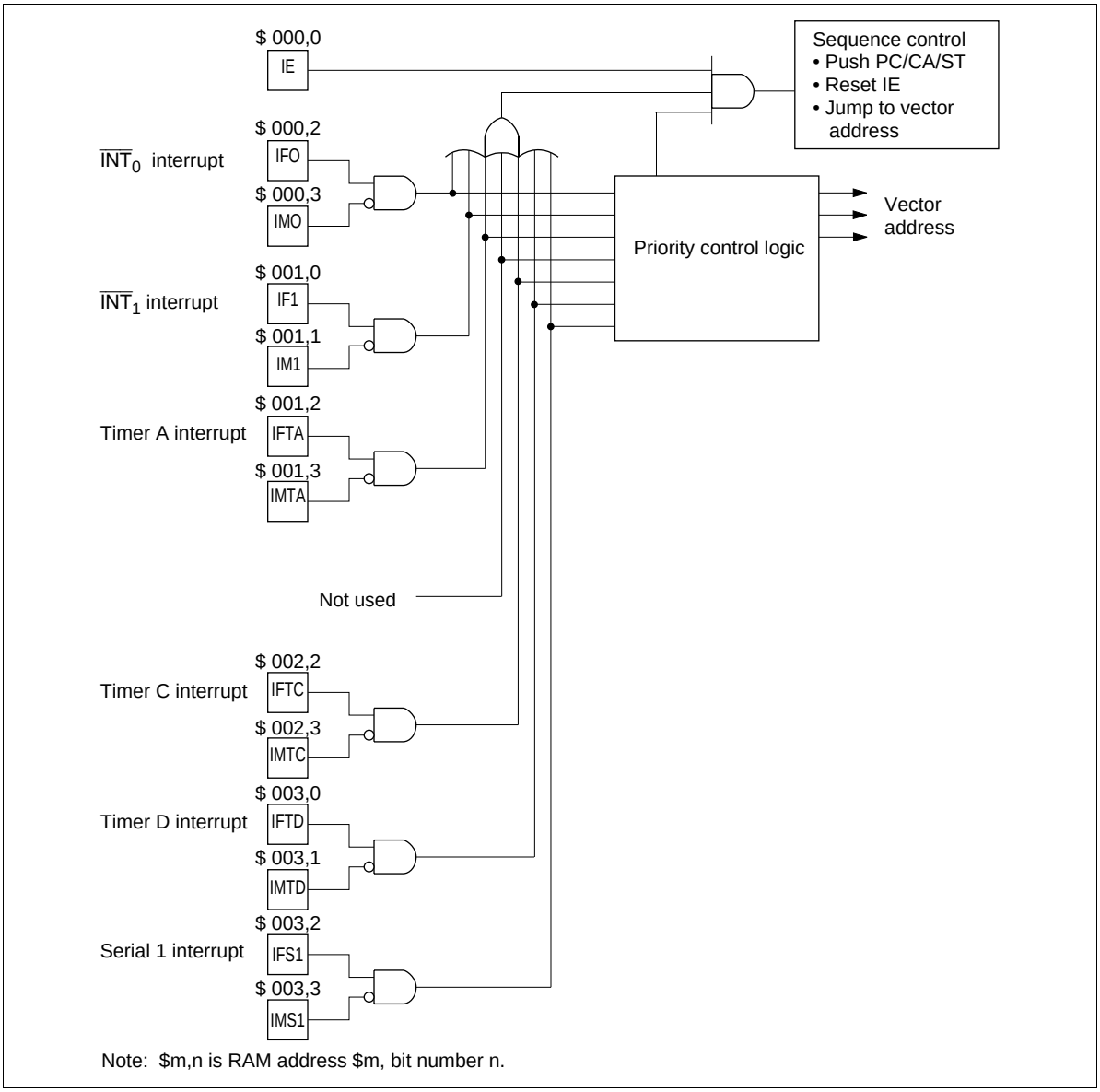


Figure 8 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source					
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**Timer A**	**Timer C**	**Timer D**	**Serial 1**
IE	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0
IFTA · $\overline{IMTA}$	*	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	*	1	0	0
IFTD · $\overline{IMTD}$	*	*	*	*	1	0
IFS1 · $\overline{IMS1}$	*	*	*	*	*	1

Note: * Can be either 0 or 1. Their values have no effect on operation.

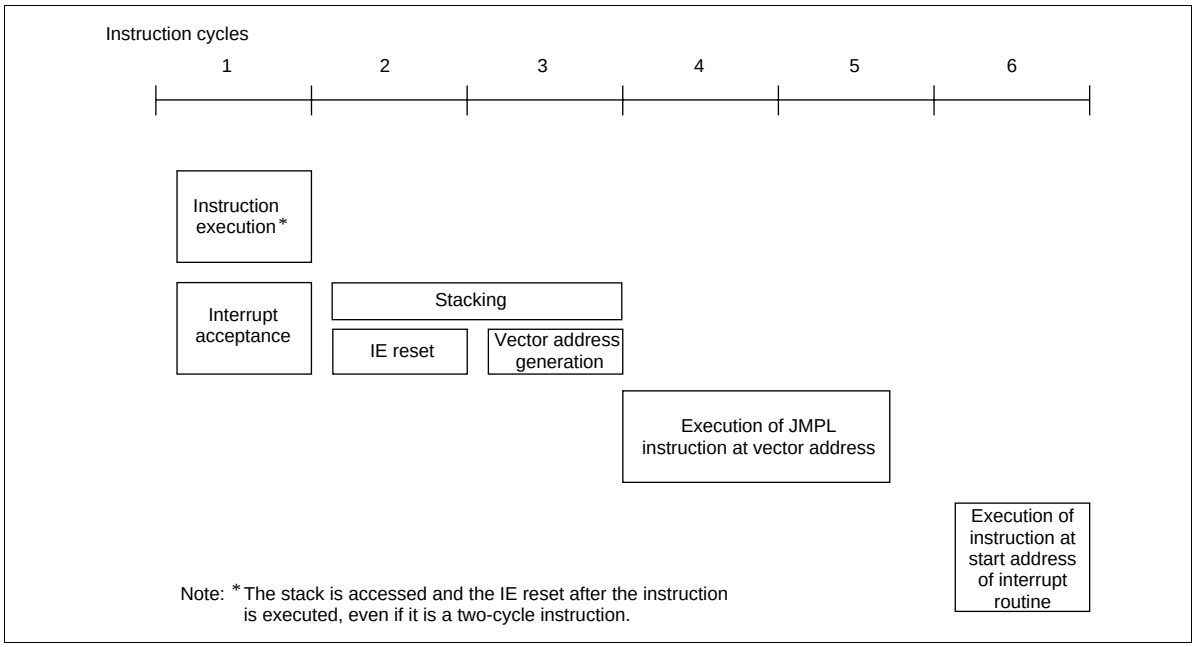


Figure 9 Interrupt Processing Sequence

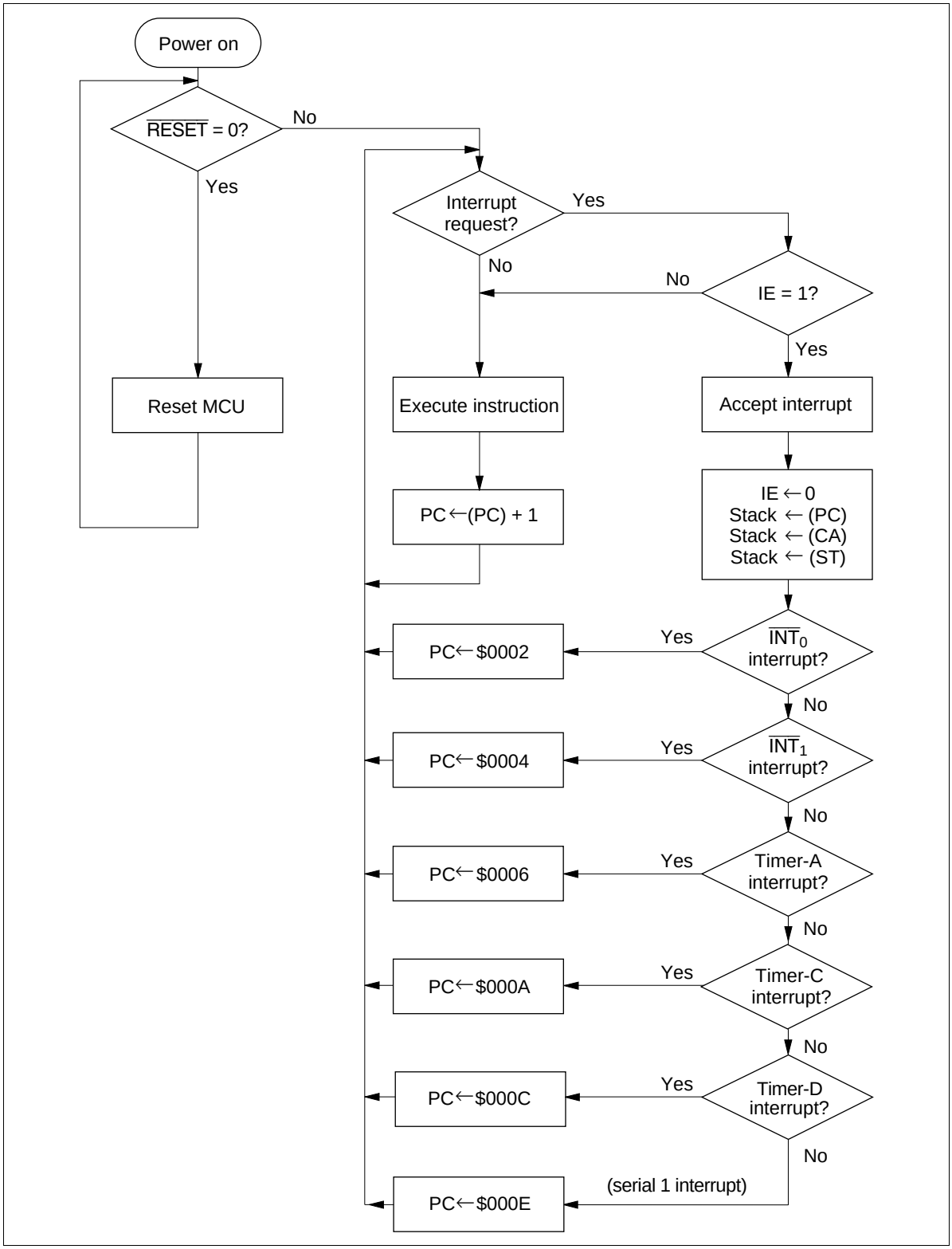


Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT}_0$, $\overline{INT}_1$): Two external interrupt signals.

External Interrupt Request Flags (IF0, IF1: $000, $001): IF0 and IF1 are set the falling of signals input to $\overline{INT}_0$ and $\overline{INT}_1$ as listed in table 5.

Table 5 External Interrupt Request Flags (IF0, IF1: $000, $001)

IF0, IF1	Interrupt Request
0	No
1	Yes

External Interrupt Masks (IM0, IM1: $000, $001): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 ExternalInterrupt Masks (IM0, 1M1: $000, $001)

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A Interrupt Request Flag (IFTA: $001, Bit 2)

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A Interrupt Mask (IMTA: $001, Bit 3)

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C, as listed in table 9.

Table 9 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 10.

Table 10 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer D Interrupt Request Flag (IFTD: $003, Bit 0): Set by overflow output from timer D, or by the rising or falling edge of signals input to EVND when the input capture function is used, as listed in table 11.

Table 11 Timer D Interrupt Request Flag (IFTD: $003, Bit 0)

IFTD	Interrupt Request
0	No
1	Yes

Timer D Interrupt Mask (IMTD: $003, Bit 1): Prevents (masks) an interrupt request caused by the timer D interrupt request flag, as listed in table 12.

Table 12 Timer D Interrupt Mask (IMTD: $003, Bit 1)

IMTD	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flags (IFS1: $003, Bit 2): Set when data transfer is completed or when data transfer is suspended, as listed in table 13.

Table 13 Serial Interrupt Request Flag (IFS1: $003, Bit 2)

IFS1	Interrupt Request
0	No
1	Yes

Serial Interrupt Masks (IMS1: $003, Bit 3): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as listed in table 14.

Table 14 Serial Interrupt Mask (IMS1: $003, Bit 3)

IMS1	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has Three operating modes as shown in table 15. The operations in each mode are listed in tables 16 and 17. Transitions between operating modes are shown in figure 11.

Table 15 Operating Modes and Clock Status

		Mode Name		
		Active	**Standby**	**Stop**
Activation method		$\overline{\text{RESET}}$ cancellation, interrupt request, $\overline{\text{STOPC}}$ cancellation in stop mode	SBY instruction	STOP instruction
Status	System oscillator	OP	OP	Stopped
Cancellation method		$\overline{\text{RESET}}$ input, STOP/SBY instruction	$\overline{\text{RESET}}$ input, interrupt request	$\overline{\text{RESET}}$ input, STOPC input in stop mode

Note: OP implies in operation

Table 16 Operations in Low-Power Dissipation Modes

Function	**Stop Mode**	**Standby Mode**
CPU	Reset	Retained
RAM	Retained	Retained
Timer A	Reset	OP
Timer C	Reset	OP
Timer D	Reset	OP
Serial interface 1	Reset	OP
Comparator	Reset	Stopped
I/O	Reset*	Retained

Note: OP implies in operation

* Output pins are at high impedance.

Table 17 I/O Status in Low-Power Dissipation Modes

	Output		**Input**
	Standby Mode	**Stop Mode**	**Active Mode**
D_0–D_9	Retained	High impedance	Input enabled
D_{12}, D_{13}, RC_0, RD_0–RD_3, RE_0	—	—	Input enabled
R0–R4	Retained or output of peripheral functions	High impedance	Input enabled

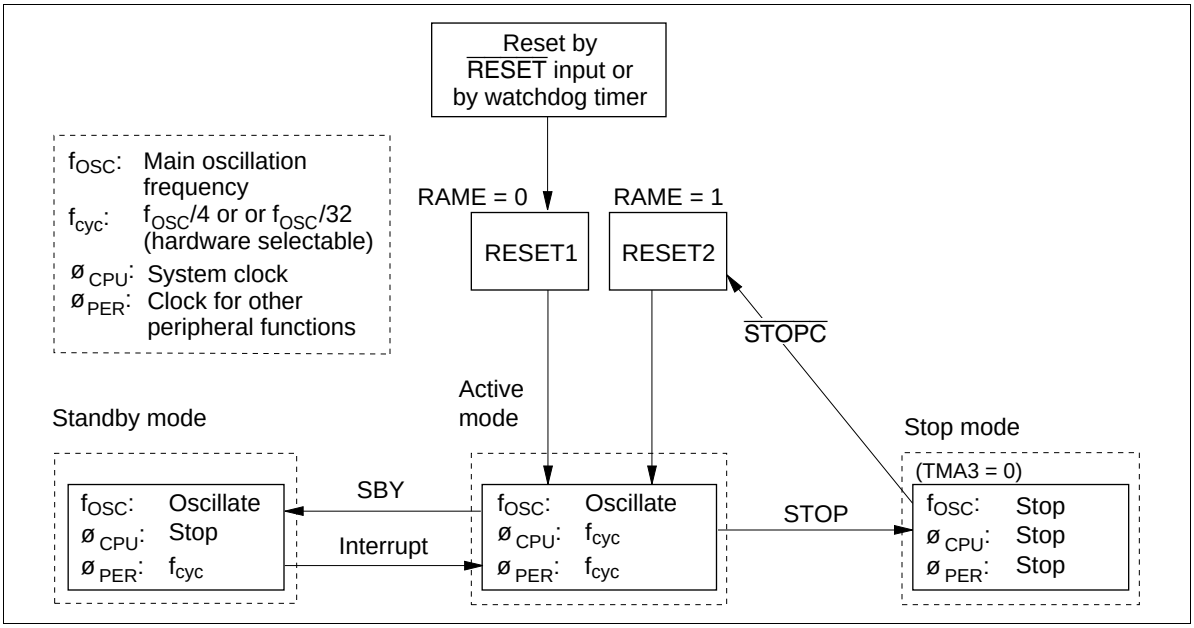


Figure 11 MCU Status Transitions

Active Mode: All MCU functions operate according to the clock generated by the system oscillators OSC_1 and OSC_2.

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops.

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a $\overline{\text{RESET}}$ input or an interrupt request. If it is terminated by $\overline{\text{RESET}}$ input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 12.

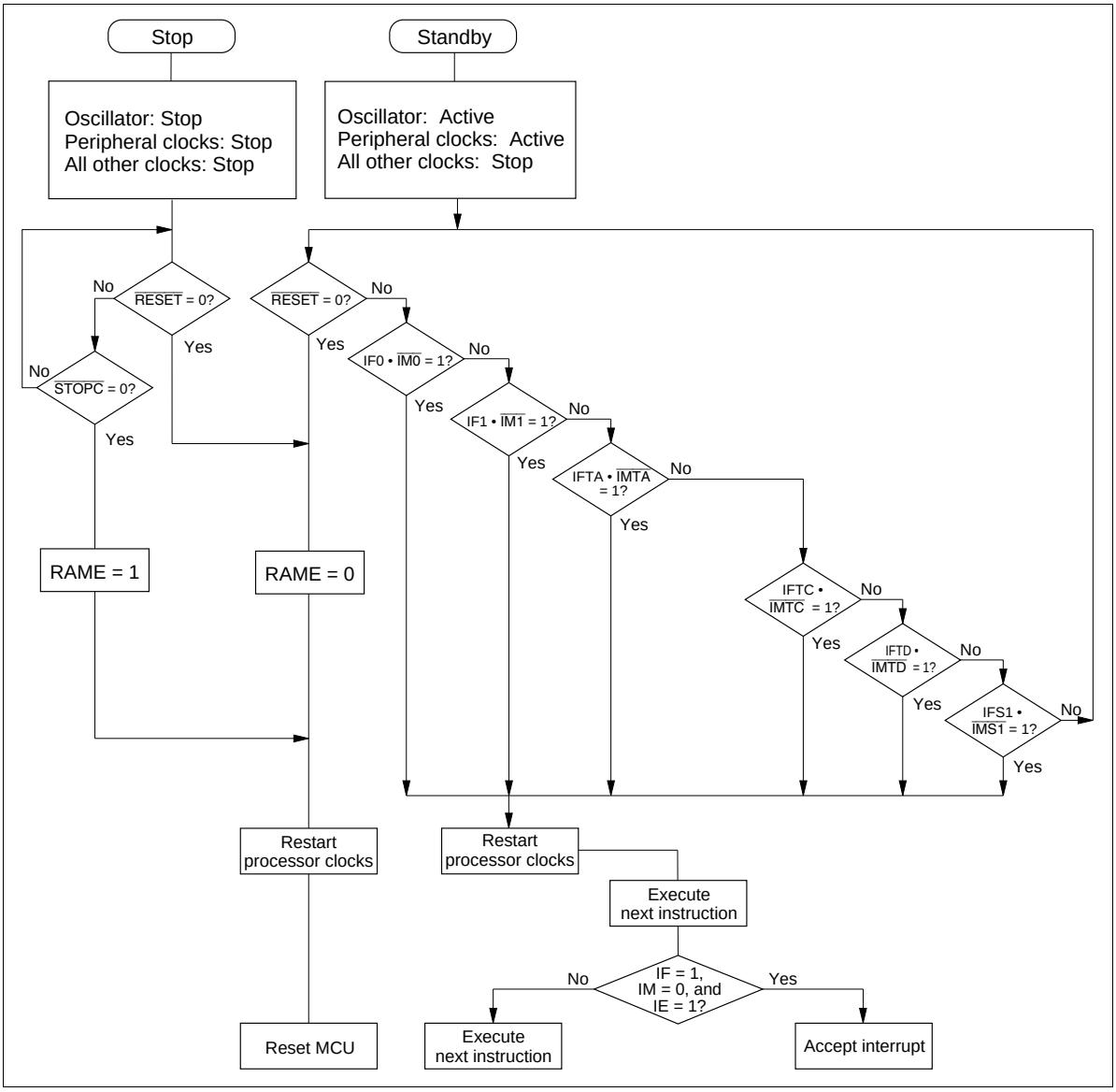


Figure 12 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC_1 and OSC_2 oscillator stops. The MCU enters stop mode if the STOP instruction is executed in active mode.

Stop mode is terminated by a $\overline{\text{RESET}}$ input or a $\overline{\text{STOPC}}$ input as shown in figure 13. $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be applied for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents before entering stop mode are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

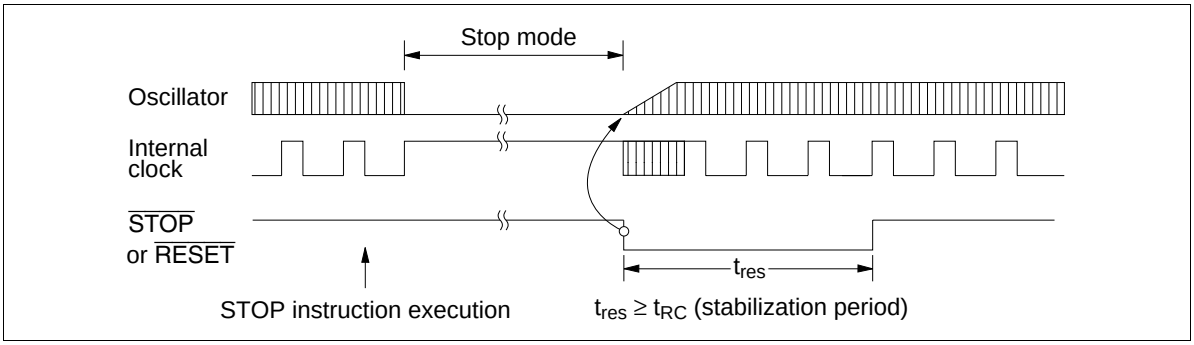


Figure 13 Timing of Stop Mode Cancellation

Stop Mode Cancellation by $\overline{\text{STOPC}}$: The MCU enters active mode from stop mode by inputting $\overline{\text{STOPC}}$ as well as by $\overline{\text{RESET}}$. In either case, the MCU starts instruction execution from the starting address (address 0) of the program. However, the value of the RAM enable flag (RAME: $021, bit 3) differs between cancellation by $\overline{\text{STOPC}}$ and by $\overline{\text{RESET}}$. When stop mode is cancelled by $\overline{\text{RESET}}$, RAME = 0; when cancelled by $\overline{\text{STOPC}}$, RAME = 1. $\overline{\text{RESET}}$ can cancel all modes, but $\overline{\text{STOPC}}$ is valid only in stop mode; $\overline{\text{STOPC}}$ input is ignored in other modes. Therefore, when the program requires to confirm that stop mode has been cancelled by $\overline{\text{STOPC}}$ (for example, when the RAM contents before entering stop mode is used after transition to active mode), execute the TEST instruction to the RAM enable flag (RAME) at the beginning of the program.

MCU Operation Sequence: The MCU operates in the sequences shown in figures 14 to 16. It is reset by an asynchronous $\overline{\text{RESET}}$ input, regardless of its status.

The low-power mode operation sequence is shown in figure 16. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

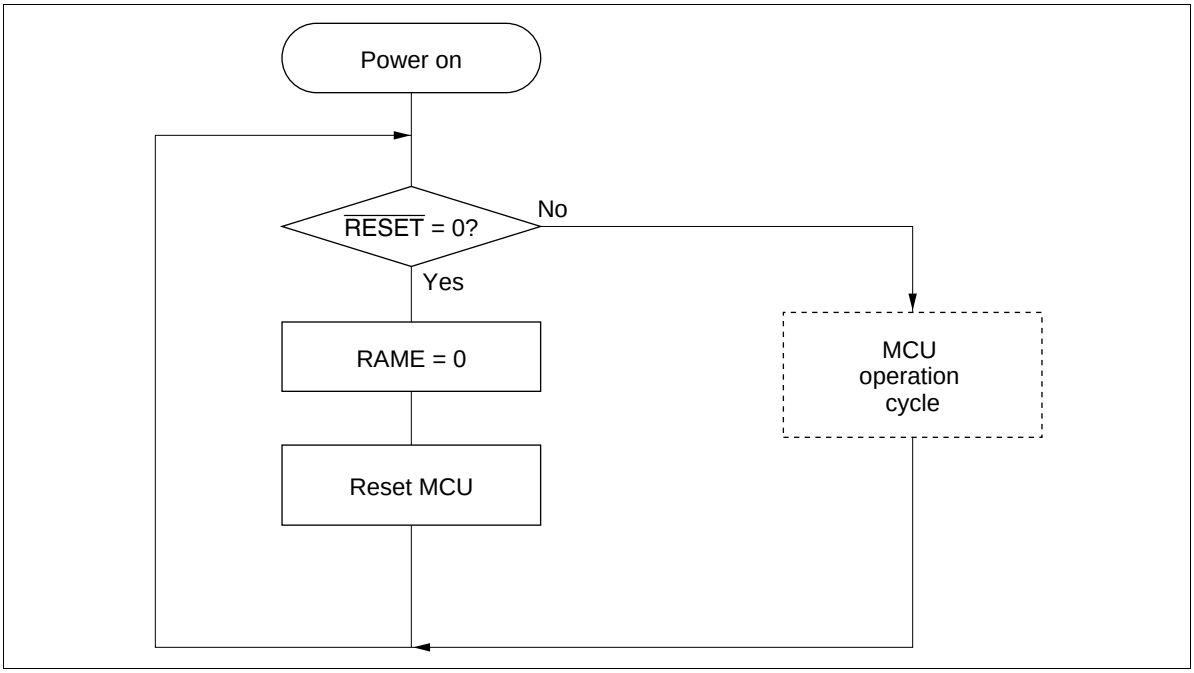


Figure 14 MCU Operating Sequence (Power On)

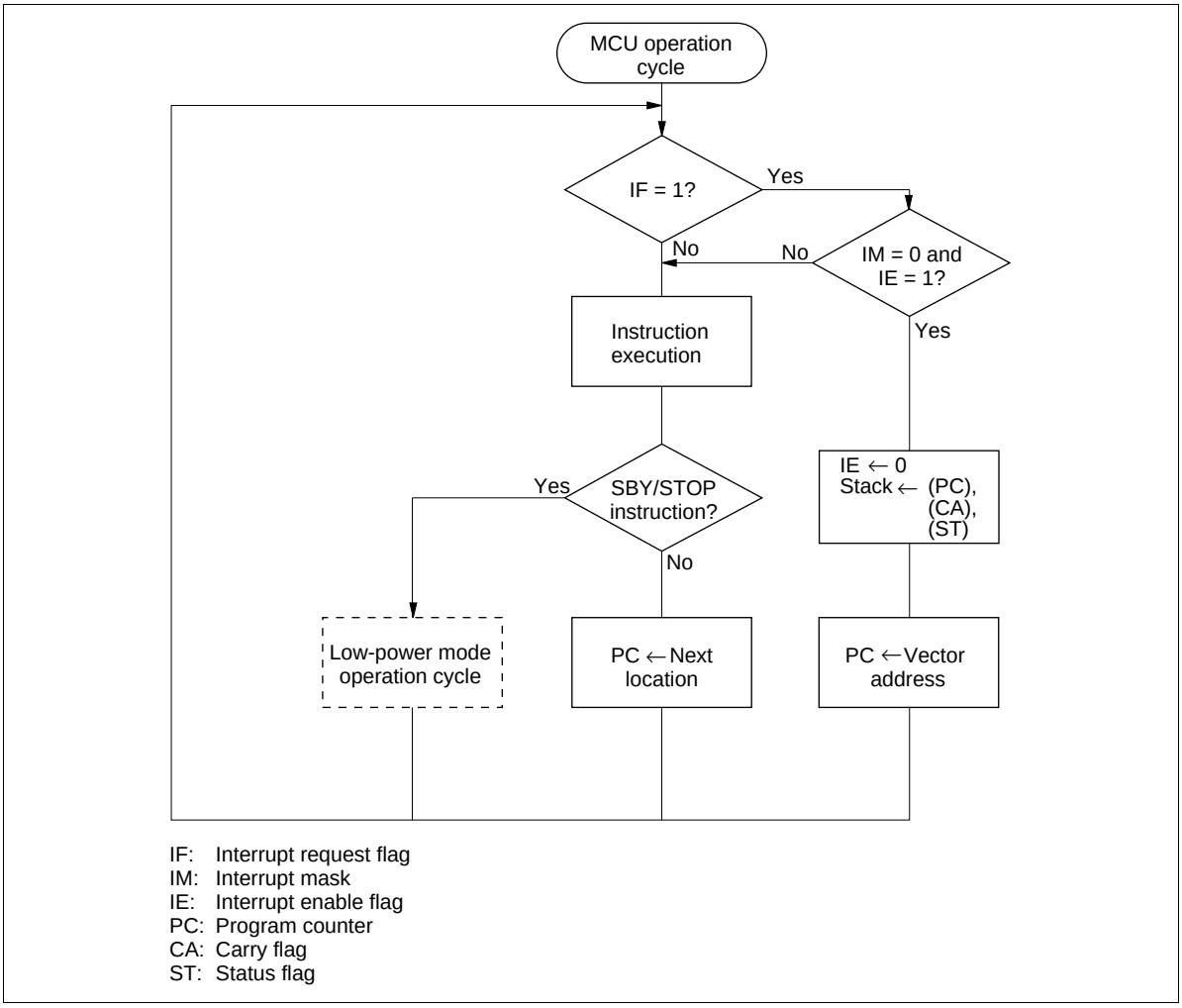
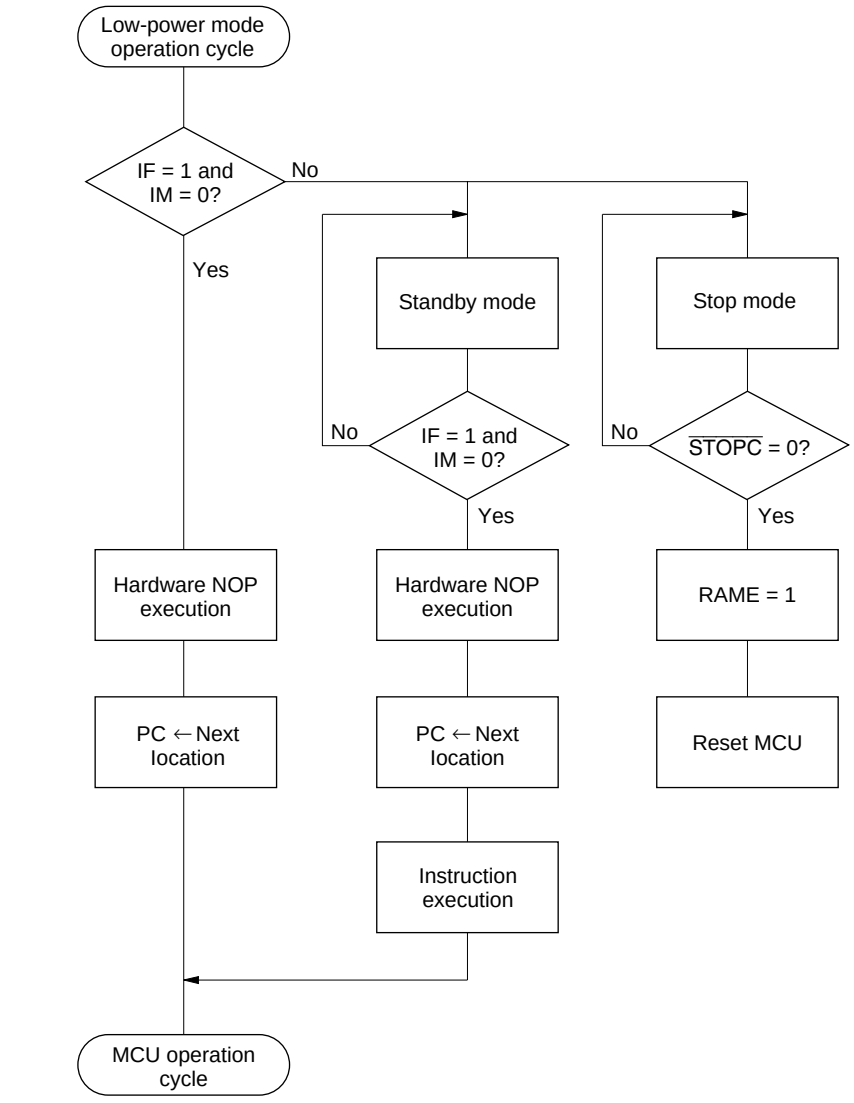


Figure 15 MCU Operating Sequence (MCU Operation Cycle)



For IF and IM operation, refer to figure 12.

Figure 16 MCU Operating Sequence (Low-Power Mode Operation)

Internal Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 17. As shown in table 18, a ceramic oscillator can be connected to OSC_1 and OSC_2. The system oscillator can also be operated by an external clock.

After $\overline{RESET}$ input or after stop mode has been cancelled, the division ratio of the system clock can be selected as 1/4 or 1/32 by setting the SEL pin level.

- 1/4 division ratio: Connect SEL to V_{CC}.
- 1/32 division ratio: Connect SEL to GND.

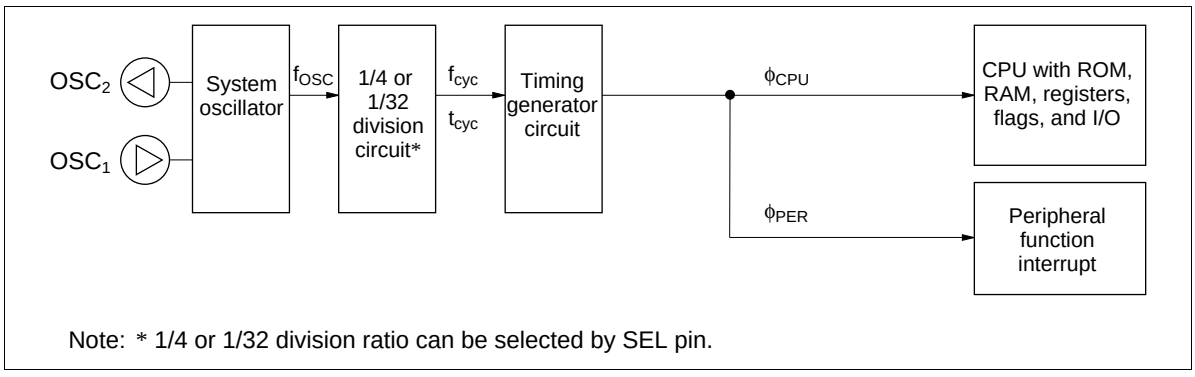


Figure 17 Clock Generation Circuit

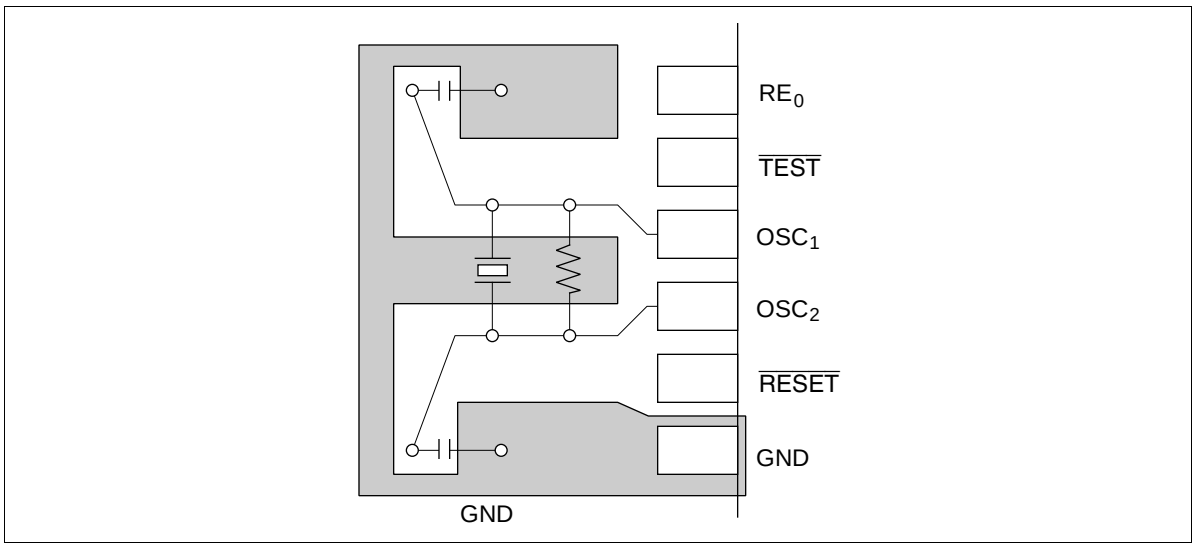
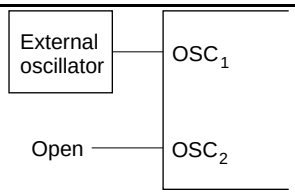
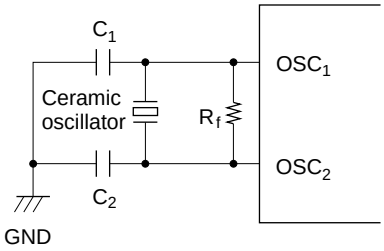


Figure 18 Typical Layout of Ceramic Oscillator

Table 18 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSB400P22 (Murata), CSB400P (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
		Ceramic oscillator: CSB800J122 (Murata), CSB800J (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
		Ceramic oscillator: CSA2.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
		Ceramic oscillator: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%
		Ceramic oscillator: CSA3.58MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 30 pF ± 20%

Notes: 1. Since the circuit constants change depending on the ceramic oscillator and stray capacitance of the board, the user should consult with the ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 18).

Input/Output

The MCU has 27 input/output pins (D_0–D_9, $R0_0$–$R4_3$) and 8 input pins (D_{12}, D_{13}, RC_0, RD_0– RD_3, RE_0). The features are described below. Some input/output pins have different features between the HD404054 Series and HD404094 Series. The differences between the HD404054 Series and HD404094 Series are listed in table 19.

- A maximum current of 15 mA is allowed for each of the pins D_4 to D_9 with a total maximum current of less than 105 mA. In addition, D_0–D_3 can each act as a 10-mA maximum current source.
- Some input/output pins are multiplexed with peripheral function pins such as for the timers or serial interface. For these pins, the peripheral function setting is done prior to the D or R port setting. Therefore, when a peripheral function is selected for a pin, the pin function and input/output selection are automatically switched according to the setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are CMOS output pins. Only the $R4_3/SO_1$ pin can be set to NMOS open-drain output by software.
- In stop mode, the MCU is reset, and therefore peripheral function selection is cancelled. Input/output pins are in high-impedance state.
- Pins D_0–D_3 have built-in pull-down MOSs, and other input/output pins have built-in pull-up MOSs, which can be individually turned on or off by software.

I/O buffer configuration is shown in figure 19 programmable I/O circuits are listed in table 20, and I/O pin circuit types are shown in table 21.

Table 19 The differences between HD404054 Series and HD404094 Series

	HD404054 Series	HD404094 Series
Large-current source pins (15 mA)	D_0–D_3	D_0–D_3
Large-current sink pins (10 mA)	D_4–D_9	D_8, D_9
Intermediate voltage NMOS open-drain pins (12 V)	—	D_4–D_7 (output only)
Pull-down MOS current pins	D_0–D_3	D_0–D_3
Pull-up MOS current pins	D_4–D_9, R0–R4	D_8, D_9, R0–R4

Table 20-1 Programmable I/O Circuits (with pull-up MOS)

MIS3 (Bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off status.

Table 20-2 Programmable I/O Circuits (with pull-down MOS)

MIS3 (Bit 3 of MIS)		0				1			
DCD, DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-down MOS		—	—	—	—	On	—	On	—

Note: — indicates off status.

D_4–D_9, R port (HD404054 Series)
D_8, D_9, R port (HD404094 Series)

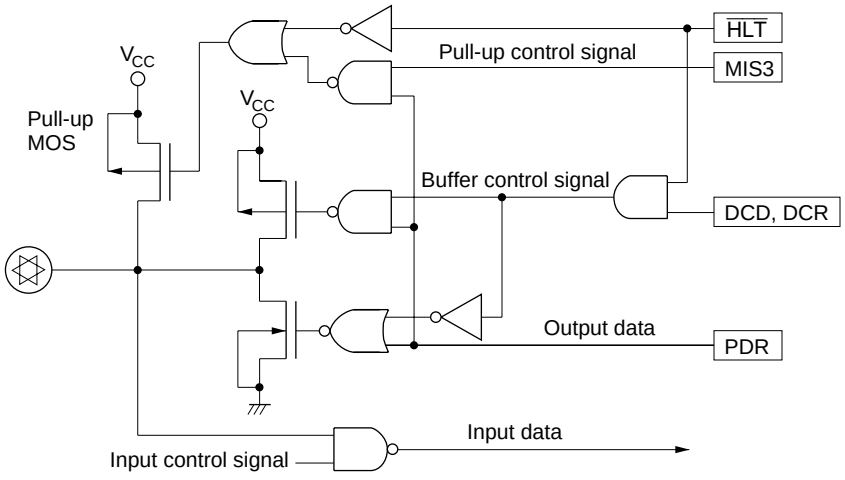


Figure 19-1 I/O Buffer Configuration (with pull-up MOS)

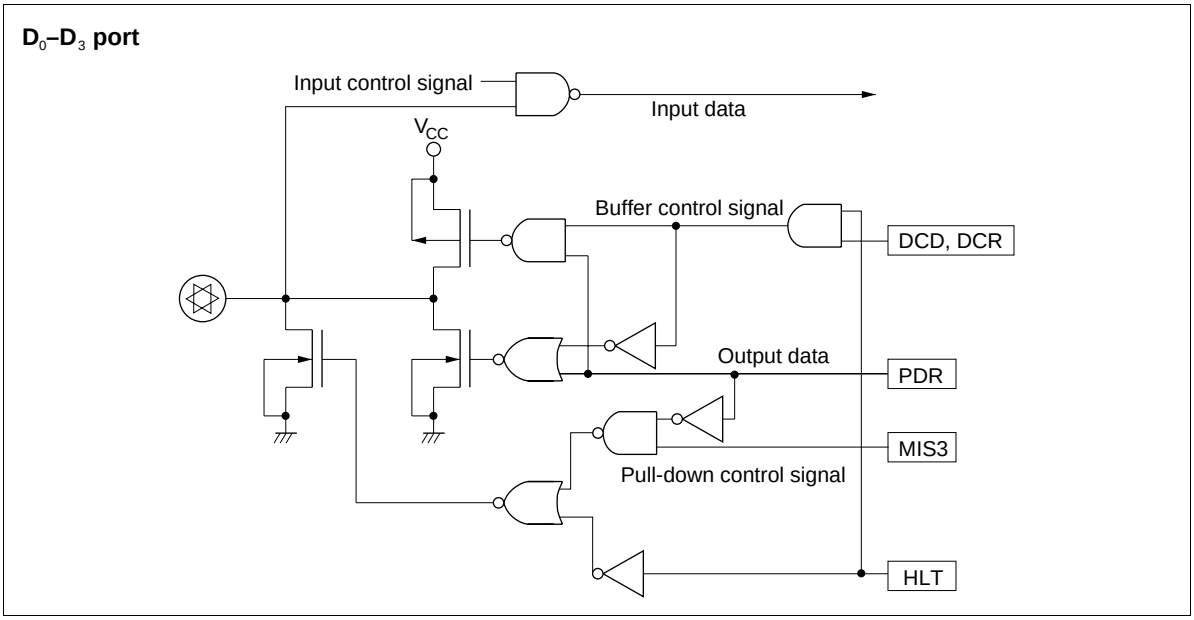
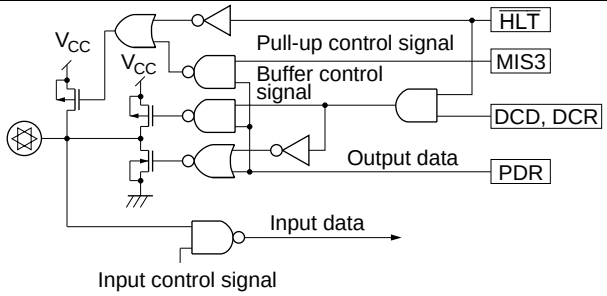
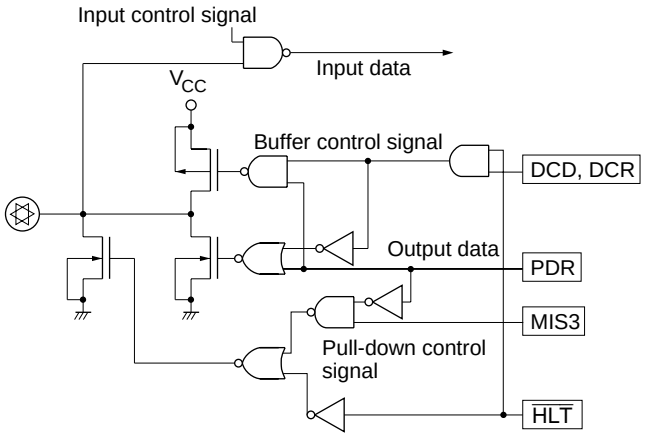
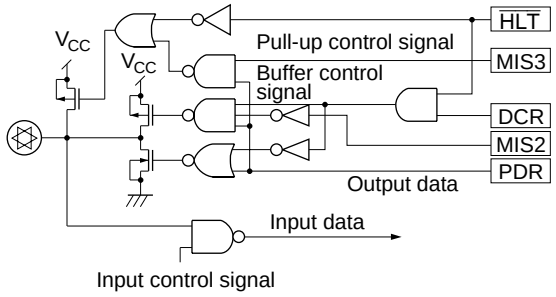
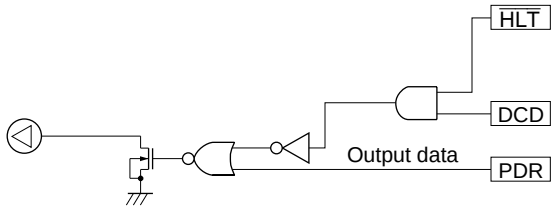
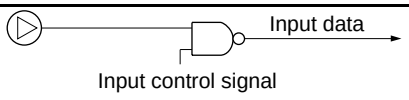
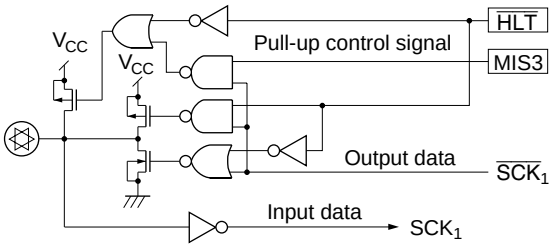
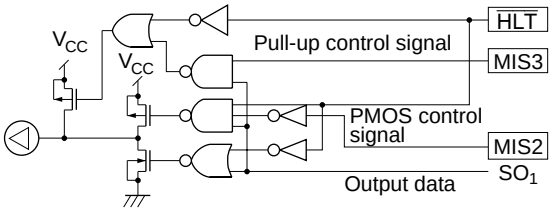
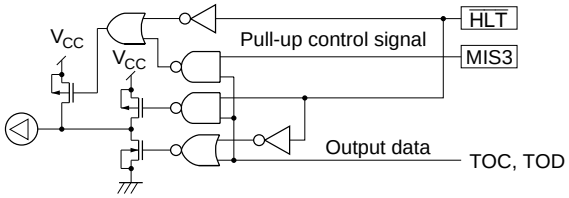
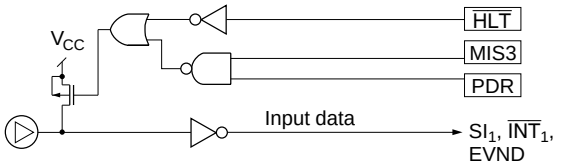
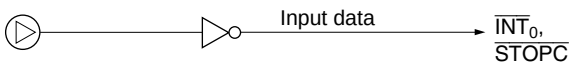


Figure 19-2 I/O Buffer Configuration (with pull-down MOS)

Table 21 Circuit Configurations of I/O Pins

I/O Pin Type	Circuit	Pins	
		HD404054 Series	HD404094 Series
Input/output pins		D_4–D_9, R0–R4	D_8, D_9, R0–R4
		D_0–D_3	D_0–D_3
		$R4_3$	$R4_3$
Output pins		—	D_4–D_7

I/O Pin Type		Circuit	Pins: HD404054 Series	Pins: HD404094 Series
Input pins			D_{12}, D_{13}, RC_0 RD_0–RD_3, RE_0	D_{12}, D_{13}, RC_0 RD_0–RD_3, RE_0
Peripheral function pins	Input/ output pins		$\overline{SCK_1}$	$\overline{SCK_1}$
	Output pins		SO_1	SO_1
			TOC, TOD	TOC, TOD
	Input pins		SI_1, $\overline{INT_1}$, EVND	SI_1, $\overline{INT_1}$, EVND
			$\overline{INT_0}$, $\overline{STOPC}$	$\overline{INT_0}$, $\overline{STOPC}$

Note: The MCU is reset in stop mode, and peripheral function selection is cancelled. The $\overline{HLT}$ signal becomes low, and input/output pins enter high-impedance state.

D Port (D_0–D_{13}): Consist of 10 input/output pins and 2 input pins addressed by one bit. D_0–D_3 are high-current sources, and D_{12} and D_{13} are input-only pins. D_4–D_9 of the HD404054 Series are high-current sinks. D_4–D_7 of the HD404094 Series are middle voltage output-only pins, and D_8 and D_9 are high-current sink pins.

Pins D_0–D_9 are set by the SED and SEDD instructions, and reset by the RED and REDD instructions. Output data is stored in the port data register (PDR) for each pin. All pins D_0–D_{13} are tested by the TD and TDD instructions.

The on/off statuses of the output buffers are controlled by D-port data control registers (DCD0–DCD2: $02C–$02E) that are mapped to memory addresses (figure 20).

Pins D_{12} and D_{13} are multiplexed with peripheral function pins $\overline{STOPC}$ and $\overline{INT_0}$, respectively. The peripheral function modes of these pins are selected by bits 2 and 3 (PMRC2, PMRC3) of port mode register C (PMRC: $025) (figure 22).

R Ports ($R0_0$–RE_0): 17 input/output pins and 6 input pins addressed in 4-bit units. Data is input to these ports by the LAR and LBR instructions, and output from them by the LRA and LRB instructions. *Output data is stored in the port data register (PDR) for each pin. The on/off statuses of the output buffers of the R ports are controlled by R-port data control registers (DCR0–DCR4: $030–$034) that are mapped to memory addresses (figure 20).

Pin $R0_0$ is are multiplexed with peripheral pin $\overline{INT_1}$ respectively. The peripheral function modes of these pins are selected by bit 0 (PMRB0) of port mode register B (PMRB: $024) (figure 21).

Pins $R3_1$–$R3_2$ are multiplexed with peripheral pins TOC and TOD respectively. The peripheral function modes of these pins are selected by bits 0–2 (TMC20–TMC22) of timer mode register C2 (TMC2: $014), and bits 0–3 (TMD20–TMD23) of timer mode register D2 (TMD2: $015) (figures 23, and 24).

Pin $R4_0$ is multiplexed with peripheral pin EVND respectively. The peripheral function modes of these pins are selected by bit 1 (PMRC1) of port mode register C (PMRC: $025) (figure 22).

Pins $R4_1$–$R4_3$ are multiplexed with peripheral pins $\overline{SCK_1}$, SI_1, and SO_1, respectively. The peripheral function modes of these pins are selected by bit 3 (SM1A3) of serial mode register 1A (SM1A: $005), and bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004), as shown in figures 25 and 26.

Ports RD_0 and RD_1 are multiplexed with peripheral function pins $COMP_0$ and $COMP_1$, respectively. The function modes of these pins are selected by bit 3 (CER3) of the compare enable register (CER: $018) (figure 27).

Port RE_0 is multiplexed with peripheral function pin VC_{ref}. While functioning as VC_{ref}, do not use this pin as an R port at the same time, otherwise, the MCU may malfunction.

Pull-Up or Pull-Down MOS Transistor Control: A program-controlled pull-up or pull-down MOS transistor is provided for each input/output pin other than input-only pins D_{12} and D_{13}. The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (table 20 and figure 28).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ or pulled down to GND by their pull-down MOS transistors.

Note: *If nonexisted bits of R ports is read, undifined data will be latched to accumulator (A) or the B register.

Data control register (DCD0 to 2: $02C to $02E) (DCR0 to 4: $030 to $034)

DCD0, DCD1

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03–DCD13	DCD02–DCD12	DCD01–DCD11	DCD00–DCD10

DCD2

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	DCD21	DCD20

DCR0

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	W
Bit name	Not used	Not used	Not used	DCR00

DCR1 to DCR4

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR13–DCR43	DCR12–DCR42	DCR11–DCR41	DCR10–DCR40

All Bits	CMOS Buffer On/Off Selection
0	Off (high-impedance)
1	On

Correspondence between ports and DCD/DCR bits

Register Name	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	D_7	D_6	D_5	D_4
DCD2	—	—	D_9	D_8
DCR0	—	—	—	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCR4	$R4_3$	$R4_2$	$R4_1$	$R4_0$

Figure 20 Data Control Registers (DCD, DCR)

Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	W
Bit name	Not used	Not used	Not used	PMRB0

PMRB0	$R0_0/\overline{INT}_1$ mode selection
0	$R0_0$
1	$\overline{INT}_1$

Figure 21 Port Mode Register B (PMRB)

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	PMRC3	PMRC2*	PMRC1	Not used

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	$D_{12}/\overline{STOPC}$ mode selection
0	D_{12}
1	$\overline{STOPC}$

PMRC3	$D_{13}/\overline{INT}_0$ mode selection
0	D_{13}
1	$\overline{INT}_0$

Note: * PMRC2 is reset to 0 only by $\overline{RESET}$ input. When $\overline{STOPC}$ is input in stop mode, PMRC2 is not reset but retains its value.

Figure 22 Port Mode Register C (PMRC)

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	—	Inhibited
		1		
	1	0		
		1	TOC	PWM output

Figure 23 Timer Mode Register C2 (TMC2)

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	—	Inhibited
			1		
		1	0		
			1	TOD	PWM output
1	×	×	×	$R3_2$	Input capture ($R3_2$ port)

×: Don't care

Figure 24 Timer Mode Register D2 (TMD2)

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	PMRA1	PMRA0

PMRA0	$R4_3$/SO_1 mode selection
0	$R4_3$
1	SO_1

PMRA1	$R4_2$/SI_1 mode selection
0	$R4_2$
1	SI_1

Figure 25 Port Mode Register A (PMRA)

Serial mode register 1A (SM1A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM1A3	SM1A2	SM1A1	SM1A0

SM1A3	$R4_1/\overline{SCK_1}$ mode selection
0	$R4_1$
1	$\overline{SCK_1}$

SM1A2	SM1A1	SM1A0	$\overline{SCK_1}$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	÷2048
		1	Output	Prescaler	÷512
	1	0	Output	Prescaler	÷128
		1	Output	Prescaler	÷32
1	0	0	Output	Prescaler	÷8
		1	Output	Prescaler	÷2
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 26 Serial Mode Register 1A (SM1A)

Compare enable register (CER: $018)

Bit	3	2	1	0
Initial value	0	—	0	0
Read/Write	W	—	W	W
Bit name	CER3	Not used	CER1	CER0

CER3	Digital/Analog selection
0	Digital input mode: $RD_0/COMP_0$ and $RD_1/COMP_1$ operate as an R port.
1	Analog input mode: $RD_0/COMP_0$ and $RD_1/COMP_1$ operate as analog input.

CER1	CER0	Analog input pin selection
0	0	$COMP_0$
0	1	$COMP_1$
1	0	Not used
1	1	Not used

Figure 27 Compare Enable Register

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS3	Pull-up MOS on/off selection
0	Off
1	On

MIS2	CMOS buffer on/off selection for pin $R4_3/SO_1$
0	On
1	Off

Figure 28 Miscellaneous Register (MIS)

Prescalers

The MCU has the following prescaler S.

The prescaler operating conditions are listed in table 22, and the prescaler output supply is shown in figure 29. The timers A, C, D input clocks except external events and the serial transmit clock except the external clock are selected from the prescaler outputs, depending on corresponding mode registers.

Prescaler Operation

Prescaler S: 11-bit counter that inputs a system clock signal. After being reset to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except at MCU reset.

Table 22 Prescaler Operating Conditions

Prescaler	Input Clock	Reset Condition	Stop Conditions
Prescaler S	System clock	MCU reset	MCU reset, stop mode

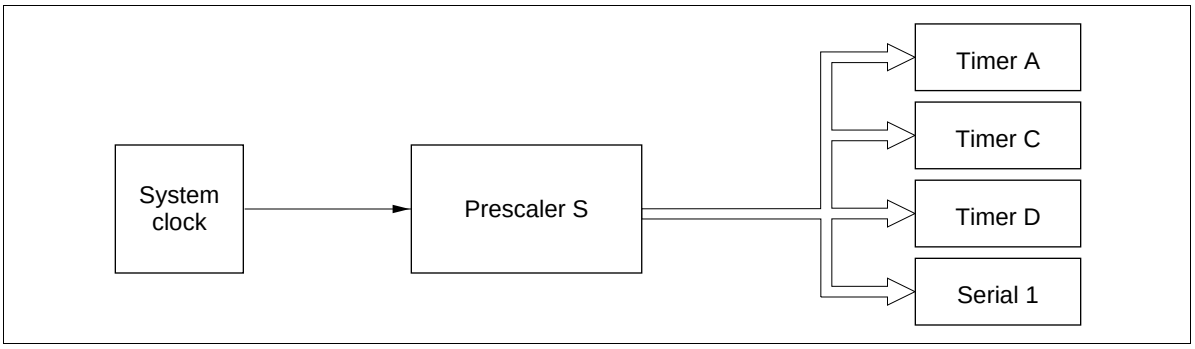


Figure 29 Prescaler Output Supply

Timers

The MCU has three timer/counters (A, C, and D).

- Timer A: Free-running timer
- Timer C: Multifunction timer
- Timer D: Multifunction timer

Timer A is an 8-bit free-running timer. Timers C and D are 8-bit multifunction timers, whose functions are listed in table 23. The operating modes are selected by software.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
  The block diagram of timer A is shown in figure 30.

Timer A Operations:

- Free-running timer operation: The input clock for timer A is selected by timer mode register A (TMA: $008).
  Timer A is reset to $00 by MCU reset and incremented at each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow is generated, and timer A is reset to $00. The overflow sets the timer A interrupt request flag (IFTA: $001, bit 2). Timer A continues to be incremented after reset to $00, and therefore it generates regular interrupts every 256 clocks.

Registers for Timer A Operation: Timer A operating modes are set by the following registers.

- Timer mode register A (TMA: $008): Four-bit write-only register that selects timer A's operating mode and input clock source as shown in figure 31.

Table 23 Timer Functions

Functions		Timer A	Timer C	Timer D
Clock source	Prescaler S	Available	Available	Available
	External event	—	—	Available
Timer functions	Free-running	Available	Available	Available
	Event counter	—	—	Available
	Reload	—	Available	Available
	Watchdog	—	Available	—
	Input capture	—	—	Available
Timer outputs	Toggle	—	Available	Available
	0 output	—	Available	Available
	1 output	—	Available	Available
	PWM	—	Available	Available

Note: — means not available.

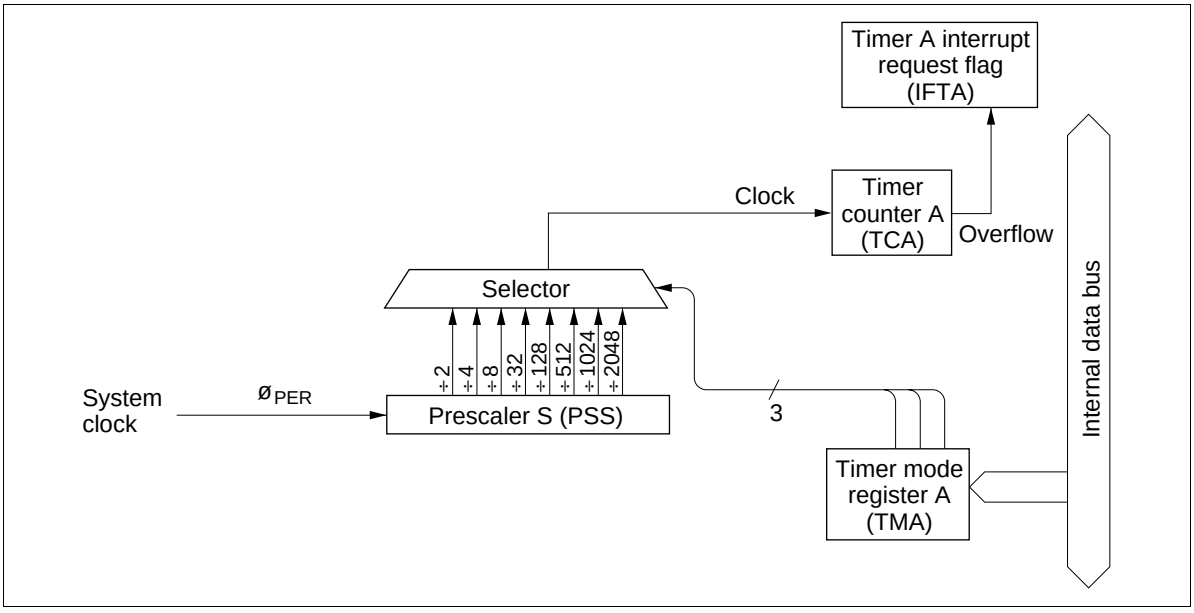


Figure 30 Block Diagram of Timer A

Timer mode register A (TMA: $008)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMA2	TMA1	TMA0

TMA2	TMA1	TMA0	Source prescaler	Input clock frequency	Operating mode
0	0	0	PSS	$2048t_{cyc}$	Timer A mode
		1	PSS	$1024t_{cyc}$	
	1	0	PSS	$512t_{cyc}$	
		1	PSS	$128t_{cyc}$	
1	0	0	PSS	$32t_{cyc}$	
		1	PSS	$8t_{cyc}$	
	1	0	PSS	$4t_{cyc}$	
		1	PSS	$2t_{cyc}$	

Note: Timer counter overflow output period (seconds) = input clock period (seconds) × 256.

Figure 31 Timer Mode Register A (TMA)

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle, 0, 1, and PWM outputs)

The block diagram of timer C is shown in figure 32.

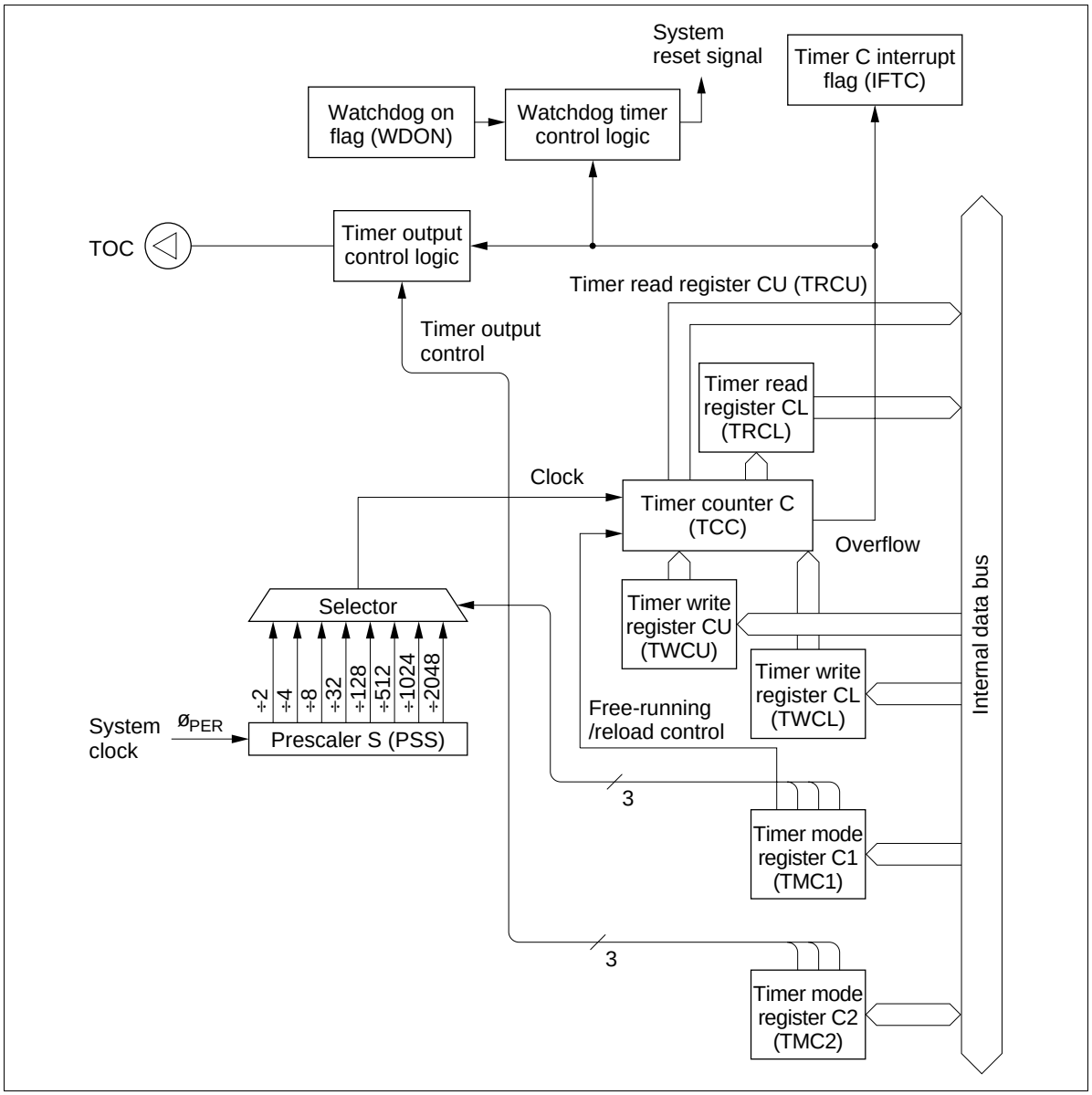


Figure 32 Block Diagram of Timer C

Timer C Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C1 (TMC1: $00D).

  Timer C is initialized to the value set in timer write register C (TWCL: $00E, TWCU: $00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2). IFTC is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: $020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. Program run can be controlled by initializing timer C by software before it reaches $FF.

- Timer output operation: The following four output modes can be selected for timer C by setting timer mode register C2 (TMC2: $014).

  Toggle

  0 output

  1 output

  PWM output

  By selecting the timer output mode, pin $R3_1$/TOC is set to TOC. The output from TOC is reset low by MCU reset.

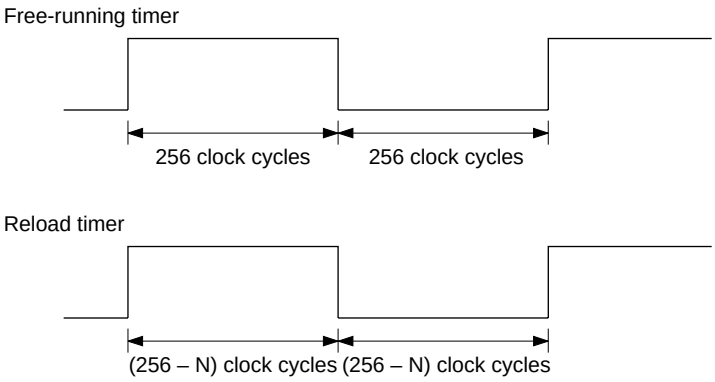
  — Toggle output: When toggle output mode is selected, the output level is inverted if a clock is input after timer C has reached $FF. By using this function and reload timer function, clock signals can be output at a required frequency for the buzzer. The output waveform is shown in figure 33.

  — PWM output: When PWM output mode is selected, timer C provides the variable-duty pulse output function. The output waveform differs depending on the contents of timer mode register C1 (TMC1: $00D) and timer write register C (TWCL: $00E, TWCU: $00F). The output waveform is shown in figure 33.

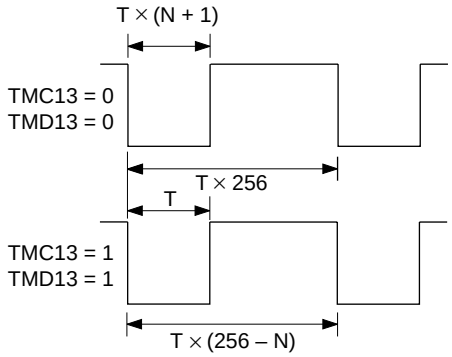
  — 0 output: When 0 output mode is selected, the output level is pulled low if a clock is input after timer C has reached $FF. Note that this function must be used only when the output level is high.

  — 1 output: When 1 output mode is selected, the output level is set high if a clock is input after timer C has reached $FF. Note that this function must be used only when the output level is low.

Toggle output waveform (timers C, and D)



PWM output waveform (timers C and D)



Notes: The waveform is always fixed low when N = $FF.
T: Input clock period to counter (figures 34 and 41)
N: The value of the timer write register

Figure 33 Timer Output Waveform

Registers for Timer C Operation: By using the following registers, timer C operation modes are selected and the timer C count is read and written.

Timer mode register C1 (TMC1: $00D)

Timer mode register C2 (TMC2: $014)

Timer write register C (TWCL: $00E, TWCU: $00F)

Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C1 (TMC1: $00D): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 34. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C1 write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: $00E, TWCU: $00F) must be done after a mode change becomes valid.

Timer mode register C1 (TMC1: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC13	TMC12	TMC11	TMC10

TMC13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMC12	TMC11	TMC10	Input clock period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

Figure 34 Timer Mode Register C1 (TMC1)

- Timer mode register C2 (TMC2: $014): Three-bit read/write register that selects the timer C output mode as shown in figure 35. It is reset to $0 by MCU reset.

Timer mode register C2 (TMC2: $014)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	R/W	R/W	R/W
Bit name	Not used	TMC22	TMC21	TMC20

TMC22	TMC21	TMC20	$R3_1$/TOC mode selection	
0	0	0	$R3_1$	$R3_1$ port
		1	TOC	Toggle output
	1	0	TOC	0 output
		1	TOC	1 output
1	0	0	—	Inhibited
		1		
	1	0		
		1	TOC	PWM output

Figure 35 Timer Mode Register C2 (TMC2)

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of a lower digit (TWCL) and an upper digit (TWCU) as shown in figures 36 and 37. The lower digit is reset to $0 by MCU reset, but the upper digit value is invalid.

  Timer C is initialized by writing to timer write register C (TWCL: $00E, TWCU: $00F). In this case, the lower digit (TWCL) must be written to first, but writing only to the lower digit does not change the timer C value. Timer C is initialized to the value in timer write register C at the same time the upper digit (TWCU) is written to. When timer write register C is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer C.

Timer write register C (lower digit) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 36 Timer Write Register C Lower Digit (TWCL)

Timer write register C (upper digit) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 37 Timer Write Register C Upper Digit (TWCU)

- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of a lower digit (TRCL) and an upper digit (TRCU) that holds the count of the timer C upper digit as shown in figures 38 and 39. The upper digit (TRCU) must be read first. At this time, the count of the timer C upper digit is obtained, and the count of the timer C lower digit is latched to the lower digit (TRCL). After this, by reading TRCL, the count of timer C when TRCU is read can be obtained.

Timer read register C (lower digit) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 38 Timer Read Register C Lower Digit (TRCL)

Timer read register C (upper digit) (TRCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 39 Timer Read Register C Upper Digit (TRCU)

Timer D

Timer D Functions: Timer D has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle, 0, 1, and PWM outputs)
- Input capture timer

The block diagram for each operation mode of timer D is shown in figures 40-1 and 40-2.

Timer D Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register D1 (TMD1: $010).

  Timer D is initialized to the value set in timer write register D (TWDL: $011, TWDU: $012) by software and incremented by one at each clock input. If an input clock is applied to timer D after it has reached $FF, an overflow is generated. In this case, if the reload timer function is enabled, timer D is initialized to its initial value set in timer write register D; if the free-running timer function is enabled, the timer is initialized to $00 and then incremented again.

  The overflow sets the timer D interrupt request flag (IFTD: $003, bit 0). IFTD is reset by software or MCU reset. Refer to figure 3 and table 1 for details.

- External event counter operation: Timer D is used as an external event counter by selecting the external event input as an input clock source. In this case, pin $R4_0$/EVND must be set to EVND by port mode register C (PMRC: $025).

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by detection edge select register 2 (ESR2: $027). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

  Timer D is incremented by one at each detection edge selected by detection edge select register 2 (ESR2: $027). The other operation is basically the same as the free-running/reload timer operation.

- Timer output operation: The following four output modes can be selected for timer D by setting timer mode register D2 (TMD2: $015).

  Toggle

  0 output

  1 output

  PWM output

  By selecting the timer output mode, pin $R3_2$/TOD is set to TOD. The output from TOD is reset low by MCU reset.

  — Toggle output: The operation is basically the same as that of timer-C's toggle output.

  — 0 output: The operation is basically the same as that of timer-C's 0 output.

  — 1 output: The operation is basically the same as that of timer-C's 1 output.

— PWM output: The operation is basically the same as that of timer-C's PWM output.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVND.

  Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by detection edge select register 2 (ESR2: $027).

  When a trigger edge is input to EVND, the count of timer D is written to timer read register D (TRDL: $011, TRDU: $012), and the timer D interrupt request flag (IFTD: $003, bit 0) and the input capture status flag (ICSF: $021, bit 0) are set. Timer D is reset to $00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer D, or if timer D generates an overflow, the input capture error flag (ICEF: $021, bit 1) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

  By selecting the input capture operation, pin $R3_2$/TOD is set to $R3_2$ and timer D is reset to $00.

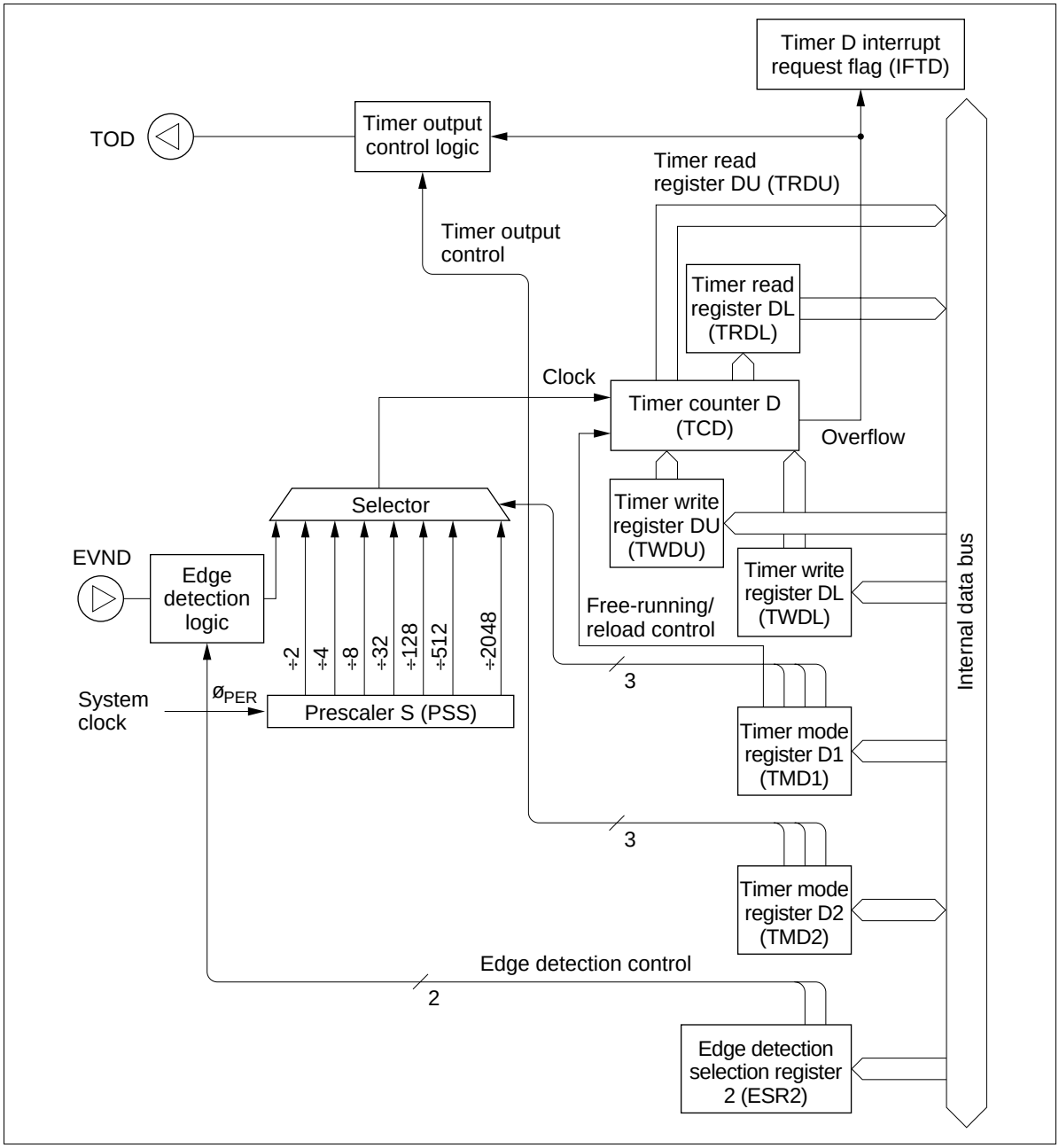


Figure 40-1 Block Diagram of Timer D (Free-Running/Reload Timer)

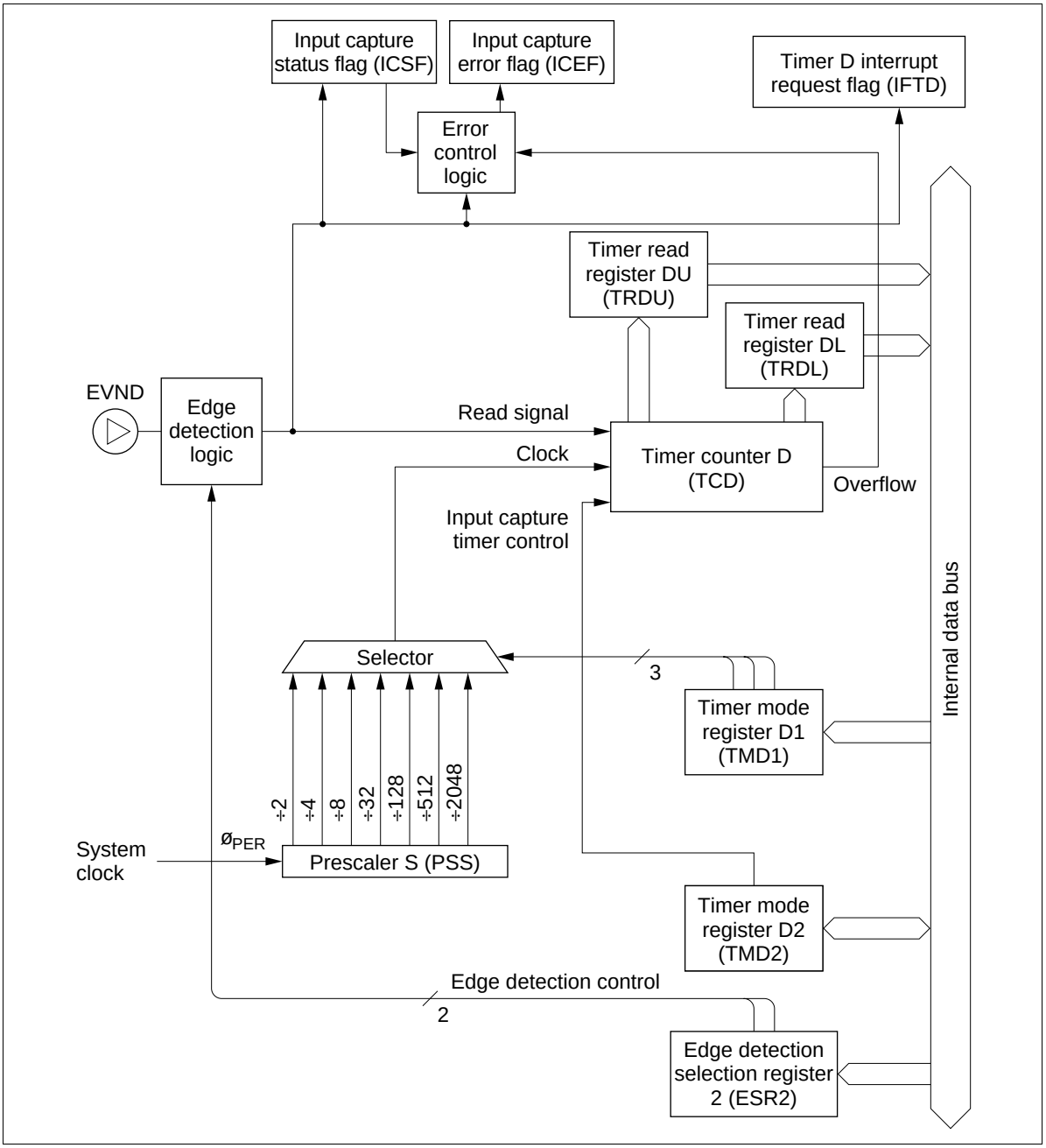


Figure 40-2 Block Diagram of Timer D (in Input Capture Timer Mode)

Registers for Timer D Operation: By using the following registers, timer D operation modes are selected and the timer D count is read and written.

Timer mode register D1 (TMD1: $010)

Timer mode register D2 (TMD2: $015)

Timer write register D (TWDL: $011, TWDU: $012)

Timer read register D (TRDL: $011, TRDU: $012)

Port mode register C (PMRC: $025)

Detection edge select register 2 (ESR2: $027)

- Timer mode register D1 (TMD1: $010): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 41. It is reset to $0 by MCU reset.

  Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register D1 (TMD1: $010) write instruction. Setting timer D's initialization by writing to timer write register D (TWDL: $011, TWDU: $012) must be done after a mode change becomes valid.

  When selecting the input capture timer operation, select the internal clock as the input clock source.

Timer mode register D1 (TMD1: $010)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMD13	TMD12	TMD11	TMD10

TMD13	Free-running/reload timer selection
0	Free-running timer
1	Reload timer

TMD12	TMD11	TMD10	Input clock period and input clock source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$R4_0$/EVND (external event input)

Figure 41 Timer Mode Register D1 (TMD1)

- Timer mode register D2 (TMD2: $015): Four-bit read/write register that selects the timer D output mode and input capture operation as shown in figure 42. It is reset to $0 by MCU reset.

Timer mode register D2 (TMD2: $015)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W
Bit name	TMD23	TMD22	TMD21	TMD20

TMD23	TMD22	TMD21	TMD20	$R3_2$/TOD mode selection	
0	0	0	0	$R3_2$	$R3_2$ port
			1	TOD	Toggle output
		1	0	TOD	0 output
			1	TOD	1 output
	1	0	0	—	Inhibited
			1		
		1	0		
			1	TOD	PWM output
1	×	×	×	$R3_2$	Input capture ($R3_2$ port)

×: Don't care

Figure 42 Timer Mode Register D2 (TMD2)

- Timer write register D (TWDL: $011, TWDU: $012): Write-only register consisting of a lower digit (TWDL) and an upper digit (TWDU) as shown in figures 43 and 44. The operation of timer write register D is basically the same as that of timer write register C (TWCL: $00E, TWCU: $00F).

Timer write register D (lower digit) (TWDL: $011)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWDL3	TWDL2	TWDL1	TWDL0

Figure 43 Timer Write Register D Lower Digit (TWDL)

Timer write register D (upper digit) (TWDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWDU3	TWDU2	TWDU1	TWDU0

Figure 44 Timer Write Register D Upper Digit (TWDU)

- Timer read register D (TRDL: $011, TRDU: $012): Read-only register consisting of a lower digit (TRDL) and an upper digit (TRDU) as shown in figures 45 and 46. The operation of timer read register D is basically the same as that of timer read register C (TRCL: $00E, TRCU: $00F).

  When the input capture timer operation is selected and if the count of timer D is read after a trigger is input, either the lower or upper digit can be read first.

Timer read register D (lower digit) (TRDL: $011)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDL3	TRDL2	TRDL1	TRDL0

Figure 45 Timer Read Register D Lower Digit (TRDL)

Timer read register D (upper digit) (TRDU: $012)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRDU3	TRDU2	TRDU1	TRDU0

Figure 46 Timer Read Register D Upper Digit (TRDU)

- Port mode register C (PMRC: $025): Write-only register that selects $R4_0$/EVND pin function as shown in figure 47. It is reset to $0 by MCU reset.

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	0	0	0	—
Read/Write	W	W	W	—
Bit name	PMRC3	PMRC2	PMRC1	Not used

PMRC1	$R4_0$/EVND mode selection
0	$R4_0$
1	EVND

PMRC2	D_{12}/$\overline{STOPC}$ mode selection
0	D_{12}
1	$\overline{STOPC}$

PMRC3	D_{13}/$\overline{INT_0}$ mode selection
0	D_{13}
1	$\overline{INT_0}$

Figure 47 Port Mode Register C (PMRC)

- Detection edge select register 2 (ESR2: $027): Write-only register that selects the detection edge of signals input to pin EVND as shown in figure 48. It is reset to $0 by MCU reset.

Detection edge register 2 (ESR2: $027)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	ESR23	ESR22	Not used	Not used

ESR23	ESR22	EVND detection edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection*

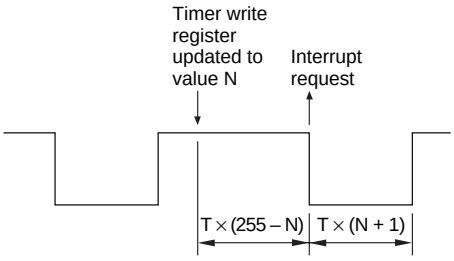
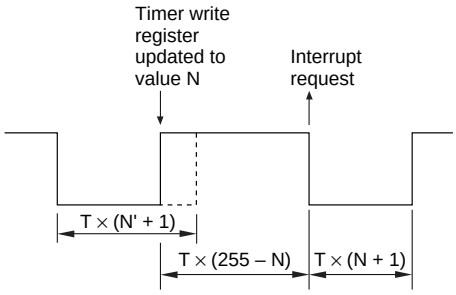
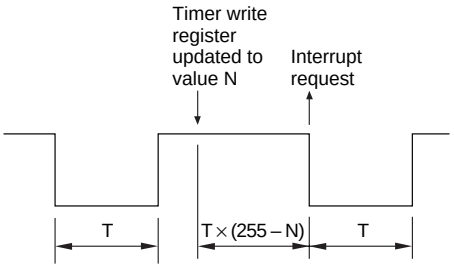
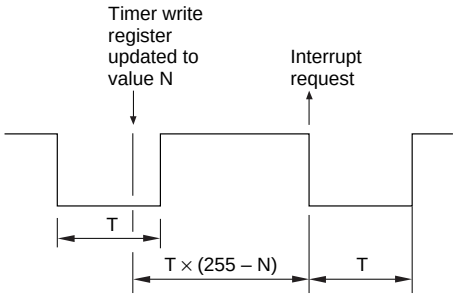
Note: *Both falling and rising edges are detected.

Figure 48 Detection Edge Select Register 2 (ESR2)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 24. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 24 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Write Register is Updated during High PWM Output**	**Timer Write Register is Updated during Low PWM Output**
Free running		
Reload		

Serial Interface 1

The MCU has one channel of serial interface. The serial interface serially transfers or receives 8-bit data, and includes the following features.

- Multiple transmit clock sources
  - External clock
  - Internal prescaler output clock
  - System clock
- Output level control in idle states

Serial interface 1

- Serial data register 1 (SR1L: $006, SR1U: $007)
- Serial mode register 1A (SM1A: $005)
- Serial mode register 1B (SM1B: $028)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)
- Octal counter (OC)
- Selector

The block diagram of serial interface 1 is shown in figure 49.

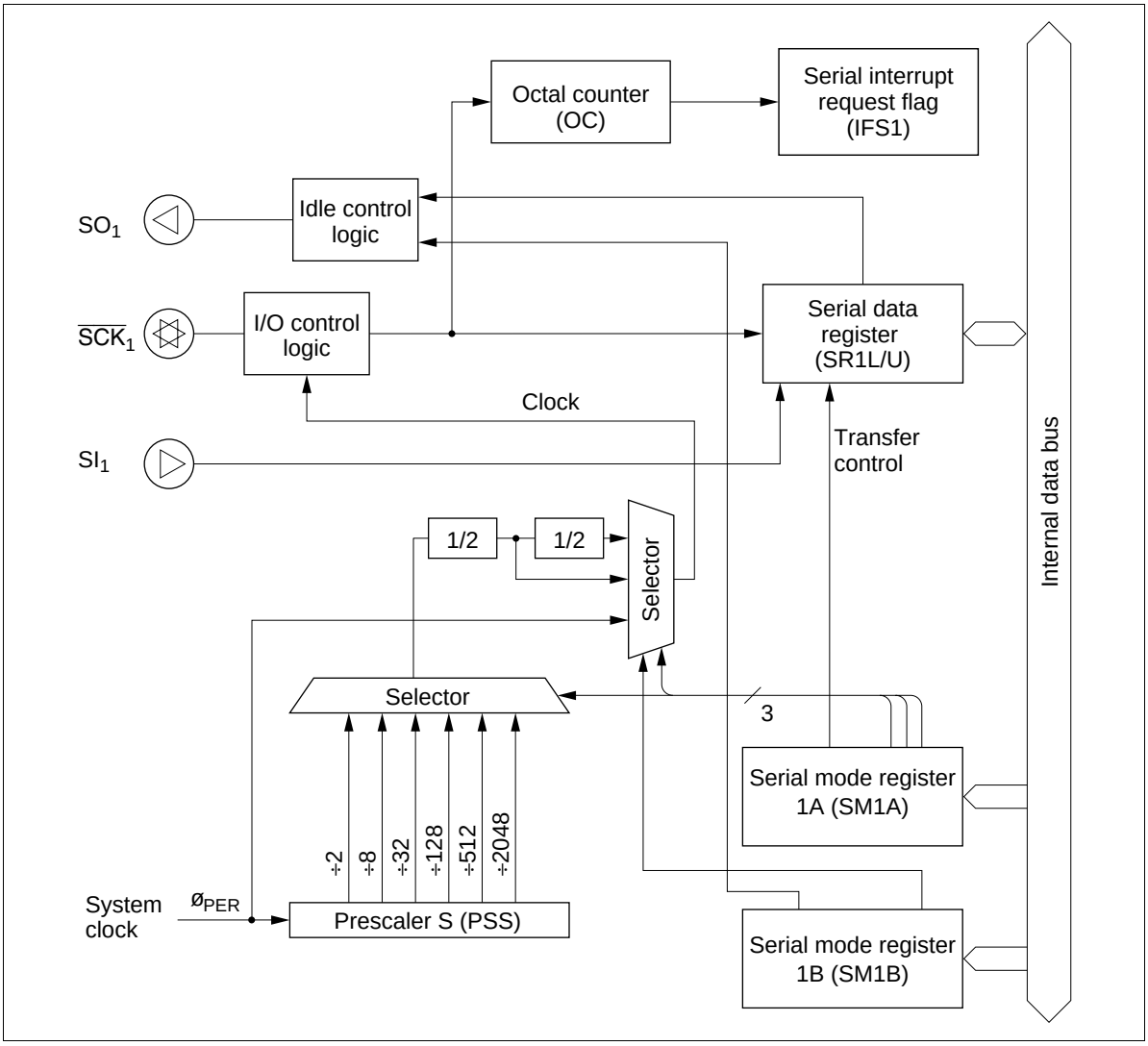


Figure 49 Block Diagram of Serial Interface 1

Serial Interface Operation

Selecting and Changing the Operating Mode: Table 25 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: $004), and serial mode register 1A (SM1A: $005) settings; to change the operating mode of serial interface 1, always initialize the serial interface internally by writing data to serial mode register 1A. Note that serial interface 1 is initialized by writing data to serial mode register 1A. Refer to the following section Registers for Serial Interface for details.

Pin Setting: The $R4_1/\overline{SCK}_1$ pin is controlled by writing data to serial mode register 1A (SM1A: $005). Pins $R4_2/SI_1$ and $R4_3/SO_1$ are controlled by writing data to port mode register A (PMRA: $004). Refer to the following section Registers for Serial Interface for details.

Transmit Clock Source Setting: The transmit clock source of serial interface 1 is set by writing data to serial mode register 1A (SM1A: $005) and serial mode register 1B (SM1B: $028). Refer to the following section Registers for Serial Interface for details.

Data Setting: Transmit data of serial interface 1 is set by writing data to serial data register 1 (SR1L: $006, SR1U: $007). Receive data of serial interface 1 is obtained by reading the contents of serial data register 1. The serial data is shifted by the transmit clock and is input from or output to an external system.

The output level of the SO_1 pin is invalid until the first data is output after MCU reset, or until the output level control in idle states is performed.

Transfer Control: Serial interface 1 is activated by the STS instruction. The octal counter is reset to 000 by the STS instruction, and it increments at the rising edge of the transmit clock for serial interface. When the eighth transmit clock signal is input or when serial transmission/reception is discontinued, the octal counter is reset to 000, the serial 1 interrupt request flag (IFS1: $003, bit 2) for serial interface 1 is set, and the transfer stops.

When the prescaler output is selected as the transmit clock of serial interface 1, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 0 to 2 (SM1A0–SM1A2) of serial mode register 1A (SM1A: $005) and bit 0 (SM1B0) of serial mode register 1B (SM1B: $028) as listed in table 26.

Table 25 Serial Interface 1 Operating Modes

SM1A	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

Table 26 Serial Transmit Clock (prescaler output)

SM1B	SM1A				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Tranamit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

Operating States: Serial interface 1 has the following operating states; transitions between them are shown in figure 50.

- STS wait state
- Transmit clock wait state
- Transfer state
- Continuous transmit clock output state (only in internal clock mode)

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 50). In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), serial interface 1 enters transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state is between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts serial data register 1 (SR1L: $006, SR1U: $007), and enters the serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  The serial interface enters STS wait state by writing data to serial mode register 1A (SM1A: $005) (04, 14) in transmit clock wait state.

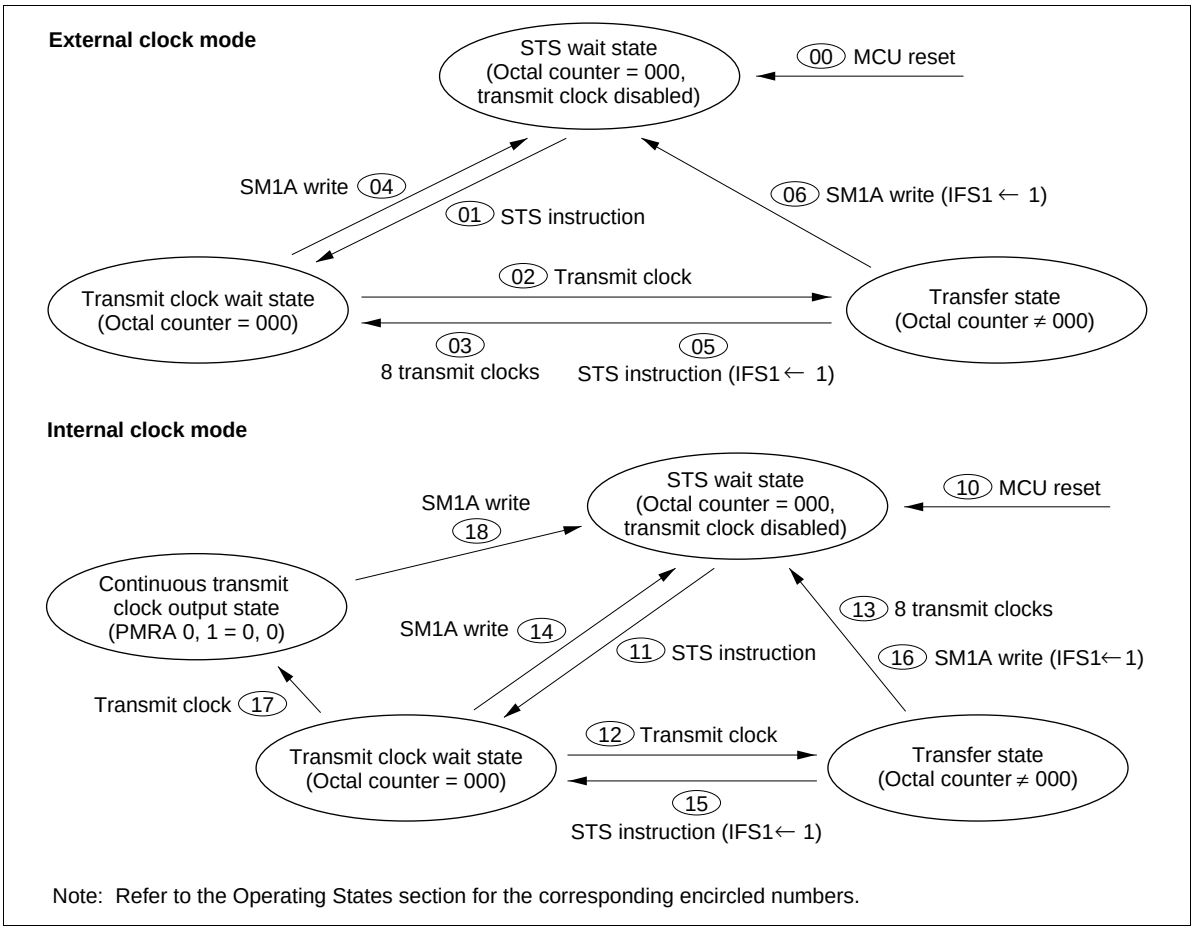
- Transfer state: Transfer state is between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

In transfer state, writing data to serial mode register 1A (SM1A: $005) (06, 16) initializes serial interface 1, and STS wait state is entered.

If the state changes from transfer to another state, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the $\overline{SCK}_1$ pin.

  When bits 0 and 1 (PMRA0, PMRA1) of port mode register A (PMRA: $004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If serial mode register 1A (SM1A: $005) is written to in continuous clock output mode (18), STS wait state is entered.



Note: Refer to the Operating States section for the corresponding encircled numbers.

Figure 50 Serial Interface State Transitions

Output Level Control in Idle States: When serial interface 1 is in STS instruction wait state, the output of serial output pin, SO_1 can be controlled by setting bit 1 (SM1B1) of serial mode register 1B (SM1B: $028) to 0 or 1. The output level control example of serial interface 1 is shown in Figure 51. Note that the output level cannot be controlled in transfer state.

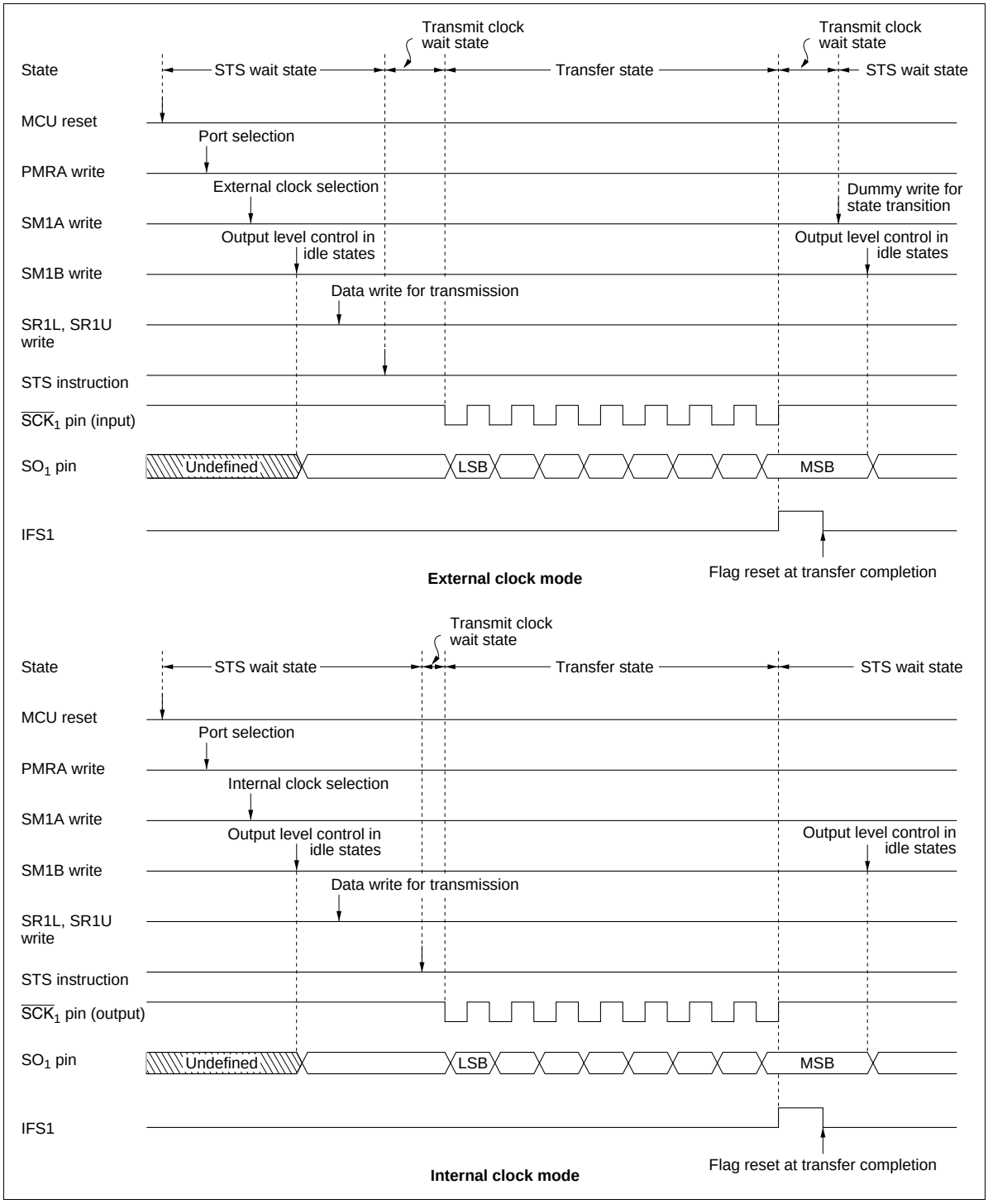


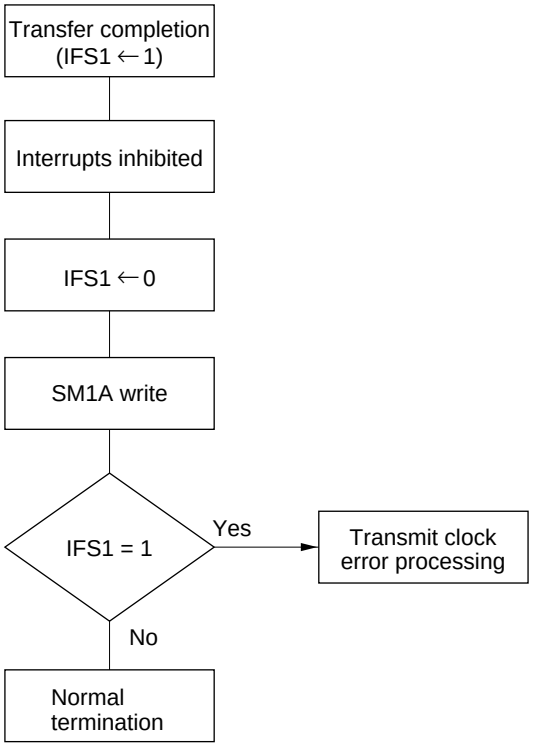
Figure 51 Example of Serial Interface 1 Operation Sequence

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 52.

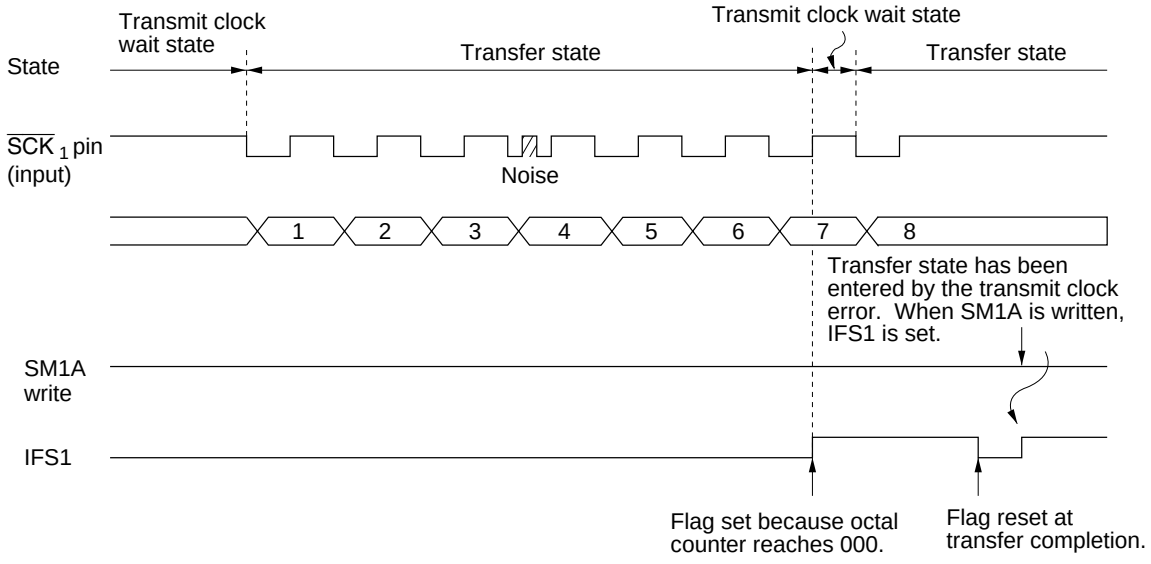
If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer is completed and IFS is reset, writing to serial mode register 1A (SM1A: $005) changes the state from transfer to STS wait. At this time serial interface 1 is in the transfer state, and the serial 1 interrupt request flag is set again, and therefore the error can be detected.

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: $004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to serial mode register 1A (SM1A: $005) again.
- Serial 1 interrupt request flag (IFS1: $003, bit 2) set: For serial interface 1, if the state is changed from transfer state to another by writing to serial mode register 1A (SM1A: $005) or executing the STS instruction during the first low pulse of the transmit clock, the serial 1 interrupt request flag is not set. To set the serial 1 interrupt request flag, a serial mode register 1A write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}_1$ pin is at 1, that is, after executing the input instruction to port R4.



Transmit clock error detection flowchart



Transmit clock error detection procedures

Figure 52 Transmit Clock Error Detection

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

- Serial mode register 1A (SM1A: $005)
- Serial mode register 1B (SM1B: $028)
- Serial data register 1 (SR1L: $006, SR1U: $007)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)

Serial Mode Register 1A (SM1A: $005): This register has the following functions (figure 53).

- $R4_1/\overline{SCK}_1$ pin function selection
- Serial interface 1 transmit clock selection
- Serial interface 1 prescaler division ratio selection
- Serial interface 1 initialization

Serial mode register 1A (SM1A: $005) is a 4-bit write-only register. It is reset to $0 by MCU reset.

A write signal input to serial mode register 1A (SM1A: $005) discontinues the input of the transmit clock to serial data register 1 (SR1L: $006, SR1U: $007) and the octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial 1 interrupt request flag (IFS1: $003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register 1A (SM1A: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SM1A3	SM1A2	SM1A1	SM1A0

SM1A3	$R4_1/\overline{SCK}_1$ mode selection
0	$R4_1$
1	$\overline{SCK}_1$

SM1A2	SM1A1	SM1A0	$\overline{SCK}_1$	Clock source	Prescaler division ratio
0	0	0	Output	Prescaler	Refer to table 26
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

Figure 53 Serial Mode Register 1A (SM1A)

Serial Mode Register 1B (SM1B: $028): This register has the following functions (figure 54).

- Serial interface 1 prescaler division ratio selection
- Serial interface 1 output level control in idle states

Serial mode register 1B (SM1B: $028) is a 2-bit write-only register. It cannot be written during data transfer.

By setting bit 0 (SM1B0) of this register, the serial interface 1 prescaler division ratio is selected. Only bit 0 (SM1B0) can be reset to 0 by MCU reset. By setting bit 1 (SM1B1), the output level of the SO_1 pin is controlled in idle states of serial interface 1. The output level changes at the same time that SM1B1 is written to.

Serial mode register 1B (SM1B: $028)

Bit	3	2	1	0
Initial value	—	—	Undefined	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	SM1B1	SM1B0

SM1B1	Output level control in idle states
0	Low level
1	High level

SM1B0	Serial clock division ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

Figure 54 Serial Mode Register 1B (SM1B)

Serial Data Register 1 (SR1L: $006, SR1U: $007): This register has the following functions (figures 55 and 56)

- Serial interface 1 transmission data write and shift
- Serial interface 1 receive data shift and read

Writing data in this register is output from the SO_1 pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI_1 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 57.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

Serial data register 1(lower digit) (SR1L: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR13	SR12	SR11	SR10

Figure 55 Serial Data Register 1 (SR1L)

Serial data register 1(upper digit) (SR1U: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR17	SR16	SR15	SR14

Figure 56 Serial Data Register 1 (SR1U)

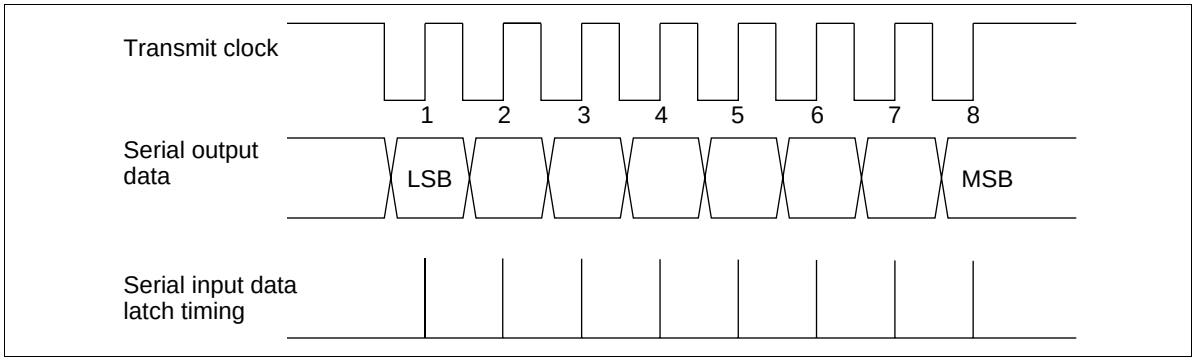


Figure 57 Serial Interface Output Timing

Port Mode Register A (PMRA: $004): This register has the following functions (figure 58).

- $R4_2/SI_1$ pin function selection
- $R4_3/SO_1$ pin function selection

Port mode register A (PMRA: $004) is a 2-bit write-only register, and is reset to $0 by MCU reset.

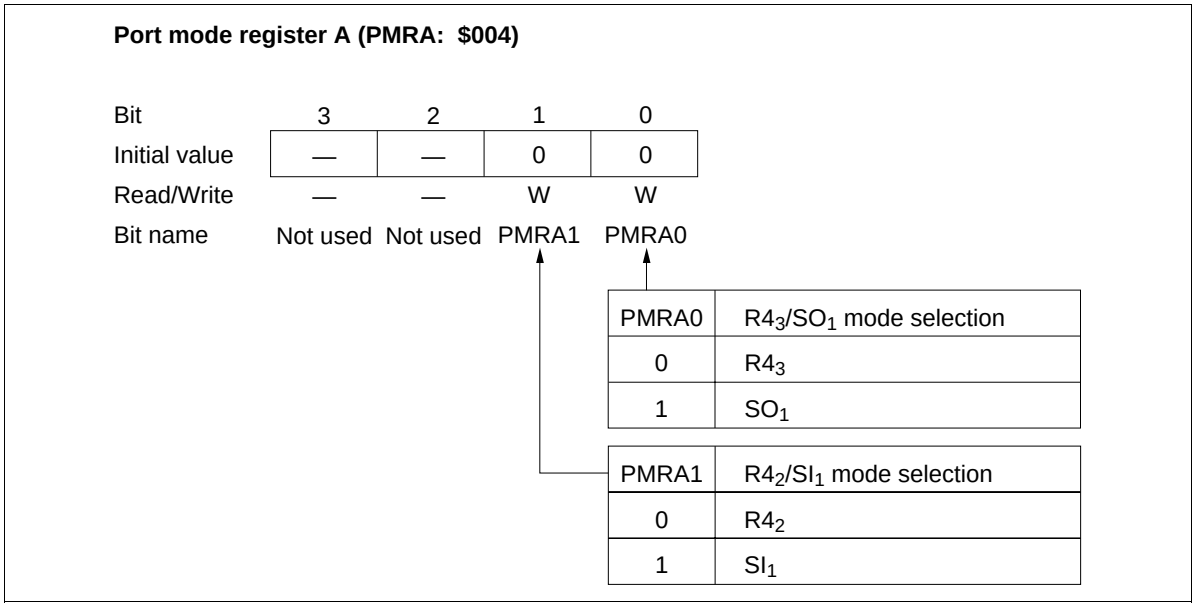


Figure 58 Port Mode Register A (PMRA)

Miscellaneous Register (MIS: $00C): This register has the following functions (figure 59).

- $R4_3/SO_1$ pin PMOS control

Miscellaneous register (MIS: $00C) is a 2-bit write-only register and is reset to $0 by MCU reset.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

MIS2	$R4_3/SO_1$ PMOS on/off selection
0	On
1	Off

MIS3	Pull-up MOS on/off selection
0	Off
1	On

Figure 59 Miscellaneous Register (MIS)

Comparator

The block diagram of the comparator is shown in figure 60. The comparator compares input voltage with the reference voltage.

Setting 1 to bit 3 (CER3) of the compare enable register (CER: $018) executes a voltage comparison. When an input voltage at $COMP_0$, $COMP_1$ is higher than the reference voltage, the TM or TMD command sets the status flag (ST) high for the corresponding bits of the compare data register (CDR: $017) to $COMP_0$ and $COMP_1$. On the other hand, when an input voltage at $COMP_0$, $COMP_1$ is lower, the TM or TMD command clears the ST to 0.

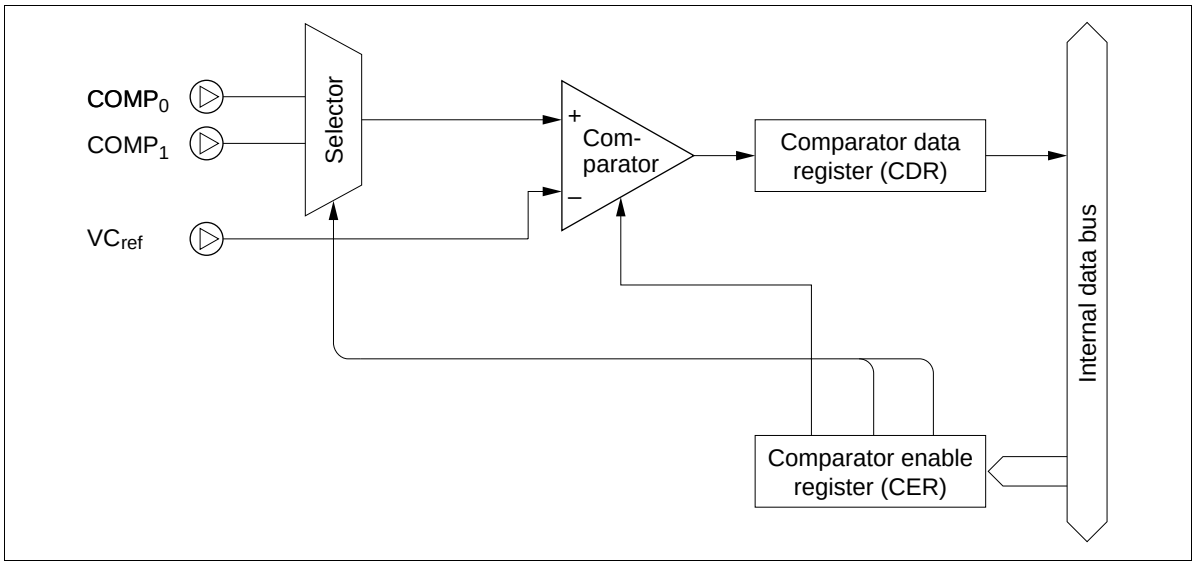


Figure 60 Block Diagram of Comparator

Compare Enable Register (CER: $018): Three-bit write-only register which enables comparator operation, and selects the reference voltage and the analog input pin (figure 61).

Compare enable register (CER: $018)

Bit	3	2	1	0
Initial value	0	—	0	0
Read/Write	W	—	W	W
Bit name	CER3	Not used	CER1	CER0

CER3	Digital/Analog selection
0	Digital input mode: $RD_0/COMP_0$, $RD_1/COMP_1$ operate as R port
1	Analog input mode: $RD_0/COMP_0$, $RD_1/COMP_1$ operate as analog input

CER1	CER0	Analog input pin selection
0	0	$COMP_0$
	1	$COMP_1$
1	0	Not used
	1	Not used

Figure 61 Compare Enable Register

Compare Data Register (CDR: $017): Two-bit read-only register which latches the result of the comparison between the analog input pins and the reference voltage. Bits 0 and 1 corresponds the results of comparison with $COMP_0$ and $COMP_1$, respectively. This register can be read only by the TM or TMD command. Only bit CER3 corresponds to the analog input pin which the input pin selection is made through pins CER0 and CER1. After a compare operation, the data in this register is not retained (figure 62).

Compare data register (CDR: $017)

Bit	3	2	1	0
Initial value	—	—	Undefined	Undefined
Read/Write	—	—	R	R
Bit name	Not used	Not used	CDR1	CDR0

Result of $COMP_0$ comparison

Result of $COMP_1$ comparison

Figure 62 Compare Data Register

Note on Use: During the compare operation pins $RD_0/COMP_0$ and $RD_1/COMP_1$ operate as analog inputs and cannot operate as R ports.

The comparator can operate in active mode but is disabled in other modes.

RE_0/VC_{ref} cannot operate as an R port when the external input voltage is selected as the reference.

Programmable ROM (HD4074054, HD4074094)

The HD4074054 and HD4074094 are ZTAT™ microcomputers with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin No.		MCU Mode		PROM Mode	
DP-42S	FP-44A	Pin Name	I/O	Pin Name	I/O
1	39	$RD_0/COMP_0$	I	$\overline{CE}$	I
2	40	$RD_1/COMP_1$	I	$\overline{OE}$	I
3	41	RD_2	I		
4	42	RD_3	I		
5	43	RC_0	I		
6	1	RE_0/VC_{ref}	I	$\overline{M}_1$	I
7	2	$\overline{TEST}$	I	$\overline{TEST}$	I
8	3	OSC_1	I	V_{CC}	
9	4	OSC_2	O		
10	5	$\overline{RESET}$	I	$\overline{RESET}$	I
11	6	GND	I	GND	
12	7	D_0	I/O		O
13	8	D_1	I/O		O
14	9	D_2	I/O	V_{CC}	
15	10	D_3	I/O	V_{CC}	
16	11	D_4	I/O*	O_4	I/O
17	12	D_5	I/O*	O_5	I/O
18	13	D_6	I/O*	O_6	I/O
19	14	D_7	I/O*	O_7	I/O
20	15	D_8	I/O	A_{13}	I
21	16	D_9	I/O	A_{14}	I
22	17	$D_{12}/\overline{STOPC}$	I	A_9	I
23	18	$D_{13}/\overline{INT}_0$	I	V_{PP}	
24	19	$R0_0/\overline{INT}_1$	I/O	$\overline{M}_0$	I
25	20	$R1_0$	I/O	A_5	I
26	21	$R1_1$	I/O	A_6	I
27	23	$R1_2$	I/O	A_7	I

Note: I/O: Input/output pin, I: Input pin, O: Output pin
* HD404054 Series: I/O, HD404094 Series: O

Pin No.		MCU Mode		PROM Mode	
DP-42S	**FP-44A**	**Pin Name**	**I/O**	**Pin Name**	**I/O**
28	24	$R1_3$	I/O	A_8	I
29	25	$R2_0$	I/O	A_0	I
30	26	$R2_1$	I/O	A_{10}	I
31	27	$R2_2$	I/O	A_{11}	I
32	28	$R2_3$	I/O	A_{12}	I
33	29	$R3_0$	I/O	A_1	I
34	30	$R3_1$/TOC	I/O	A_2	I
35	31	$R3_2$/TOD	I/O	A_3	I
36	32	$R3_3$	I/O	A_4	I
37	33	$R4_0$/EVND	I/O	O_0	I/O
38	34	$R4_1/\overline{SCK}_1$	I/O	O_1	I/O
39	35	$R4_2/SI_1$	I/O	O_2	I/O
40	36	$R4_3/SO_1$	I/O	O_3	I/O
41	37	SEL	I		
42	38	V_{CC}	I	V_{CC}	
–	22	NC	–		
–	44	NC	–		

Note: I/O: Input/output pin, I: Input pin, O: Output pin

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode. PROM mode is set by pulling $\overline{TEST}$, $\overline{M}_0$, and $\overline{M}_1$ low, and $\overline{RESET}$ low as shown in figure 63. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256-type EPROM using a standard PROM programmer and an 42-to-28-pin socket adapter. Recommended PROM programmers and socket adapters of the HD4074054 and HD4074094 are listed in table 27.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable the use of a general-purpose PROM programmer. This circuit splits each instruction into five lower bits and five upper bits that are read from or written to consecutive addresses. This means that if, for example, 4-kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 8-kbyte address space ($0000–$7FFF) must be specified.

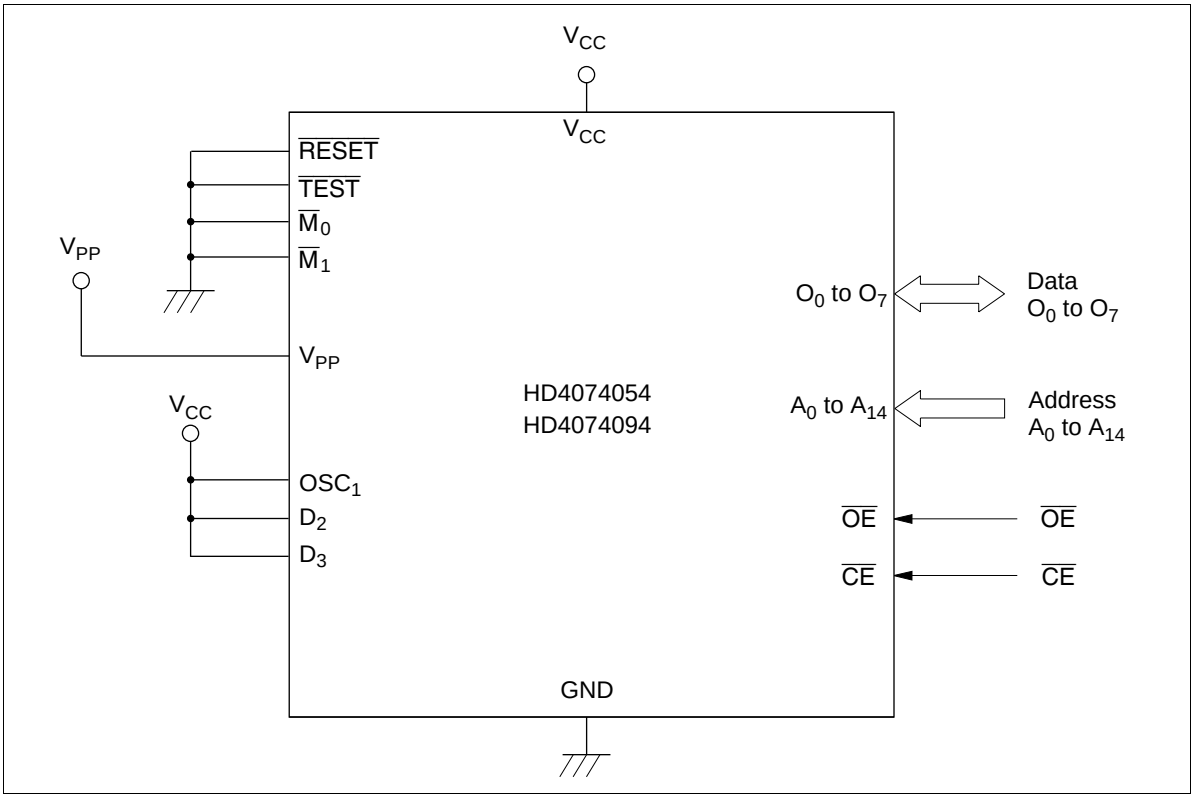


Figure 63 PROM Mode Connections

Table 27 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Model Name**	**Manufacturer**
DATA I/O Corp.	121B	DP-42S	HS4654ESS01H	Hitachi
AVAL Corp.	PKW-1000	FP-44A	HS4654ESH01H	Hitachi

Warnings

1. Always specify addresses $0000 to $1FFF when programming with a PROM programmer. If address $2000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased or reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltages (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel 27256 setting.

Programming and Verification

The built-in PROM of the MCU can be programmed at high speed without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as listed in table 28.

Table 28 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_7**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 64 and described below.

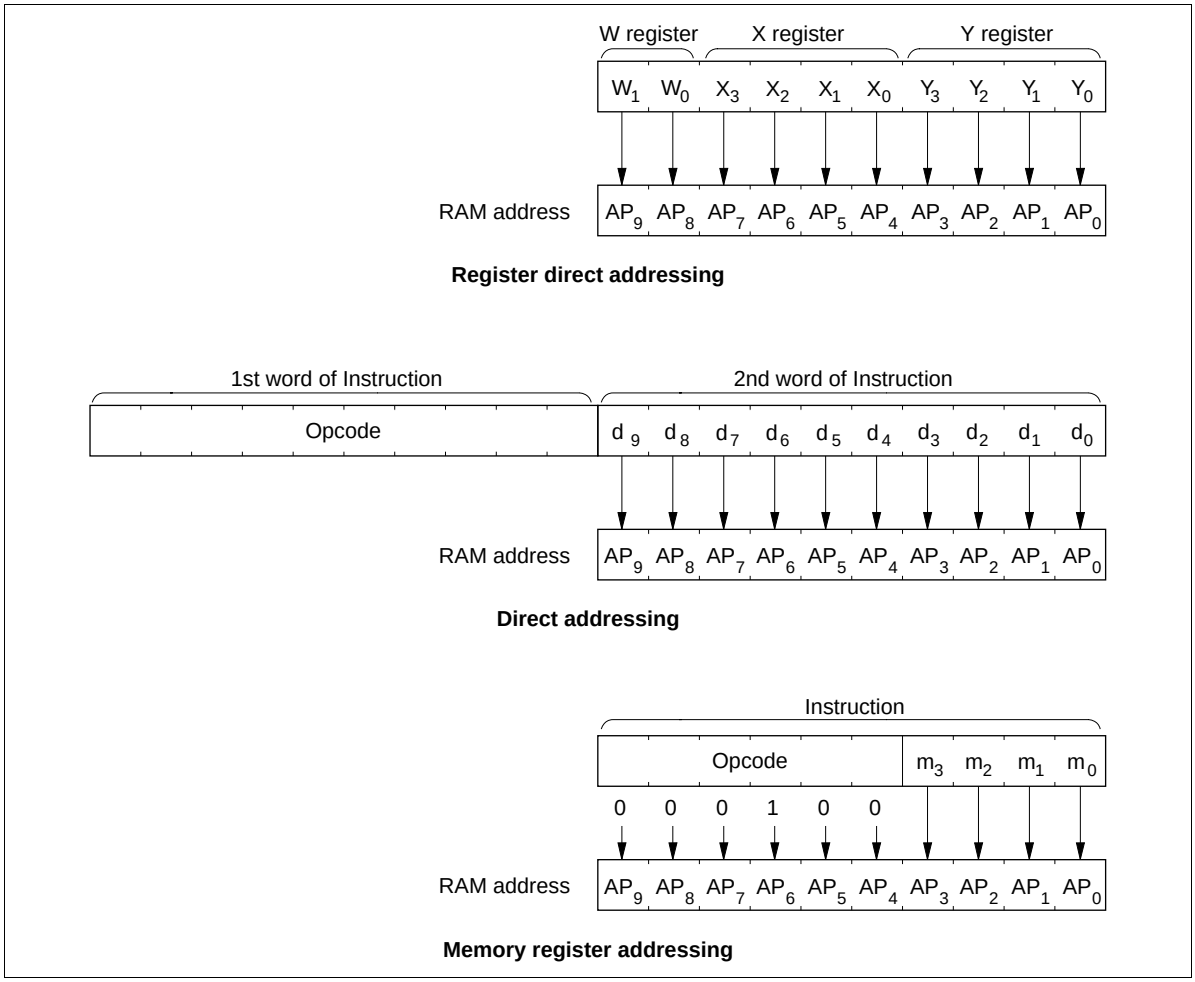


Figure 64 RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from $040 to $04F, are accessed with the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 65 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 67. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $0000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 66. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

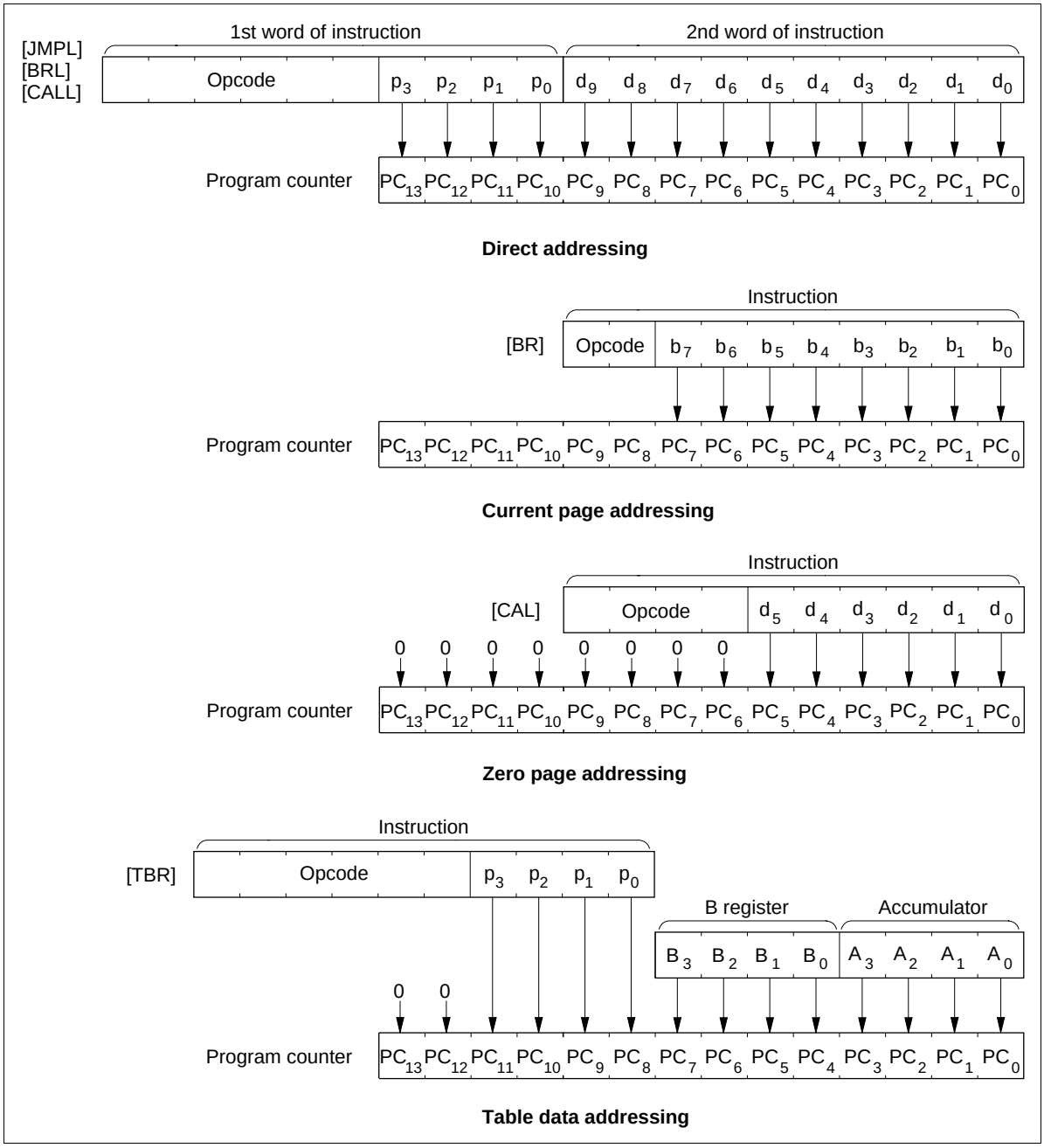


Figure 65 ROM Addressing Modes

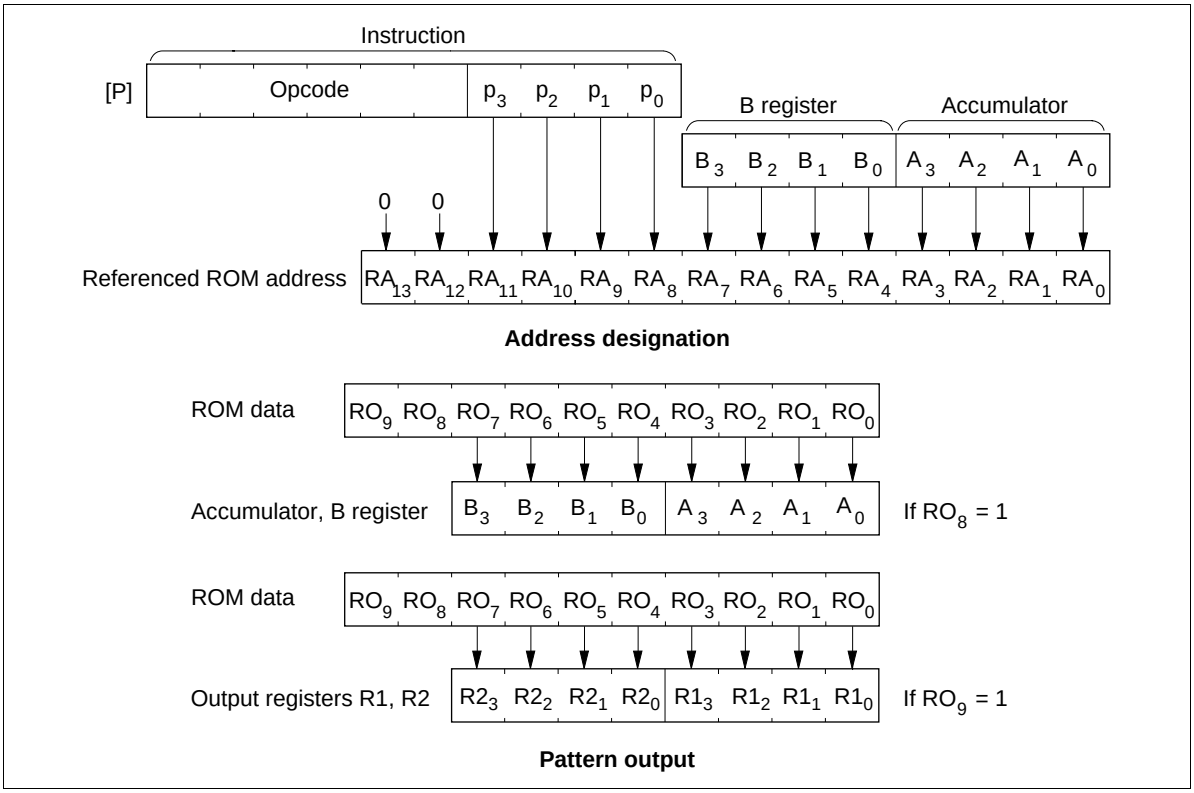


Figure 66 P Instruction

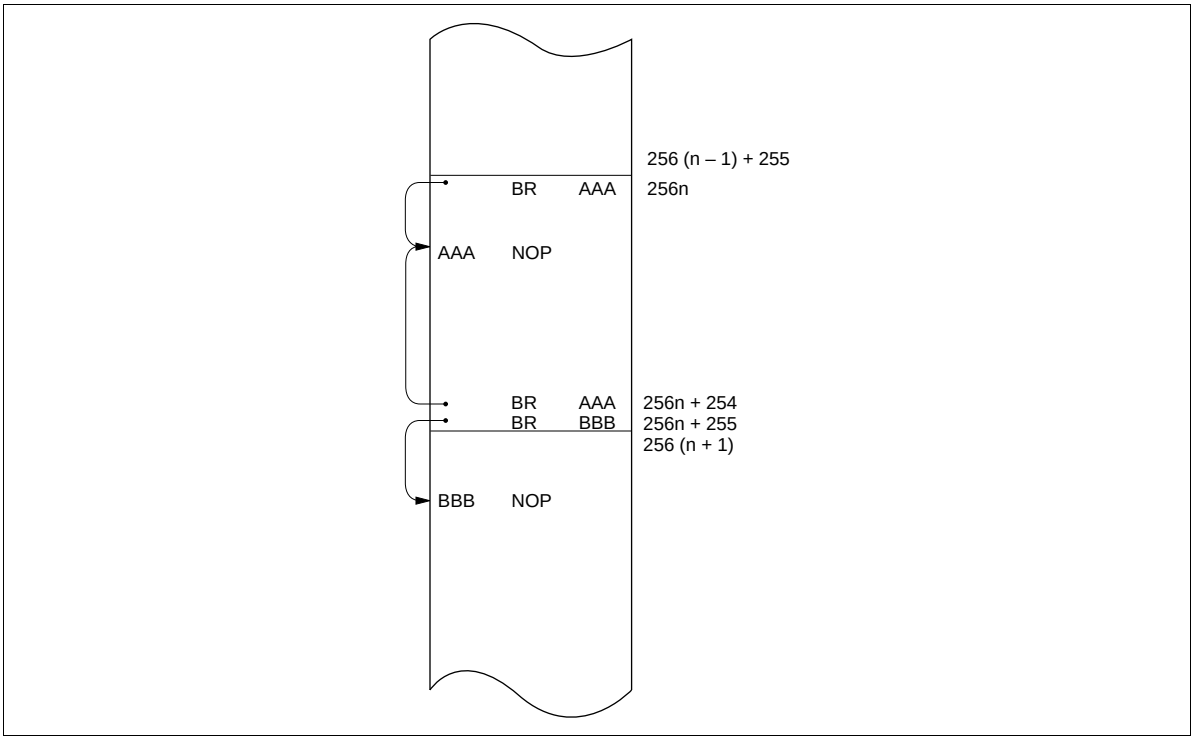


Figure 67 Branching when the Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	
		–0.3 to +15.0	V	2
Total permissible input current	$\sum I_o$	80	mA	3
Total permissible output current	$-\sum I_o$	50	mA	4
Maximum input current	I_o	4	mA	5, 6
		30	mA	5, 7
Maximum output current	$-I_o$	4	mA	8, 9
		20	mA	8, 10
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to D_{13} (V_{PP}) of HD4074054 and HD4074094.
2. Applies to D_4 to D_7 of HD404092, HD404094, and HD4074094.
3. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
4. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
5. The maximum input current is the maximum current flowing from each I/O pin to GND.
6. Applies to D_0–D_3, and R0–R4.
7. Applies to D_4–D_9.
8. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.
9. Applies to D_4–D_9 and R0–R4.
10. Applies to D_0–D_3.

Electrical Characteristics

DC Characteristics (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20 °C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK_1}$, SI_1, EVND	0.9 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3	—	V_{CC} + 0.3	V	External clock	
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK_1}$, SI_1, EVND	–0.3	—	0.10 V_{CC}	V		
		OSC_1	–0.3	—	0.3	V	External clock	
Output high voltage	V_{OH}	$\overline{SCK_1}$, SO_1, TOC,TOD	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK_1}$, SO_1, TOC,TOD	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	$\overline{RESET}$, $\overline{STOPC}$, $\overline{INT_0}$, $\overline{INT_1}$, $\overline{SCK_1}$, SI_1, SO_1, EVND, OSC_1, TOC, TOD	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC1}	V_{CC}	—	5	—	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Digital input mode	2, 4,
			—	5	10	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz Digital input mode	3, 4,
	I_{CC2}	V_{CC}	—	0.6	1.8	mA	V_{CC} = 3 V, f_{OSC} = 800 kHz Digital input mode	2, 4,
	I_{CMP1}	V_{CC}	—	9	—	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz Analog comp. mode	2, 4,
			—	9	15	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz Analog comp. mode	3, 4,
	I_{CMP2}	V_{CC}	—	3.1	4.3	mA	V_{CC} = 3 V, f_{OSC} = 800 kHz Analog comp. mode	2, 4,

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	1.2	—	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2, 6,
			—	3	6	mA	V_{CC} = 5 V, f_{OSC} = 8 MHz	3, 6,
	I_{SBY2}	V_{CC}	—	0.2	0.7	mA	V_{CC} = 3 V, f_{OSC} = 800 kHz	2, 6,
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	1	5	µA	V_{CC} = 3 V	2, 7
			—	1	10	µA	V_{CC} = 5 V	3, 7
Stop mode retaining voltage	V_{STOP}	V_{CC}	—	1.3	—	V		8
Comparator input reference voltage scope	VC_{ref}	VC_{ref}	0	—	V_{CC} – 1.2	V		

Notes:
1. Output buffer current is excluded.
2. Applies to HD404052, HD404054, HD4074054, HD404092, HD404094 and HD4074094.
3. Applies to HD40A4052 and HD40A4054.
4. I_{CC1} and I_{CC2} are the source currents when no I/O current is flowing while the MCU is in reset state. Test conditions: MCU: Reset
   Pins: $\overline{RESET}$ at GND (0 V to 0.3V)
   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
5. RD_0 and RD_1 pins are analog input mode when no I/O current is flowing.
   Test conditions: MCU: Analog input mode
   Pins: $RD_0/COMP_0$ at GND (0 V to 0.3 V)
   $RD_1/COMP_1$ at GND (0 V to 0.3 V)
   RE_0/VC_{ref} at GND (0 V to 0.3 V)
6. I_{SBY1} and I_{SBY2} are the source currents when no I/O current is flowing while the MCU timer is operating. Test conditions: MCU: I/O reset
   Serial interface stopped
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
7. These are the source currents when no I/O current is flowing.
   Test conditions: Pins: $\overline{RESET}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
   $\overline{TEST}$ at V_{CC} (V_{CC} – 0.3 to V_{CC})
   D_{13}* at V_{CC} (V_{CC} – 0.3 to V_{CC})
   Note: * Applies to HD4074054 and HD4074094
8. RAM data retention.

I/O Characteristics for Standard Pins (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_{12}–D_{13}, R0–RD, RE_0	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_{12}–D_{13}, R0–RD, RE_0	–0.3	—	0.3 V_{CC}	V		
Output high voltage	V_{OH}	R0–R4	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	R0–R4	—	—	0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\lvert I_{IL} \rvert$	D_{12}, R0–RD, RE_0	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		D_{13}	—	—	1	µA	V_{in} = 0 V to V_{CC}	1, 2, 4
			—	—	1	µA	V_{in} = V_{CC} – 0.3 V to V_{CC}	1, 3
			—	—	20	µA	V_{in} = 0 V to 0.3 V	1, 3
Pull-up MOS current	$–I_{PU}$	R0–R4	—	30	—	µA	V_{CC} = 3 V, V_{in} = 0 V	2, 3
			20	100	500	µA	V_{CC} = 5 V, V_{in} = 0 V	4
Input high voltage	V_{IHA}	$COMP_0$, $COMP_1$	—	VC_{ref}+0.05	—	V	Analog compare mode	5
Input low voltage	V_{ILA}	$COMP_0$, $COMP_1$	—	VC_{ref}–0.05	—	V	Analog compare mode	5

Notes: 1. Output buffer current is excluded.
2. Applies to HD404052, HD404054, HD404092, HD404094.
3. Applies to HD4074054, HD4074094.
4. Applies to HD40A4052, HD40A4054.
5. The analog input reference voltage should be in the range $0 \le VC_{ref} \le V_{CC}$–1.2.

I/O Characteristics for High-Current Pins and Intermediate-Voltage Pins (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s) HD404054 Series	Pin(s) HD404094 Series	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_0–D_9	D_0–D_3, D_8, D_9	0.7 V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_9	D_0–D_3, D_8, D_9	–0.3	—	0.3 V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_9	D_0–D_3, D_8, D_9	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
		D_0–D_3	D_0–D_3	2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 4.5 V to 6.0 V	2
		—	D_4–D_7	11.5	—	—	V	500 kΩ at 12 V	
Output low voltage	V_{OL}	D_0–D_9	D_0–D_9	—	—	0.4	V	I_{OL} = 0.4 mA	
		D_4–D_9	D_4–D_9	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 V to 6.0 V	2
I/O leakage current	$\lvert I_{IL} \rvert$	D_0–D_9	D_0–D_3, D_8, D_9	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		—	D_4–D_7	—	—	20	µA	V_{in} = 0 V to 12 V	1
Pull-down MOS current	I_{PD}	D_0–D_3	D_0–D_3	—	30	—	µA	V_{CC} = 3 V, V_{in} = 3 V	3
			—	20	100	500	µA	V_{CC} = 5 V, V_{in} = 5 V	4
Pull-up MOS current	$-I_{PU}$	D_4–D_9	D_8, D_9	—	30	—	µA	V_{CC} = 3 V, V_{in} = 0 V	3
			—	20	100	500	µA	V_{CC} = 5 V, V_{in} = 0 V	4

Notes: 1. Output buffer current is excluded.
2. When using HD4074054, HD4074094, V_{CC} = 4.5 V to 5.5 V.
3. Applies to HD404052, HD404054, HD4074054, HD404092, HD404094, HD4074094.
4. Applies to HD40A4052, HD40A4054.

AC Characteristics (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	—	4	MHz		1
			0.4	—	8.5	MHz		2
Instruction cycle time	t_{cyc}		—	8	—	µs	f_{OSC} = 4 MHz, ÷32	1, 4
			—	3.76	—	µs	f_{OSC} = 8.5 MHz, ÷32	2, 4
			—	1	—	µs	f_{OSC} = 4 MHz, ÷4	1, 3
			—	0.47	—	µs	f_{OSC} = 8.5 MHz, ÷4	2, 3
Oscillation stabilization time (ceramic)	t_{RC}	OSC_1, OSC_2	—	—	7.5	ms	V_{CC} = 2.7 V to 5.5 V: HD4074054, HD4074094	3, 4
							V_{CC} = 2.7 V to 6.0 V: HD404052, HD404054, HD404092, HD404094	
			—	—	60	ms	V_{CC} = 1.8 V to 2.7 V: HD404052, HD404054, HD404092, HD404094	
			—	—	7.5	ms	V_{CC} = 4.0 V to 6.0 V: HD40A4052,HD40A4054	5, 6
External clock high width	t_{CPH}	OSC_1	105	—	—	ns		1, 7
			49	—	—	ns		2, 7
External clock low width	t_{CPL}	OSC_1	105	—	—	ns		1, 7
			49	—	—	ns		2, 7
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		1, 7
			—	—	10	ns		2, 7
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		1, 7
			—	—	10	ns		2, 7
$\overline{INT_0}$, $\overline{INT_1}$, EVND high width	t_{IH}	$\overline{INT_0}$, $\overline{INT_1}$, EVND	2	—	—	t_{cyc}		8
$\overline{INT_0}$, $\overline{INT_1}$, EVND low width	t_{IL}	$\overline{INT_0}$, $\overline{INT_1}$, EVND	2	—	—	t_{cyc}		8
$\overline{RESET}$ low width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		9
$\overline{STOPC}$ low width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		10
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		9
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		10

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input capacitance	C_{in}	All pins except D_{13} D_4–D_7	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		D_4–D_7	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
		D13	—	—	15	pF	f = 1 MHz, V_{in} = 0 V: HD404052, HD404054, HD404092, HD404094, HD40A4052,HD40A4054	
			—	—	180	pF	f = 1 MHz, V_{in} = 0 V: HD4074054, HD4074094	
Analog comparator stabilization time	t_{CSTB}	$COMP_0$, $COMP_1$	—	—	2	t_{cyc}	V_{CC} = 2.7 V to 5.5 V: HD4074054, HD4074094	9
							V_{CC} = 2.7 V to 6.0 V: HD404052, HD404054, HD404092, HD404094	
			—	—	4	t_{cyc}	V_{CC} = 4.0 V to 6.0 V: HD40A4052,HD40A4054	11
			—	—	20	t_{cyc}	V_{CC} = 1.8 V to 2.7 V: HD404052, HD404054, HD404092, HD404094	

Notes:
1. Applies to HD404052, HD404054, HD4074054, HD404092, HD404094, HD4074094.
2. Applies to HD40A4052, HD40A4054.
3. SEL = 1
4. SEL = 0
5. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 2.7 (HD4074054, HD4074094)/1.8 (HD404052, HD404054, HD404092, HD404094) /4.0 (HD40A4052, HD40A4054)V at power-on, or after $\overline{\text{RESET}}$ input goes low or $\overline{\text{STOPC}}$ input goes low when stop mode is cancelled. At power-on or when stop mode is cancelled, $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ must be input for at least t_{RC} to ensure the oscillation stabilization time. If using a ceramic oscillator, contact its manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.
6. Applies to ceramic oscillator only.
7. Refer to figure 68.
8. Refer to figure 69.
9. Refer to figure 70.
10. Refer to figure 71.
11. Analog comparator stabilization time is the period for the analog comparator to stabilize and for correct data to be read after entering $RD_0/COMP_0$, $RD_1/COMP_1$ into analog input mode.

Serial Interface Timing Characteristics (HD404052, HD404054, HD404092, HD404094: V_{CC} = 1.8 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD40A4052, HD40A4054: V_{CC} = 4.0 V to 6.0 V, GND = 0 V, T_a = –20°C to +75°C; HD4074054, HD4074094: V_{CC} = 2.7 V to 5.5 V, GND = 0 V, T_a = –20°C to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$	1	—	—	t_{cyc}	Load shown in figure 73	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}	Load shown in figure 73	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}	Load shown in figure 73	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$	—	100	—	ns	Load shown in figure 73	1, 2
			—	—	80	ns		1, 3
Transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$	—	100	—	ns	Load shown in figure 73	1, 2
			—	—	80	ns		1, 3
Serial output data delay time	t_{DSO}	SO_1	—	—	500	ns	Load shown in figure 73	1, 2
			—	—	200	ns		1, 3
Serial input data setup time	t_{SSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3
Serial input data hold time	t_{HSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3

Note: 1. Refer to figure 72.
2. Applies to HD404052, HD404054, HD404092, HD404094, HD4074054, HD4074094.
3. Applies to HD40A4052, HD40A4054.

During Transmit Clock Input

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}_1$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$	—	100	—	ns		1, 2
			—	—	80	ns		1, 3
Transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$	—	100	—	ns		1, 2
			—	—	80	ns		1, 3
Serial output data delay time	t_{DSO}	SO_1	—	—	500	ns	Load shown in figure 73	1, 2
			—	—	200	ns		1, 3
Serial input data setup time	t_{SSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3
Serial input data hold time	t_{HSI}	SI_1	300	—	—	ns		1, 2
			150	—	—	ns		1, 3

Note: 1. Refer to figure72.
2. Applies to HD404052, HD404054, HD404092, HD404094, HD4074054, HD4074094.
3. Applies to HD40A4052, HD40A4054.

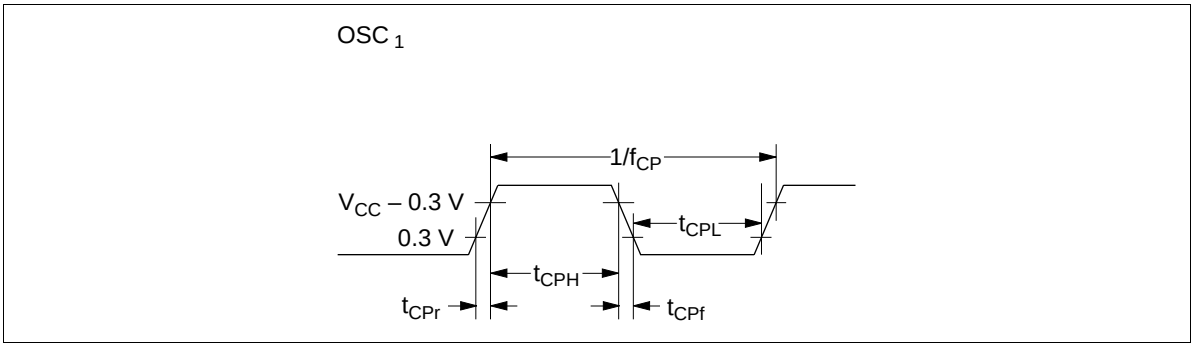


Figure 68 External Clock Timing

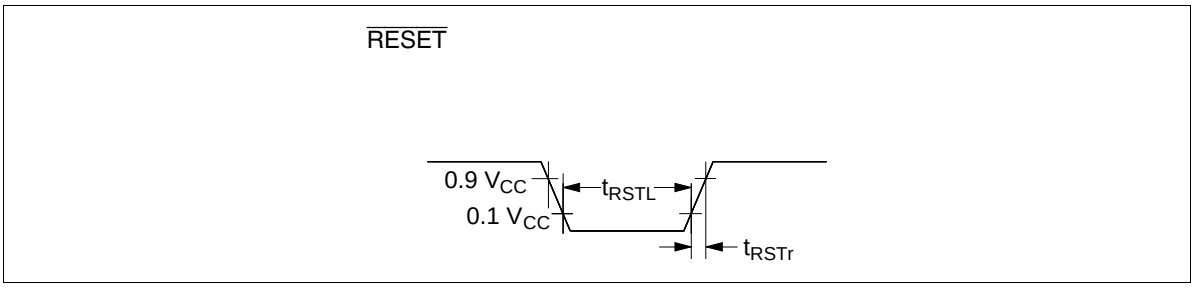


Figure 69 Interrupt Timing

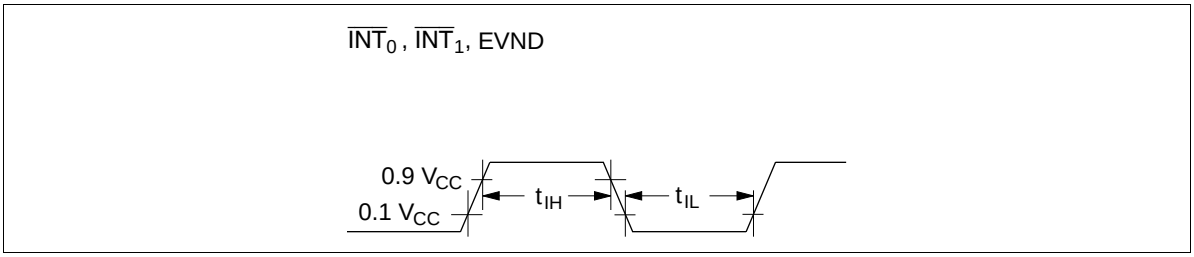


Figure 70 Reset Timing

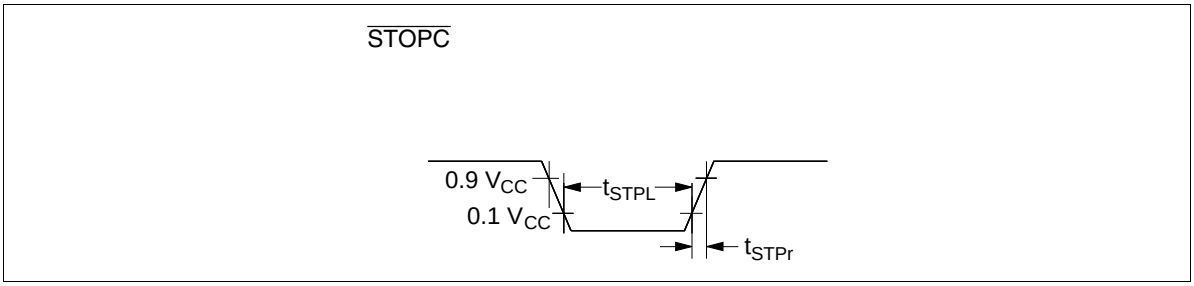
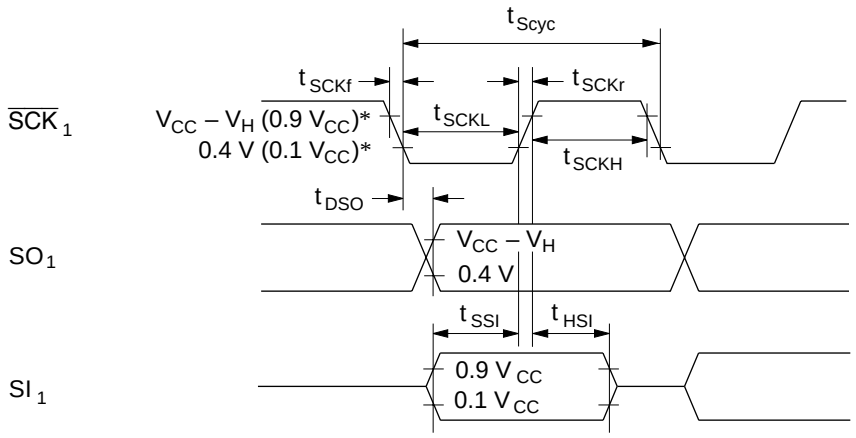


Figure 71 $\overline{\text{STOPC}}$ Timing



Note: * $V_{CC} - V_H$ and 0.4 V are the threshold voltages for transmit clock output.
V_H = 1.0 V : HD404052, HD404054, HD4074054, HD404092, HD404094, HD4074094
V_H = 2.0 V : HD40A4052, HD40A4054
0.9 V_{CC} and 0.1 V_{CC} are the threshold voltages for transmit clock output.

Figure 72 Serial Interface Timing

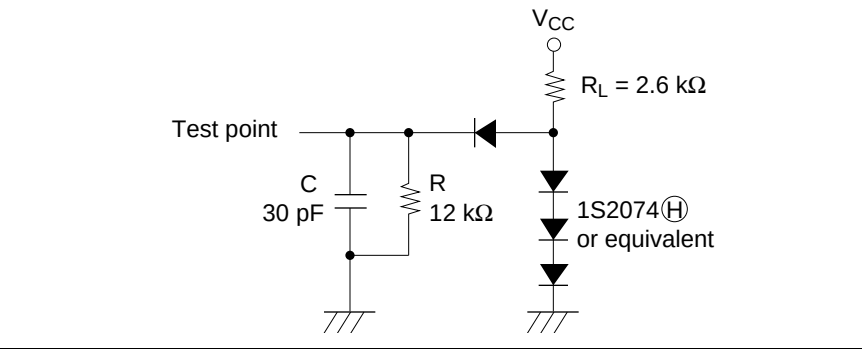


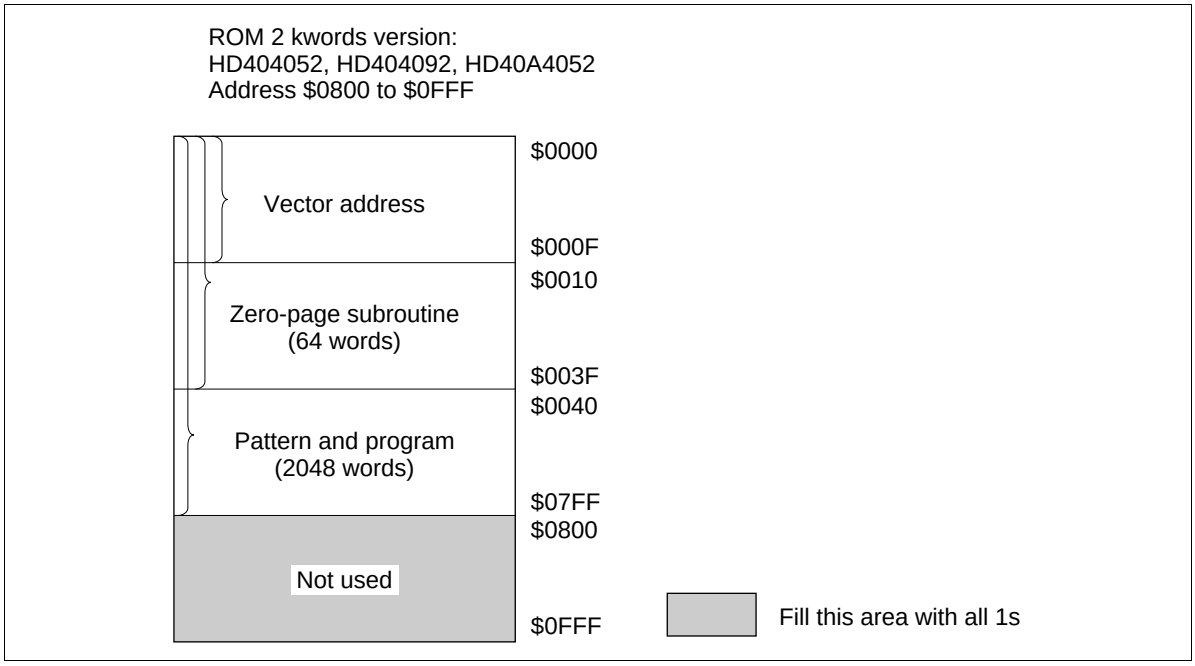
Figure 73 Timing Load Circuit

Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as 4-kword versions (HD404054, HD404094 and HD40A4054). A 4-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 4-kword version.

This limitation apply to the case of using EPROM and the case of using data base.



HD40(A)4052/HD40(A)4054 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404052: 2-kword	☐ HD40A4052: 2-kword
☐ HD404054: 4-kword	☐ HD40A4054: 4-kword

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop mode

☐ Used
☐ Not used

5. Package

☐ DP-42S
☐ FP-44A

HD404092/HD404094 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404092: 2-kword
☐ HD404094: 4-kword

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. Oscillator for OSC1 and OSC2

☐ Ceramic oscillator	f =	MHz
☐ Crystal oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop mode

☐ Used
☐ Not used

5. Package

☐ DP-42S
☐ FP-44A

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