Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT/DT - 2646T/AT/CT
IDT54/74FCT648T/AT/CT
IDT54/74FCT652T/AT/CT/DT - 2652T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - Extended commercial range of –40°C to +85°C
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, TSSOP, CERPACK and LCC packages
- **Features for FCT646T/648T/652T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit “live insertion”
- **Features for FCT2646T/2652T:**
  - Std., A, and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

DESCRIPTION:

The FCT646T/FCT2646T/FCT648T/FCT652T/2652T consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

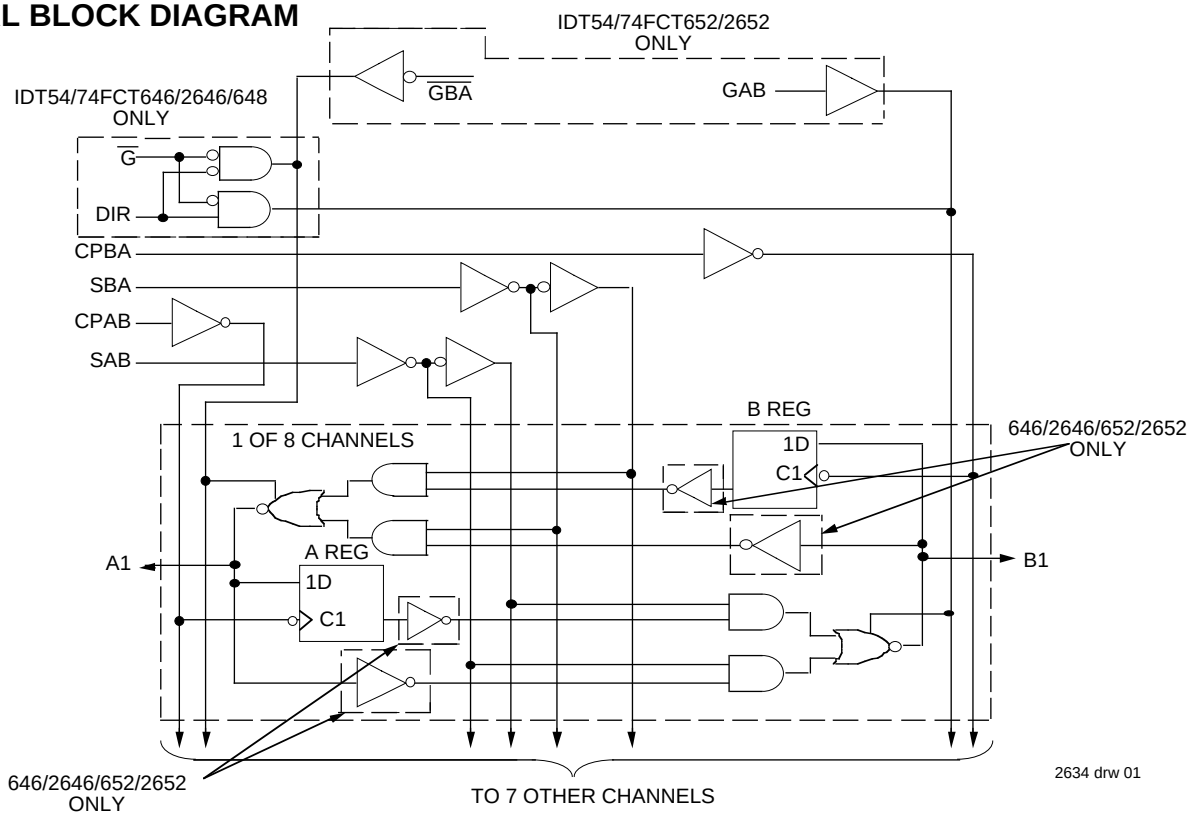
The FCT652T/FCT2652T utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The FCT646T/FCT2646T/FCT648T utilize the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

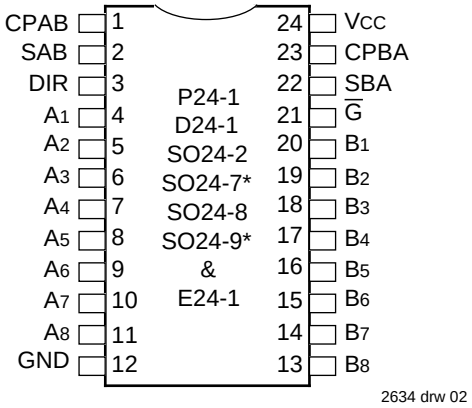
The FCT26xxT have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM



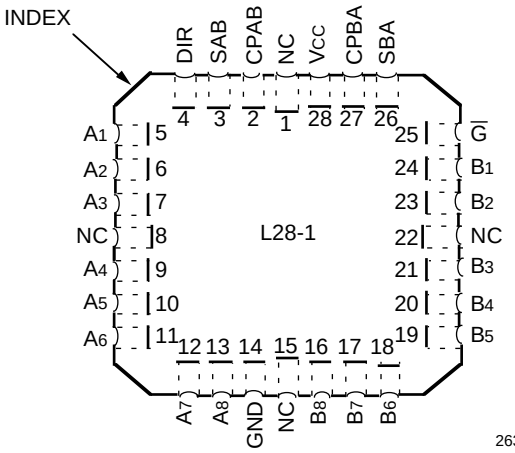
PIN CONFIGURATIONS

FCT646/FCT2646T
FCT648



2634 drw 02

DIP/SOIC/SSOP/
QSOP/TSSOP/CERPACK
TOP VIEW

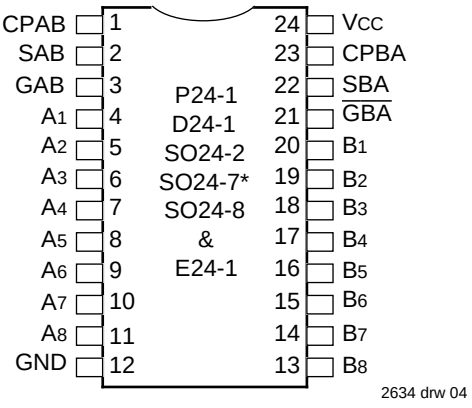


2634 drw 03

LCC
TOP VIEW

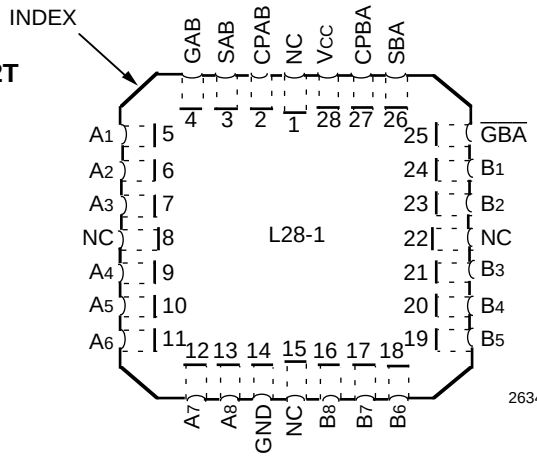
* FCT646/2646T/AT/CT/DT only

FCT652/FCT2652T



2634 drw 04

DIP/SOIC/SSOP/
QSOP/CERPACK
TOP VIEW



2634 drw 05

LCC
TOP VIEW

* FCT652/2652T/AT/CT/DT only

PIN DESCRIPTION

Pin Names	Description
A_1 - A_8	Data Register A Inputs Data Register B Outputs
B_1 - B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (646/648)
GAB, $\overline{GBA}$	Output Enable Inputs (652)

2634 tbl 01

FUNCTION TABLE (646/648)

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	FCT646T/FCT2646T	FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

2634 tbl 02

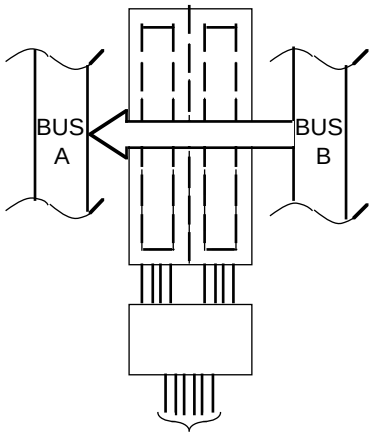
FUNCTION TABLE (652)

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	FCT652T/FCT2652T
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

2634 tbl 03

NOTES:

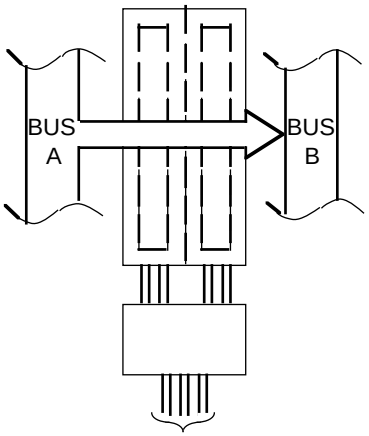
1. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
646/2646/ 648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO A

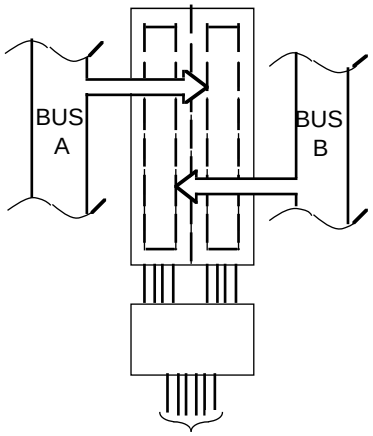
2634 drw 06



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
646/2646/ 648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO B

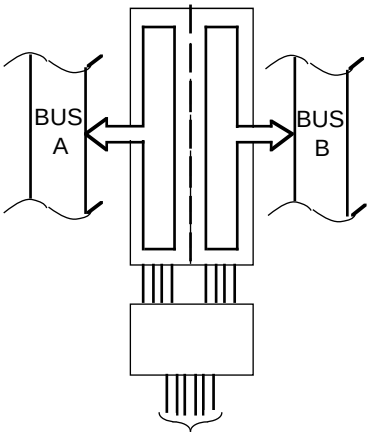
2634 drw 07



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/2646/ 648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM
A AND/OR B

2634 drw 08



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or	H or	H	H
646/2646/ 648 (1)	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or	X	H
	H	L	H or	X	H	X

TRANSFER STORES
DATA TO A AND/OR B

2634 drw 09

NOTE:
1. 646/2646/648 cannot transfer data to A bus and B bus simultaneously.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

2634 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2634 lnk 05
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(4)		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2634 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT646T/648T/652T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2634 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2646T/2652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

NOTES: 2634 lnk 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

NOTES: 2634 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			646/648/652T 2646/2652T				646/648/652AT 2646/2652AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition(1)	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{G}$, DIR to Bus(3)		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{G}$, DIR to Bus(3)		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns

2634 tbl 09

			646/648/652CT 2646/2652CT				646/652DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition(1)	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	1.5	5.4	1.5	6.0	1.5	4.4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{G}$, DIR to Bus(3)		1.5	7.8	1.5	8.9	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{G}$, DIR to Bus(3)		1.5	6.3	1.5	7.7	1.5	4.3	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	4.4	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		1.5	6.2	1.5	7.0	1.5	5.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.0	—	—	—	ns
t_W	Clock Pulse Width, HIGH or LOW(4)		5.0	—	5.0	—	3.0	—	—	—	ns

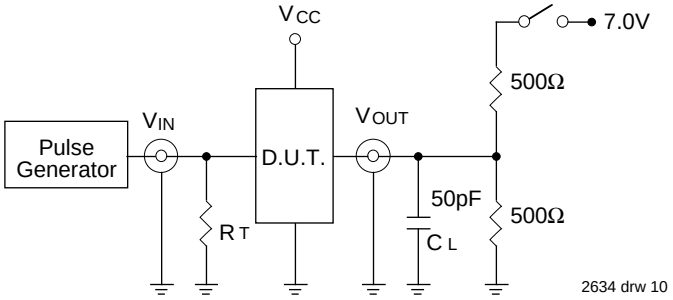
NOTES:

2634 tbl 10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, $\overline{GBA}$ to Bus for 652.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2634 drw 10

SWITCH POSITION

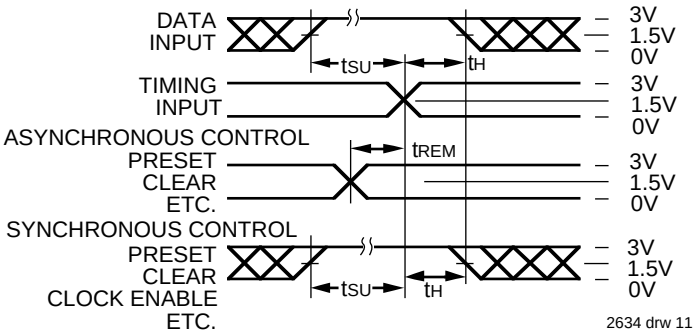
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2634 lnk 11

DEFINITIONS:

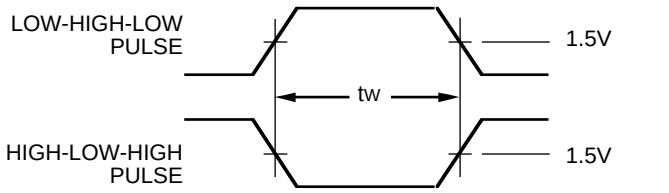
C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



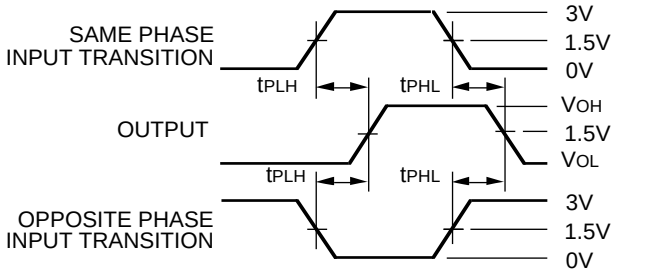
2634 drw 11

PULSE WIDTH



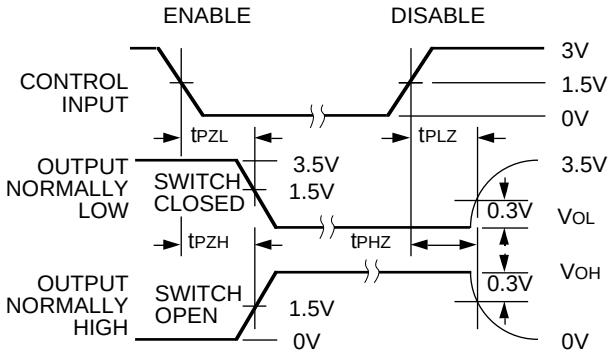
2634 drw 12

PROPAGATION DELAY



2634 drw 13

ENABLE AND DISABLE TIMES



2634 drw 14

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION