HIGH-SPEED CMOS BUS INTERFACE 10-BIT LATCH

IDT74FCTL2841T

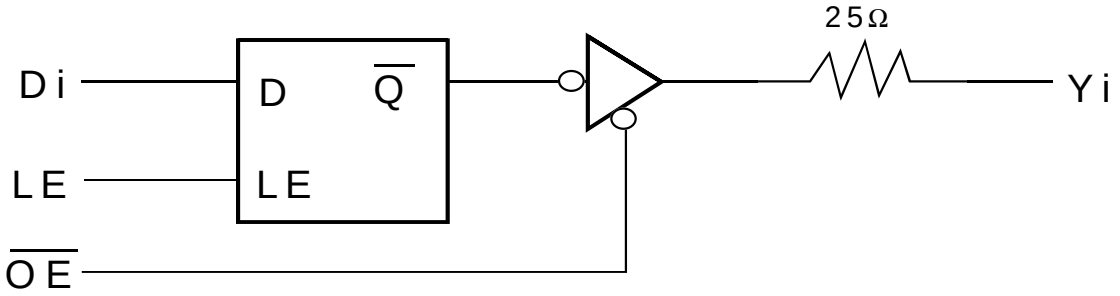
FEATURES:

- Pin and function compatible to the Quality QS74FCT Family
- Extended commercial range of –40°C to +85°C
- CMOS power levels: <7.5mW static
- Available in PDIP, SOIC, and QSOP packages
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.5ns t_{PD} for C
- I_{OL} = 12mA

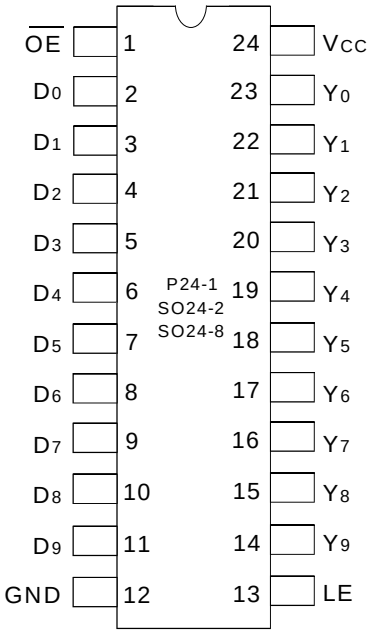
DESCRIPTION:

The IDT74FCTL2841T is a 10-bit high-speed CMOS TTL-compatible buffered latch with 3-state outputs, ideal for driving high-capacitance loads such as memory address and data buses. The device comes in A, B, and C speed grades with 5.5ns (Max.) t_{PHL}/t_{PLH} for the C grade. The 2841 device is a 25Ω resistor output version, useful for driving transmission lines and reducing system noise. The 2841 eliminates the need for external series resistors in high speed systems and can replace the 841 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PDIP/ SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to +7	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current (per pin)	120	mA
I_{IK}	Continuous Clamp Current,	– 20	mA
I_{OK}	$V_I < 0$ or $V_O < 0$	– 50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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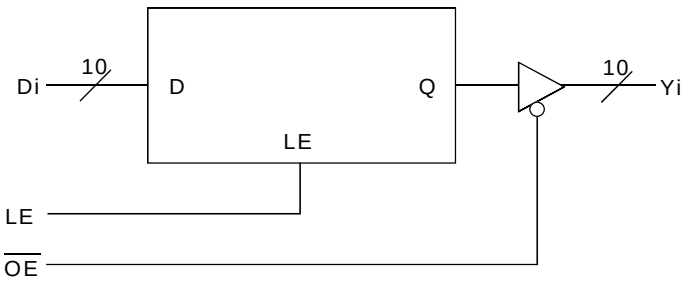
NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Name	I/O	Description
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs V_I are in high-impedance (off) state.

LOGIC SYMBOL



FUNCTION TABLE (1)

Inputs			Internal	Output	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Extended Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for all inputs		—	0.2	—	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	0 ≤ V_{IN} < Vcc	—	—	5	µA
I_{IL}	Input LOW Current						
I_{OZ}	Off-State Output Current (Hi-Z)	V_{CC} = Max.	0 ≤ V_{IN} ≤ Vcc	—	—	5	µA
I_{OR}	Current Drive	V_{CC} = Min., V_{OUT} = 2.0V(2, 3)		50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA, T_A = 25°C(3)		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -15mA	2.4	—	—	V
V_{OL}	Output LOW Voltage - 25Ω	V_{CC} = Min.	I_{OL} = 12mA	—	—	0.5	V
R_{OUT}	Output Resistance - 25Ω	V_{CC} = Min.	I_{OL} = 12mA	20	28	40	Ω

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
3. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
Extended Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions(1)	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(2) freq = 0	—	2	mA
I_{CCD}	Supply Current per Input per MHz	V_{CC} = Max. Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or Vcc(3,4)	—	0.25	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

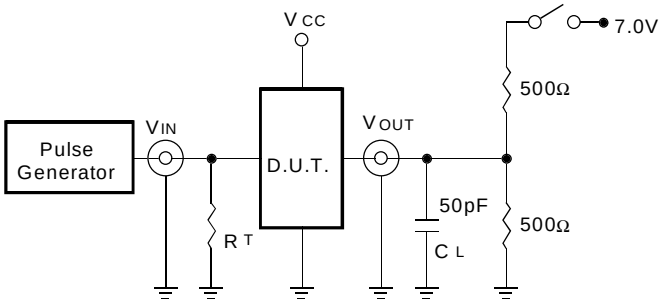
Following Conditions Apply Unless Otherwise Specified:
Extended Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter[2]	74FCTL2841AT		74FCTL2841BT		74FCTL2841CT		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} t_{PLH}	Data to Y Delay $\overline{OE}$ = LOW	—	9.5	—	6.5	—	5.5	ns
t_{PHL} t_{PLH}	Data to Y Delay[3,4] $\overline{OE}$ = LOW	—	20	—	13	—	13	ns
t_{SU}	Data to LE Setup	2.5	—	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time	2.5	—	2.5	—	2.5	—	ns
t_{LEY}	LE to Y Delay $\overline{OE}$ = LOW	—	12	—	8	—	8	ns
t_{LEY}	LE to Y Delay[3,4] $\overline{OE}$ = LOW	—	16	—	15.5	—	15	ns
t_W	LE Pulse Width, HIGH [3]	6	—	4	—	4	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	—	11.5	—	8	—	6.5	ns
t_{PZH} t_{PZL}	Output Enable Time[3,4] $\overline{OE}$ to Yi	—	23	—	14	—	12	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3,5] $\overline{OE}$ to Yi	—	7	—	6	—	5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Yi	—	8	—	7	—	6	ns

NOTES:
1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.
2. See Test Circuits and Waveforms.
3. This parameter is guaranteed by design but not tested.
4. C_{LOAD} = 300pF
5. C_{LOAD} = 5pF

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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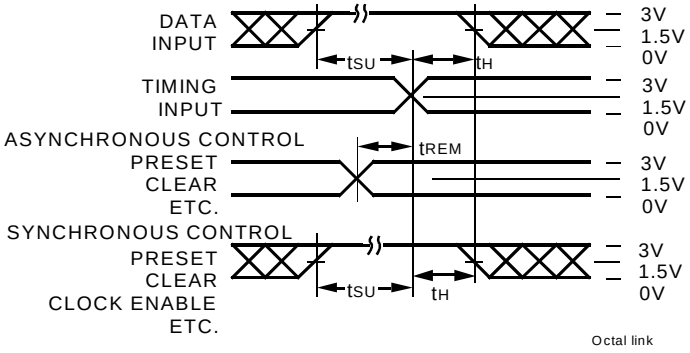
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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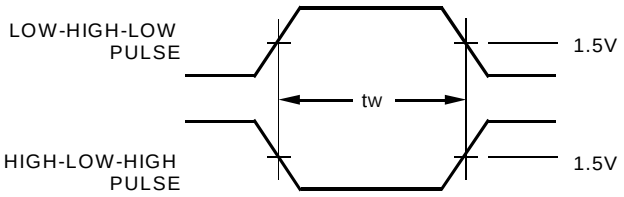
PULSE WIDTH



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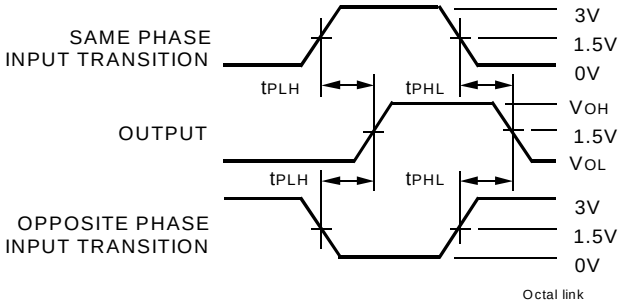
PROPAGATION DELAY



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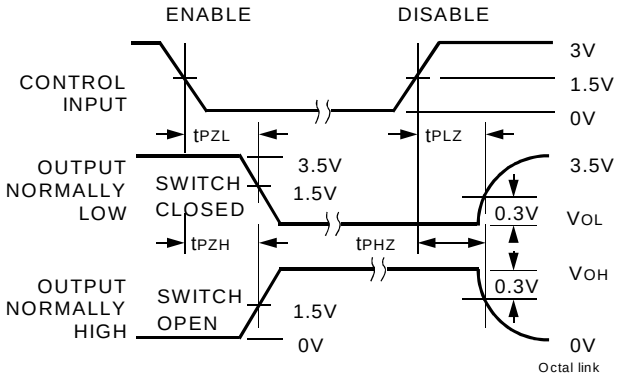
ENABLE AND DISABLE TIMES



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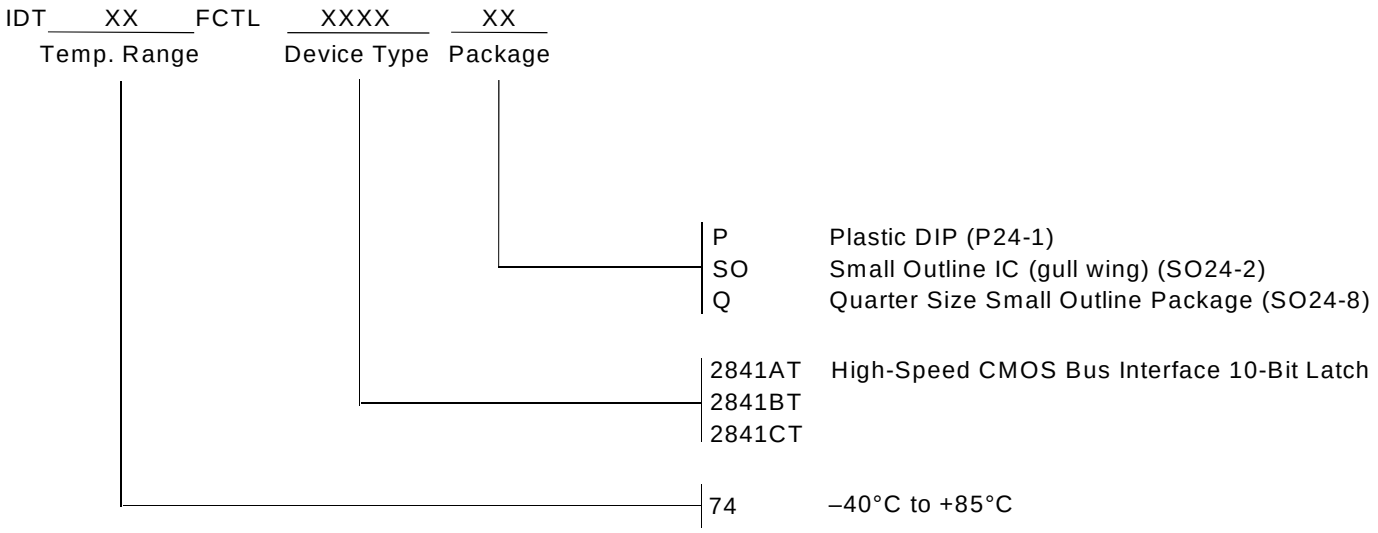
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
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