Integrated Device Technology, Inc.

16K x 32 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M1002

FEATURES

- High-density 512K CMOS Dual-Port RAM module
- Fast access times
  - —Commercial: 30, 35ns
  - —Military: 40, 45ns
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 64 bits or more using the Master/Slave function
- Separate byte read/write signals for byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted fine pitch (25 mil) LCC packages allow through-hole module to fit into 121 pin PGA footprint
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

DESCRIPTION

The IDT7M1002 is a 16K x 32 high-speed CMOS Dual-Port Static RAM Module constructed on a co-fired ceramic substrate using four 16K x 8 (IDT7006) Dual-Port Static RAMs in surface-mounted LCC packages. The IDT7M1002 module is designed to be used as stand-alone 512K Dual-Port RAM or as a combination Master/Slave Dual-Port RAM for 64-bit or more word width systems. Using the IDT Master/Slave approach in such system applications results in full-speed, error-free operation without the need for additional discrete logic.

The module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ and $\overline{INT}$.

The IDT7M1002 module is packaged in a ceramic 121 pin PGA (Pin Grid Array)1.35 inches on a side. Maximum access times as fast as 30ns are available over the commercial temperature range and 40ns over the military temperature range.

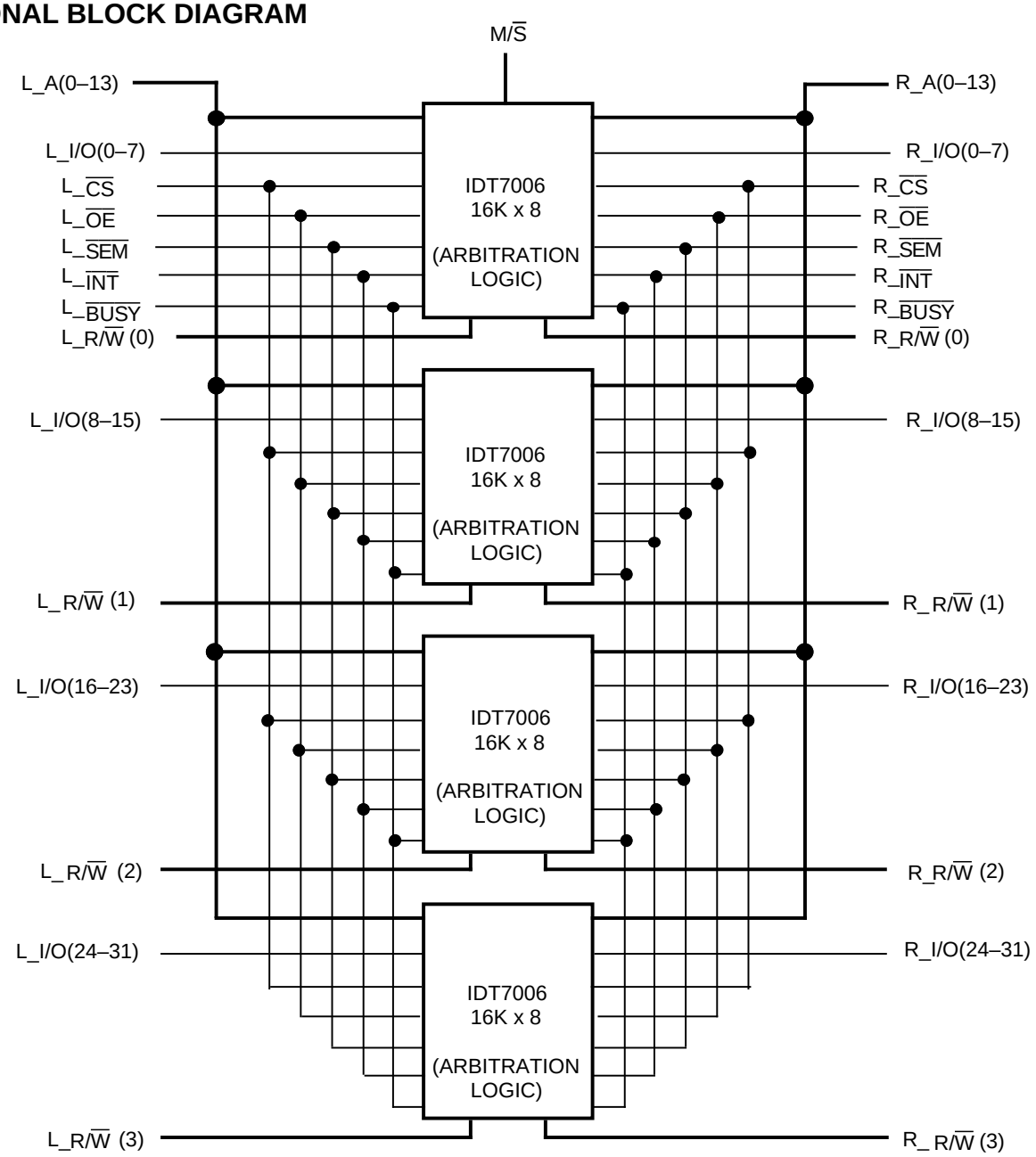
All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	L_I/O(24)	L_I/O(26)	L_I/O(28)	L_I/O(30)	L_$\overline{CS}$	L_$\overline{OE}$	L_R/$\overline{W}$(3)	R_$\overline{OE}$	R_$\overline{CS}$	R_I/O(30)	R_I/O(28)	R_I/O(26)	R_I/O(24)
B	L_I/O(23)	L_I/O(25)	L_I/O(27)	L_I/O(29)	L_I/O(31)	L_A(0)	L_R/$\overline{W}$(4)	R_A(0)	R_I/O(31)	R_I/O(29)	R_I/O(27)	R_I/O(25)	R_I/O(23)
C	L_I/O(21)	L_I/O(22)	VCC	L_A(3)	L_A(2)	L_A(1)	GND	R_A(1)	R_A(2)	R_A(3)	GND	R_I/O(22)	R_I/O(21)
D	L_I/O(19)	L_I/O(20)	L_A(4)	GND							R_A(4)	R_I/O(20)	R_I/O(19)
E	L_I/O(17)	L_I/O(18)	L_A(5)								R_A(5)	R_I/O(18)	R_I/O(17)
F	L_$\overline{SEM}$	L_I/O(16)	L_A(6)								R_A(6)	R_I/O(16)	R_$\overline{SEM}$
G	L_$\overline{BUSY}$	L_$\overline{INT}$	GND				PGA TOP VIEW				GND	R_$\overline{INT}$	R_$\overline{BUSY}$
H	L_R/$\overline{W}$(1)	L_R/$\overline{W}$(2)	L_A(7)								R_A(7)	R_R/$\overline{W}$ (2)	R_R/$\overline{W}$ (1)
I	L_I/O(15)	L_I/O(14)	L_A(8)								R_A(8)	R_I/O(14)	R_I/O(15)
J	L_I/O(13)	L_I/O(12)	L_A(9)								R_A(9)	R_I/O(12)	R_I/O(13)
K	L_I/O(11)	M/$\overline{S}$	GND	L_A(10)	L_A(11)	L_A(12)	GND	R_A(12)	R_A(11)	R_A(10)	VCC	GND	R_I/O(11)
L	L_I/O(10)	L_I/O(8)	L_I/O(6)	L_I/O(4)	L_I/O(2)	L_A(13)	R_R/$\overline{W}$ (4)	R_A(13)	R_I/O(2)	R_I/O(4)	R_I/O(6)	R_I/O(8)	R_I/O(10)
M	L_I/O(9)	L_I/O(7)	L_I/O(5)	L_I/O(3)	L_I/O(1)	L_I/O(0)	R_R/$\overline{W}$ (3)	R_I/O(0)	R_I/O(1)	R_I/O(3)	R_I/O(5)	R_I/O(7)	R_I/O(9)

2795 drw 01

FUNCTIONAL BLOCK DIAGRAM



2795 drw 02

PIN NAMES

Left Port	Right Port	Description
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–31)	R_I/O (0–31)	Data Inputs/Outputs
L_R/W (1–4)	R_R/W (1–4)	Read/Write Enables
L_CS	R_CS	Chip Select
L_OE	R_OE	Output Enable
L_BUSY	R_BUSY	Busy Flag
L_INT	R_INT	Interrupt Flag
L_SEM	R_SEM	Semaphore Control
M/S		Master/Slave Control
Vcc		Power
GND		Ground

2795 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commerical	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2795 tbl 02

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2795 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2795 tbl 04

NOTE:
1. VIL ≥ –3.0V for pulse width less than 20ns

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$\|I_{LI}\|$	Input Leakage (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA	2.4	—	V

2795 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, $\overline{SEM}$ = Don't Care Outputs Open, f = f_{MAX}	—	1360	—	1600	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., L_$\overline{CS}$ and R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	280	—	340	mA
I_{SB1}	Standby Suppy Current (One Port Inactive)	V_{CC} = Max., L_$\overline{CS}$ or R_$\overline{CS} \geq V_{IH}$ Outputs Open, f = f_{MAX}	—	1000	—	1160	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	L_$\overline{CS}$ and R_$\overline{CS} \geq V_{CC}$ – 0.2V $V_{IN} > V_{CC}$ – 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \geq V_{CC}$ – 0.2V	—	60	—	120	mA

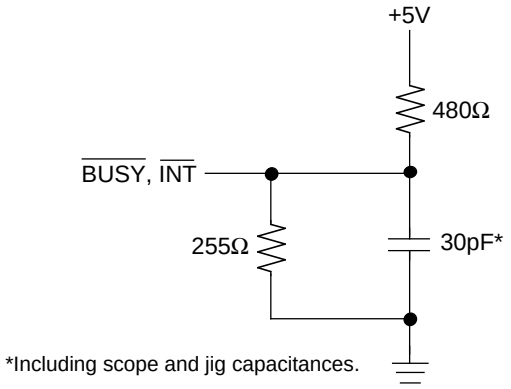
2795 tbl 06

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN} (1)	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{SEM}$, Address)	V_{IN} = 0V	40	pF
$C_{IN(2)}$	Input Capacitance (R/$\overline{W}$, $\overline{I/O}$, $\overline{INT}$)	V_{IN} = 0V	12	pF
$C_{IN(3)}$	Input Capacitance ($\overline{BUSY}$, M/$\overline{S}$)	V_{IN} = 0V	45	pF
C_{OUT}	Output Capacitance (I/O)	V_{OUT} = 0V	12	pF

2795 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.



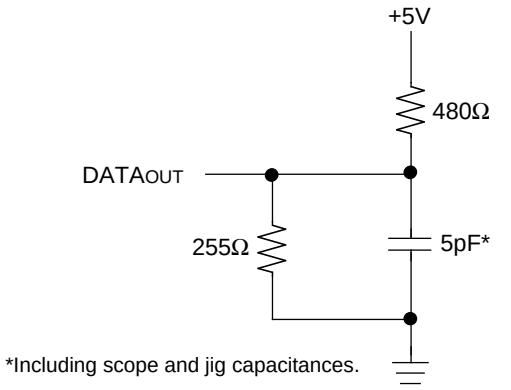
2795 drw 03

Figure 1. Output Load

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2795 tbl 08



2795 drw 04

Figure 2. Output Load
(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

		7M1002SxxG				7M1002SxxGB				
		30		–35		–40		–45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	ns
t_{ACS}[2]	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
t_{OE}	Output Enable Access Time	—	17	—	20	—	22	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{LZ}[1]	Output to Low-Z	3	—	3	—	3	—	5	—	ns
t_{HZ}[1]	Output to High-Z	—	15	—	15	—	17	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{CW}[2]	Chip Select to End-of-Write	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns

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(Continued on next page)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 55°C to +125°C or 0°C to +70°C)

		7M1002SxxG				7M1002SxxGB				
		30		–35		–40		–45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle (continued)										
t_{DW}	Data Valid to End-of-Write	22	—	25	—	25	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{HZ}(1)	Output to High-Z	—	15	—	15	—	17	—	20	ns
t_{OW}(1)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	10	—	ns
Busy Cycle-Master Mode(3)										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	30	—	35	—	35	—	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	25	—	30	—	30	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	25	—	30	—	30	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Deselect	—	25	—	25	—	25	—	25	ns
t_{WDD}(5)	Write Pulse to Data Delay	—	55	—	60	—	65	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	40	—	45	—	50	—	55	ns
t_{APS}(6)	Arbitration Priority Set-Up Time	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	ns
Busy Cycle-Slave Mode (4)										
t_{WB}(7)	Write to BUSY Input	0	—	0	—	0	—	0	—	ns
t_{WH}(8)	Write Hold after BUSY	25	—	25	—	25	—	25	—	ns
t_{WDD}(5)	Write Pulse to Data Delay	—	55	—	60	—	65	—	70	ns
Interrupt Timing										
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	30	—	32	—	35	ns
t_{INR}	Interrupt Reset Time	—	25	—	30	—	32	—	35	ns

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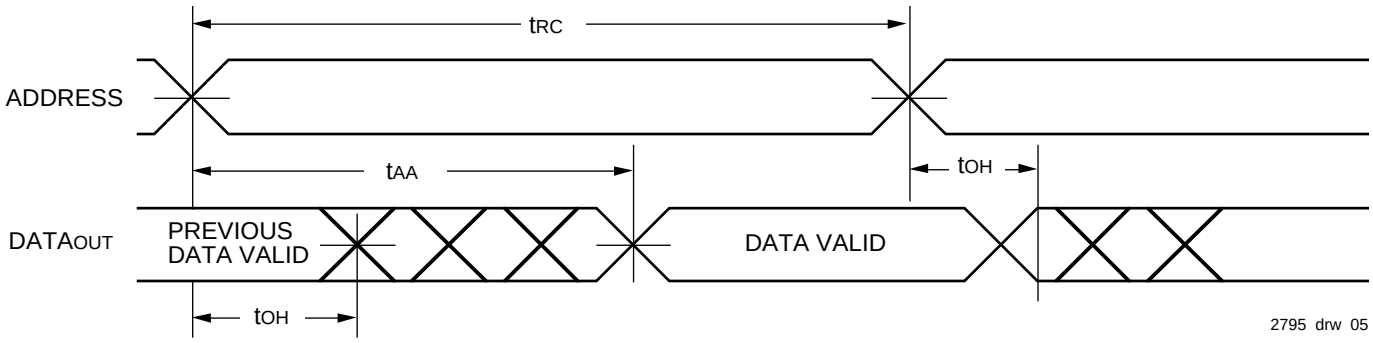
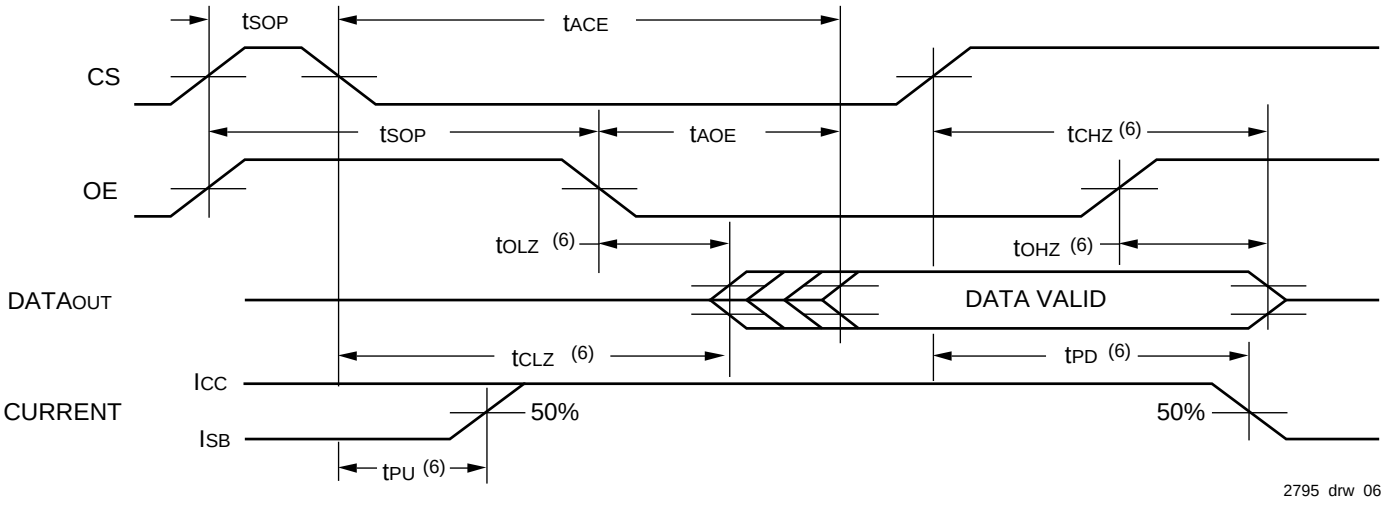
NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \le V_{IL}$ and $\overline{SEM} \ge V_{IH}$. To access semaphore, $\overline{CS} \ge V_{IH}$ and $\overline{SEM} \le V_{IL}$.
3. When the module is being used in the Master Mode (M/$\overline{S} \ge V_{IH}$).
4. When the module is being used in the Slave Mode (M/$\overline{S} \le V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. tBDD is a calculated parameter and is the greater of 0, tWDD - tWP (actual), or tDDD - tWP (actual).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)

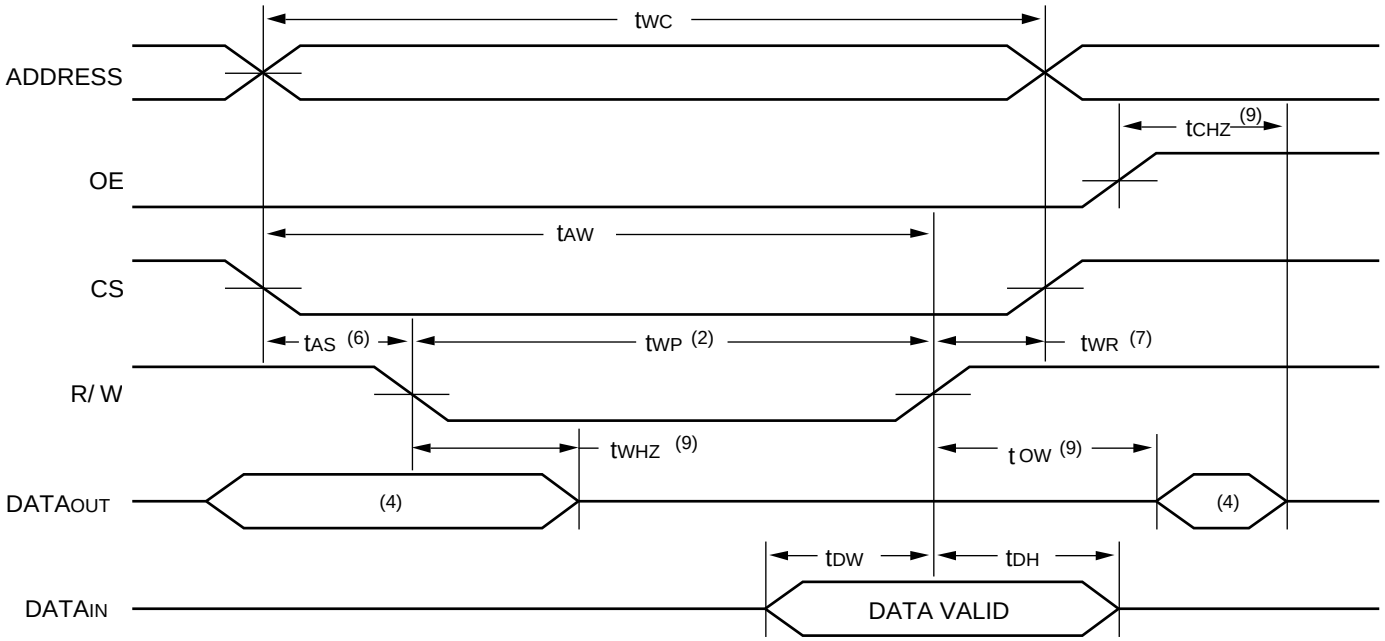


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3, 5)



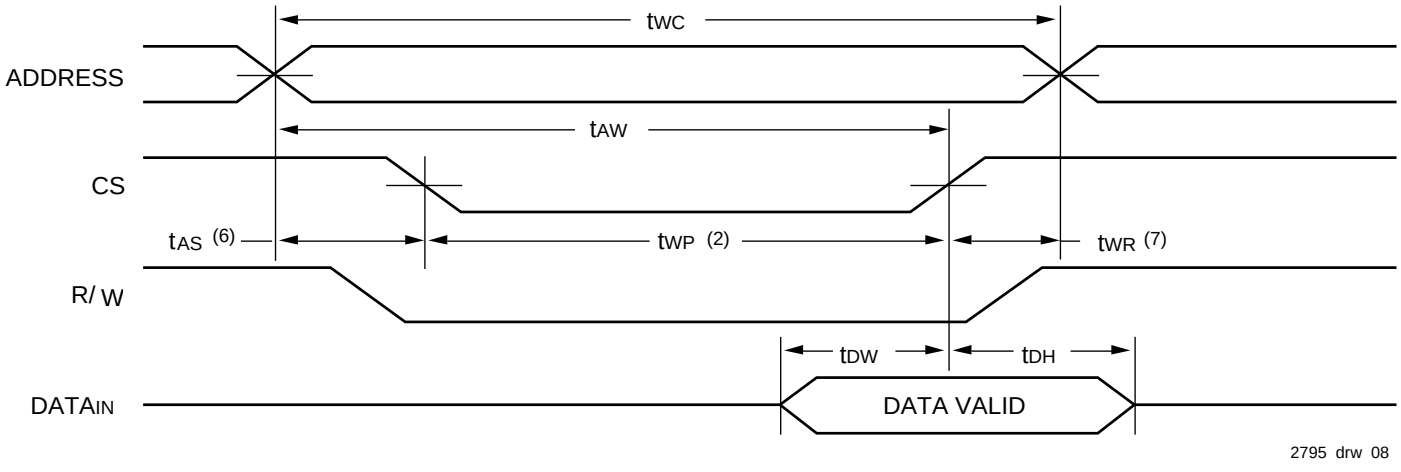
NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled $\overline{CS} \leq V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
6. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 4)



2795 drw 07

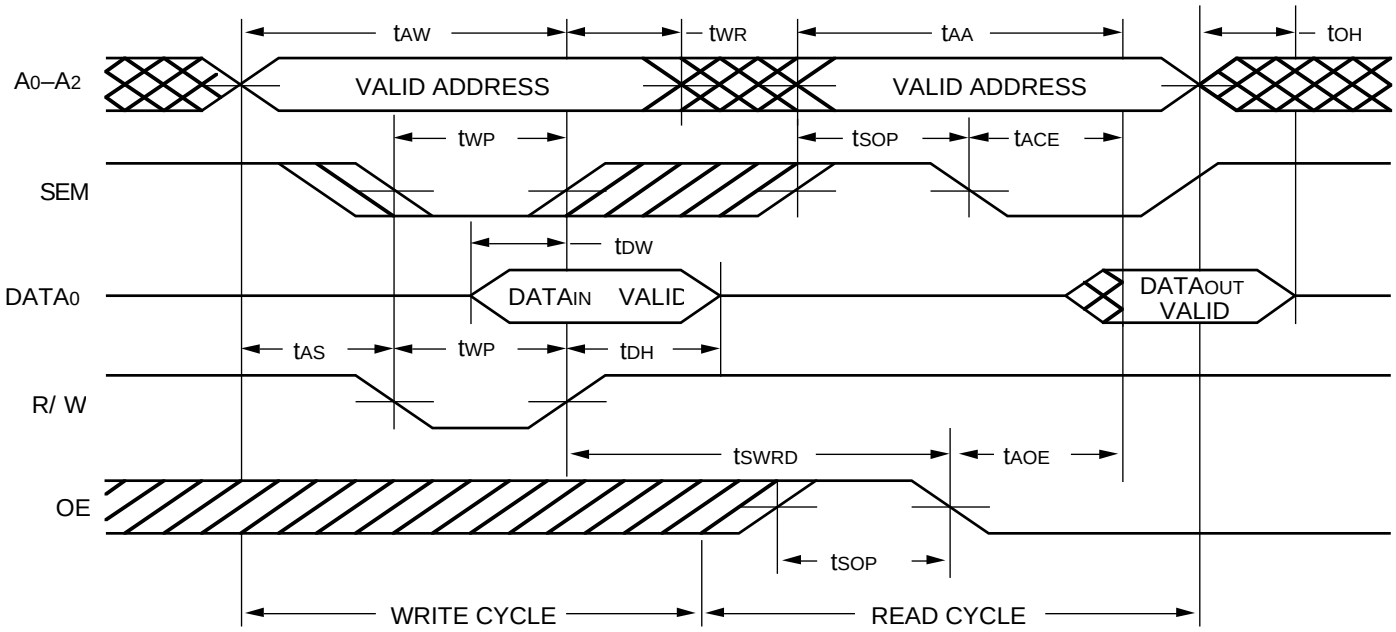
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 4)



2795 drw 08

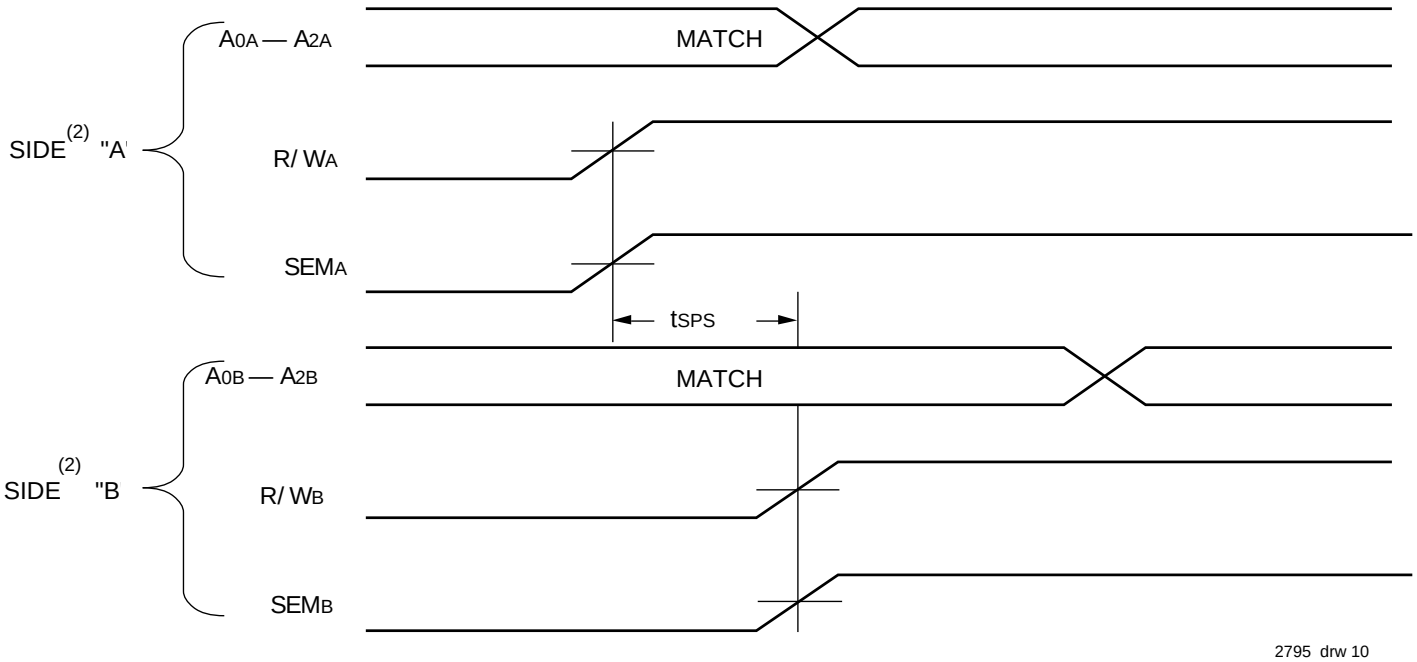
NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE, EITHER SIDE(1)



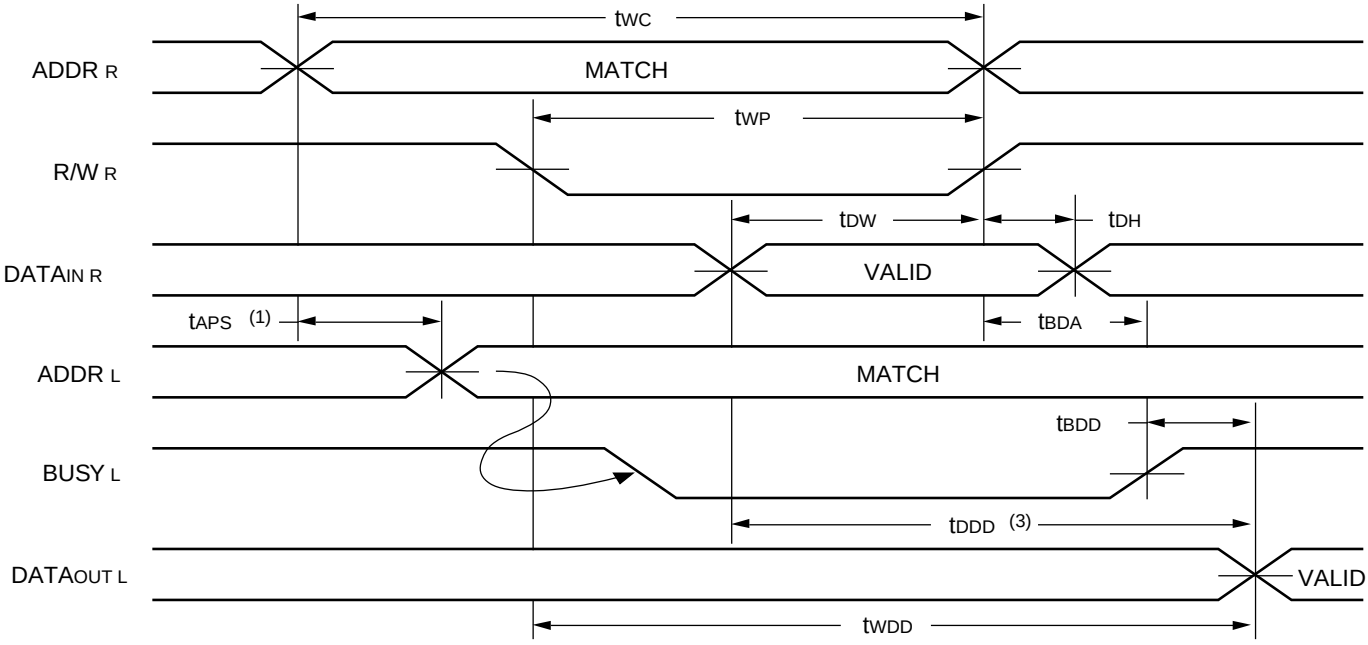
NOTE:
1. $\overline{CS} \geq V_{IH}$ for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION(1, 3, 4)



NOTES:
1. $D_{OR} = D_{OL} \leq V_{IL}$, ($L\_\ \overline{CS} = R\_\ \overline{CS}$) $\geq V_{IH}$ Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to $R/\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

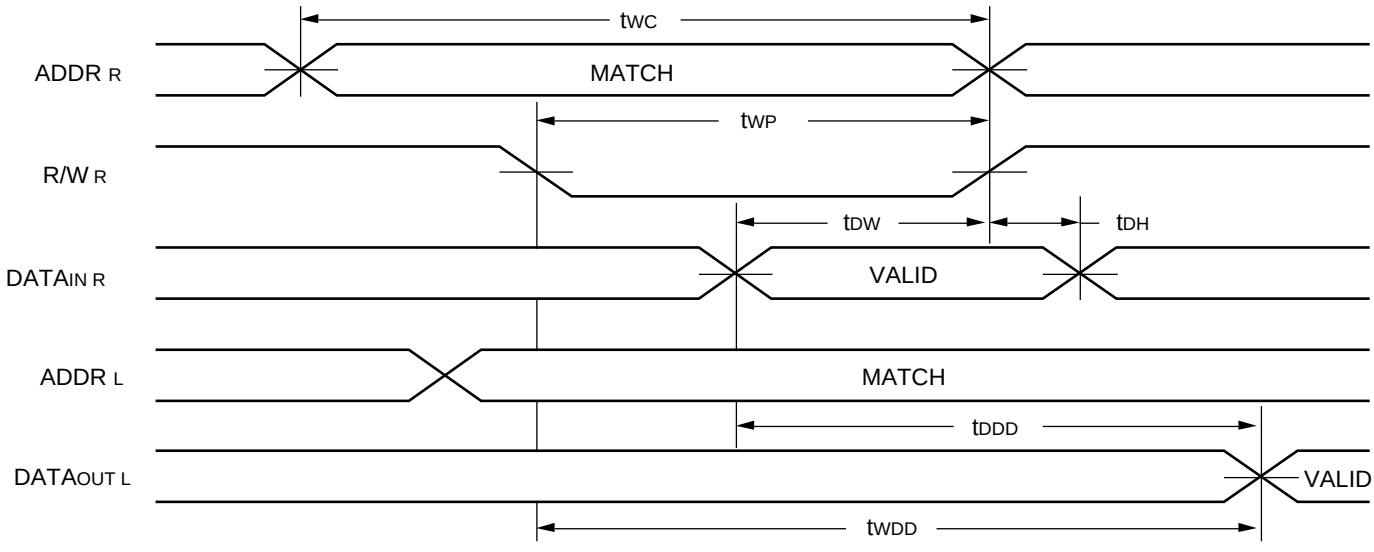
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (M/$\overline{S}$ ≥ VIH)(2)



2795 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL
3. $\overline{OE}$ ≤ VIL for the reading port.

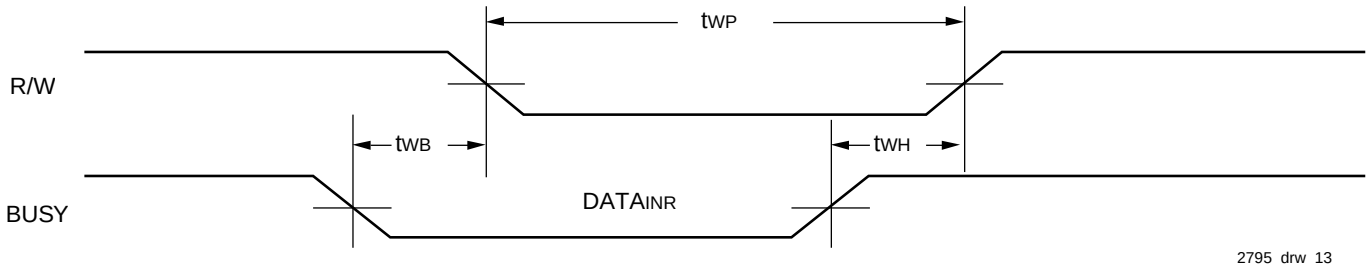
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY (M/$\overline{S}$ ≤ VIH)(1, 2)



2795 drw 12

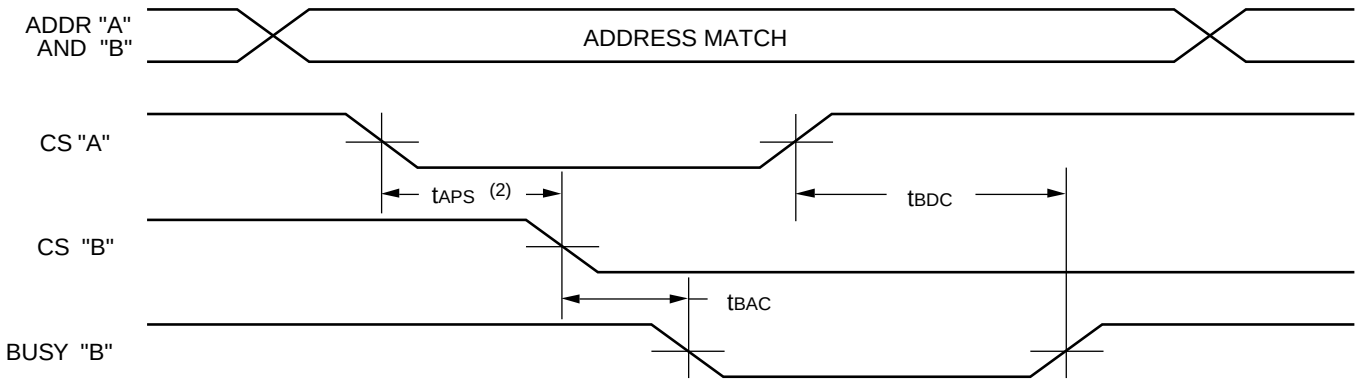
NOTES:
1. $\overline{BUSY}$ input equals HIGH for the writing port.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (M/$\overline{S}$ ≤ VIL)



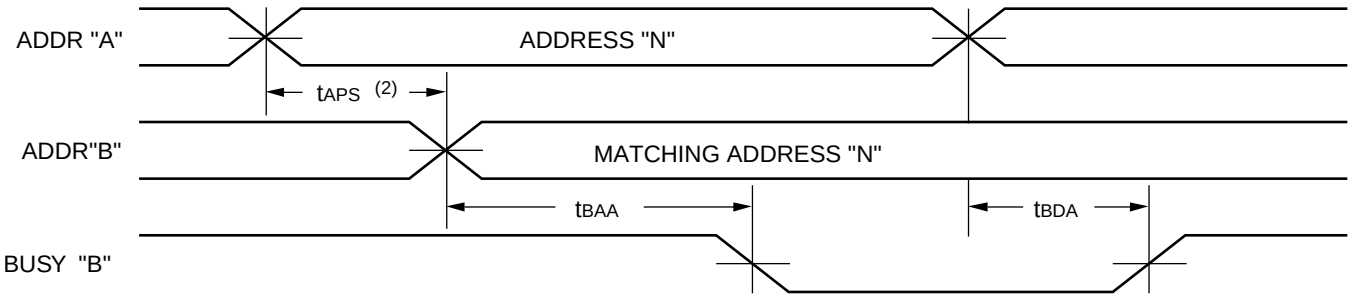
2795 drw 13

TIMING WAVEFORM OF BUSY ARBITRATION ($\overline{CS}$ CONTROLLED TIMING)(1)



2795 drw 14

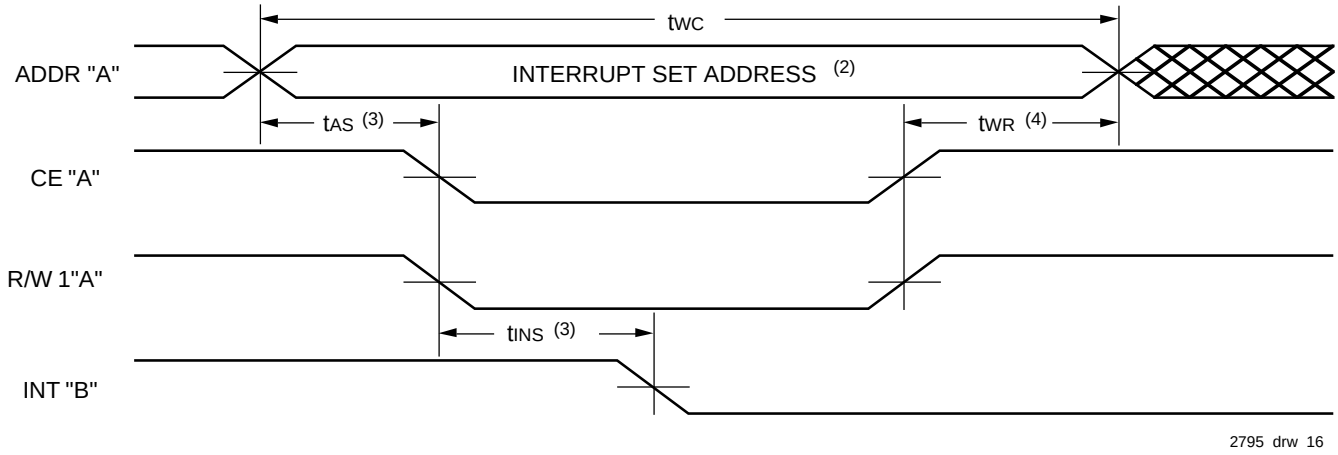
TIMING WAVEFORM OF BUSY ARBITRATION (CONTROLLED BY ADDRESS MATCH TIMING(1)



2795 drw 15

NOTES:
1. All timing is the same for the left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

TIMING WAVEFORM OF INTERRUPT CYCLE(1)



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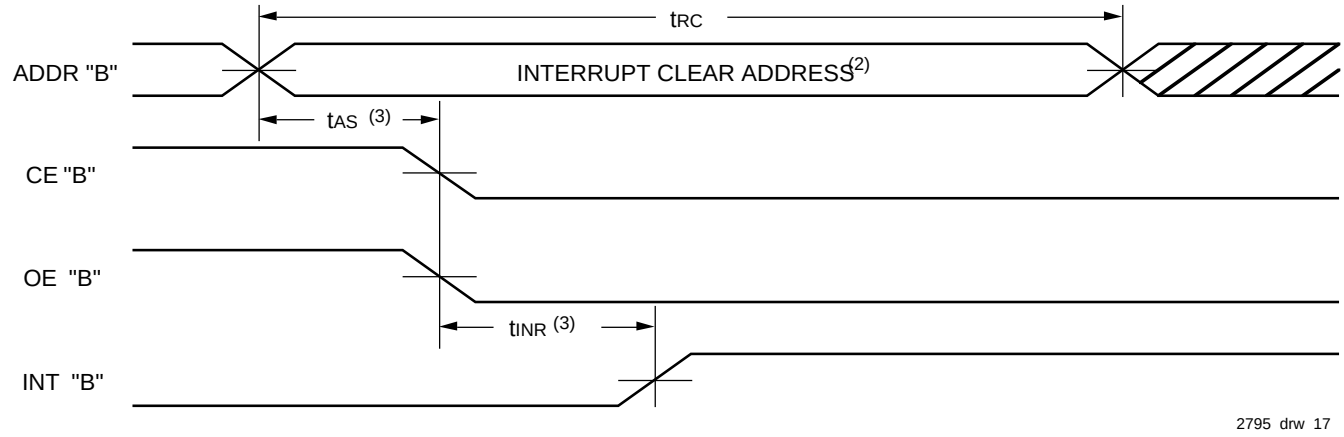

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NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLE I: Non-Contention Read/Write Control(1)

Inputs				Outputs	Mode
$\overline{CS}$	R/W	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	X	X	H	High-Z	Deselected or Power Down
L	L	X	H	Data_In	Write
L	H	L	H	Data_OUT	Read
X	X	H	X	High-Z	Outputs Disabled

2795 tbl 13

NOTE:
1. The conditions for non-contention are L_A (0–13) ≠ R_A (0–13).
2. ⌐ denotes a LOW to HIGH waveform transition.

TRUTH TABLE II: Semaphore Read/Write Control

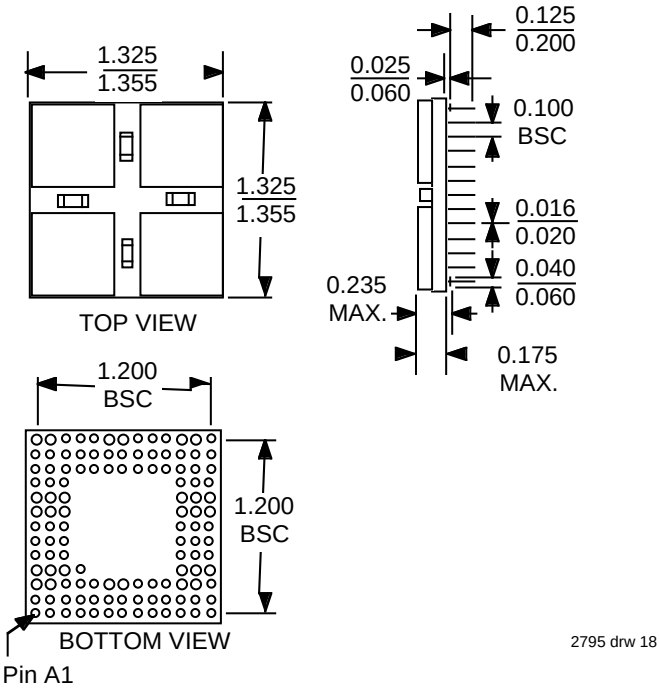
Inputs(2)				Outputs	Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	H	L	L	Data_OUT	Read Data in Semaphore Flag
H	⌐	X	L	Data_IN	Write Data_IN (0, 8, 16, 24)
L	X	X	L	—	Not Allowed

2795 tbl 14

INTERRUPT/BUSY FLAGS, DEPTH & WIDTH EXPANSION, MASTER/SLAVE CONTROL, SEMAPHORES

For more details regarding Interrupt/Busy flags, depth and/or width expansion, master/slave control, or semaphore operations, please consult the IDT7006 data sheet.

PACKAGE DIMENSIONS



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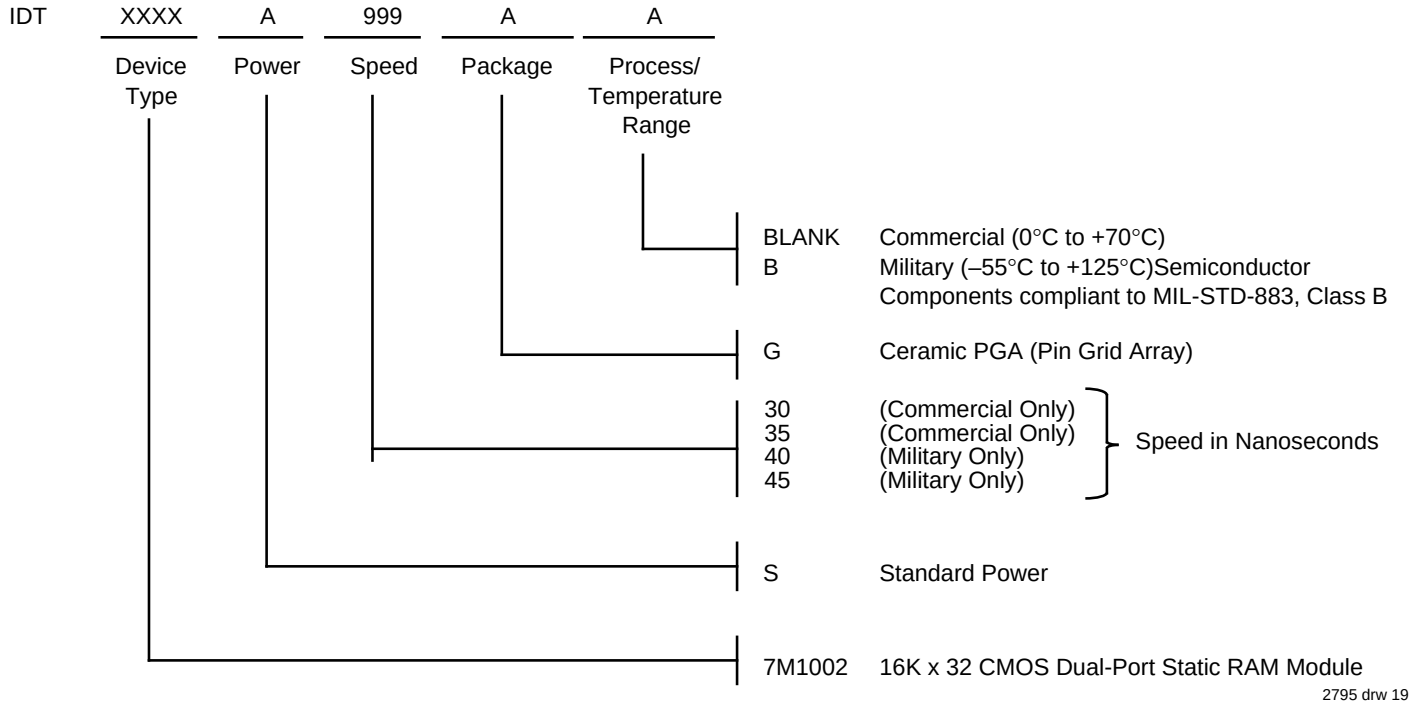
ORDERING INFORMATION



2795 drw 19