64K x 32
CMOS Static RAM Module

IDT7MP4036

Features

- **High-density 2MB Static RAM module**
- **Low profile 64-pin ZIP (Zig-zag In-line vertical Package) or 64-pin SIMM (Single In-line Memory Module)**
- **Ultra fast access time: 12ns (max.)**
- **Surface mounted plastic components on an epoxy laminate (FR-4) substrate**
- **Single 5V (±10%) power supply**
- **Multiple GND pins and decoupling capacitors for maximum noise immunity**
- **Inputs/outputs directly TTL-compatible**

Pin Configuration[1]

	1	GND	
PD_0	2	3	PD_1	PD_0 – OPEN
I/O_0	4	5	I/O_8	PD_1 – GND
I/O_1	6	7	I/O_9	
I/O_2	8	9	I/O_{10}	
I/O_3	10	11	I/O_{11}	
V_{CC}	12	13	A_0	
A_7	14	15	A_1	
A_8	16	17	A_2	
A_9	18	19	I/O_{12}	
I/O_4	20	21	I/O_{13}	
I/O_5	22	23	I/O_{14}	
I/O_6	24	25	I/O_{15}	
I/O_7	26	27	GND	
$\overline{WE}$	28	29	A_{15}	
A_{14}	30	31	$\overline{CS}_2$	
$\overline{CS}_1$	32			
		33	$\overline{CS}_4$	
$\overline{CS}_3$	34	35	NC	
NC	36	37	$\overline{OE}$	
GND	38	39	I/O_{24}	
I/O_{16}	40	41	I/O_{25}	
I/O_{17}	42	43	I/O_{26}	
I/O_{18}	44	45	I/O_{27}	
I/O_{19}	46	47	A_3	
A_{10}	48	49	A_4	
A_{11}	50	51	A_5	
A_{12}	52	53	V_{CC}	
A_{13}	54	55	A_6	
I/O_{20}	56	57	I/O_{28}	
I/O_{21}	58	59	I/O_{29}	
I/O_{22}	60	61	I/O_{30}	
I/O_{23}	62	63	I/O_{31}	
GND	64			

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ZIP, SIMM
Top View

NOTE:

1. Pins 2 and 3 (PD_0 and PD_1) are read by the user to determine the density of the module. If PD_0 reads Open and PD_1 reads GND, then the module had a 64K depth.

Description

The IDT7MP4036 is a 64K x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using eight 64K x 4 Static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 256K Static RAMs fabricated in IDT's high-performance, high-reliability CMOS technology. The IDT7MP4036 is available with access time as fast as 12ns with minimal power consumption.

The IDT7MP4036 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.50 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4036 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD_0 and PD_1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD_0 and PD_1 to determine a 64K depth.

Pin Names

I/O_{0-31}	Data Inputs/Outputs
A_{0-15}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

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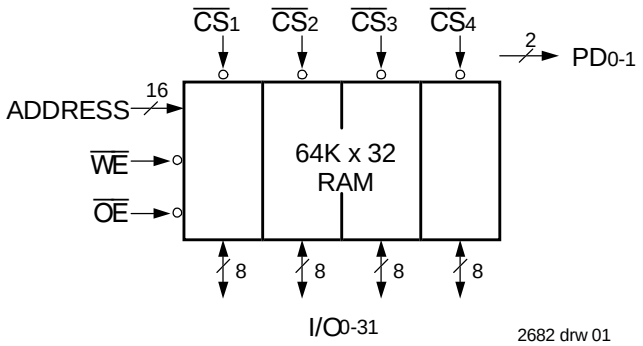
DECEMBER 1999

Functional Block Diagram



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Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

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Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	15	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	V_{IN} = 0V	70	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

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NOTE:
1. This parameter is guaranteed by design but not tested.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. I/O pins must not exceed V_{CC} +0.5V.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}(2)	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

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NOTES:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.
2. I/O pins must not exceed V_{CC}+0.5V.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

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DC Electrical Characteristics

(Vcc = 5.0V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	80	µA
I_{LI}	Input Leakage Current (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Outputs Open	—	1280	mA
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, f = f_{MAX}, Outputs Open	—	360	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V, f = 0 V_{IN} > V_{CC} - 0.2V or < 0.2V	—	240	mA

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AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2682 tbl 08

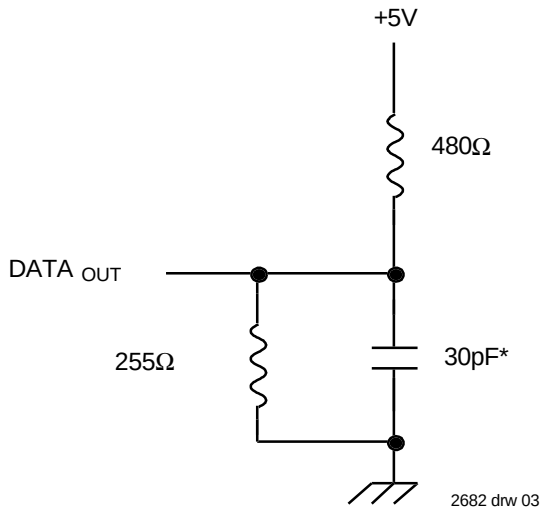

Figure 1. Output Load

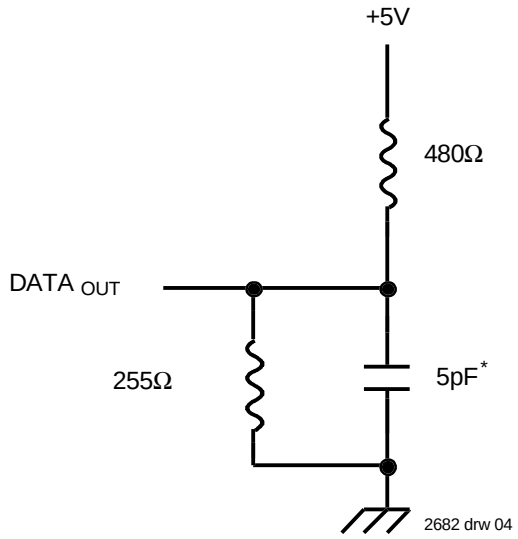

Figure 2. Output Load
(for t_{OLZ}, t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

*incluces scope and jig.

AC Electrical Characteristics

(Vcc = 5V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4036SxxZ, 7MP4036SxxM						Unit
		-12[2]		-13		-15		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	13	—	15	—	ns
t_{AA}	Address Access Time	—	12	—	13	—	15	ns
t_{ACS}	Chip Select Access Time	—	12	—	13	—	15	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	2	—	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	9	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	7	—	7	—	8	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	7	—	7	—	8	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	12	—	13	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	13	—	15	—	ns
t_{CW}	Chip Select to End-of-Write	10	—	11	—	12	—	ns
t_{AW}	Address Valid to End-of-Write	11	—	12	—	13	—	ns
t_{AS}	Address Set-up Time	1	—	1	—	1	—	ns
t_{WP}	Write Pulse Width	10	—	11	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	7	—	7	—	8	ns
t_{DW}	Data to Write Time Overlap	7	—	7	—	8	—	ns
t_{DH}	Data Hold Time	1	—	1	—	1	—	ns
t_{OW}[1]	Output Active from End-of-Write	2	—	2	—	1	—	ns

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NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

AC Electrical Characteristics

(Vcc = 5V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4036SxxZ, 7MP4036SxxM						Unit
		-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	—	25	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	10	—	15	—	22	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	10	—	15	—	22	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	20	—	25	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	12	—	15	—	18	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	0	—	0	—	0	—	ns

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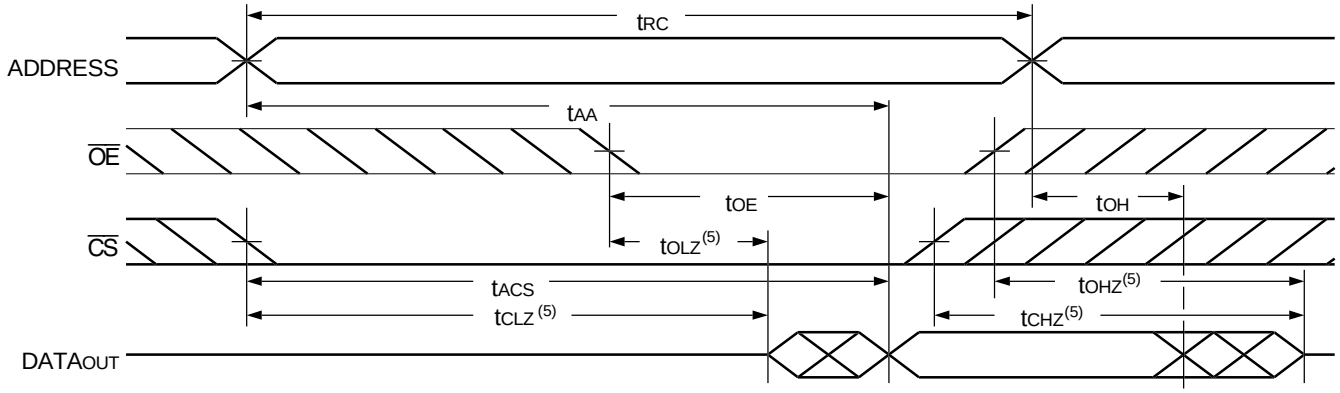
NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

Timing Waveform of Read Cycle No. 1(1)



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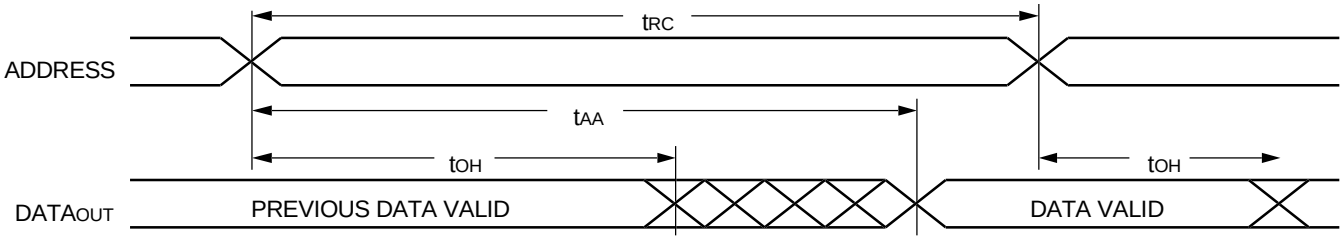
Timing Waveform of Read Cycle No. 2(1,2,4)



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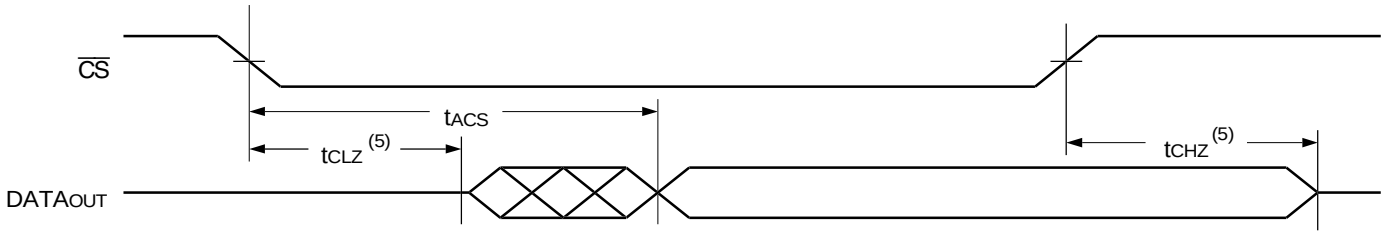
Timing Waveform of Read Cycle No. 3(1,3,4)



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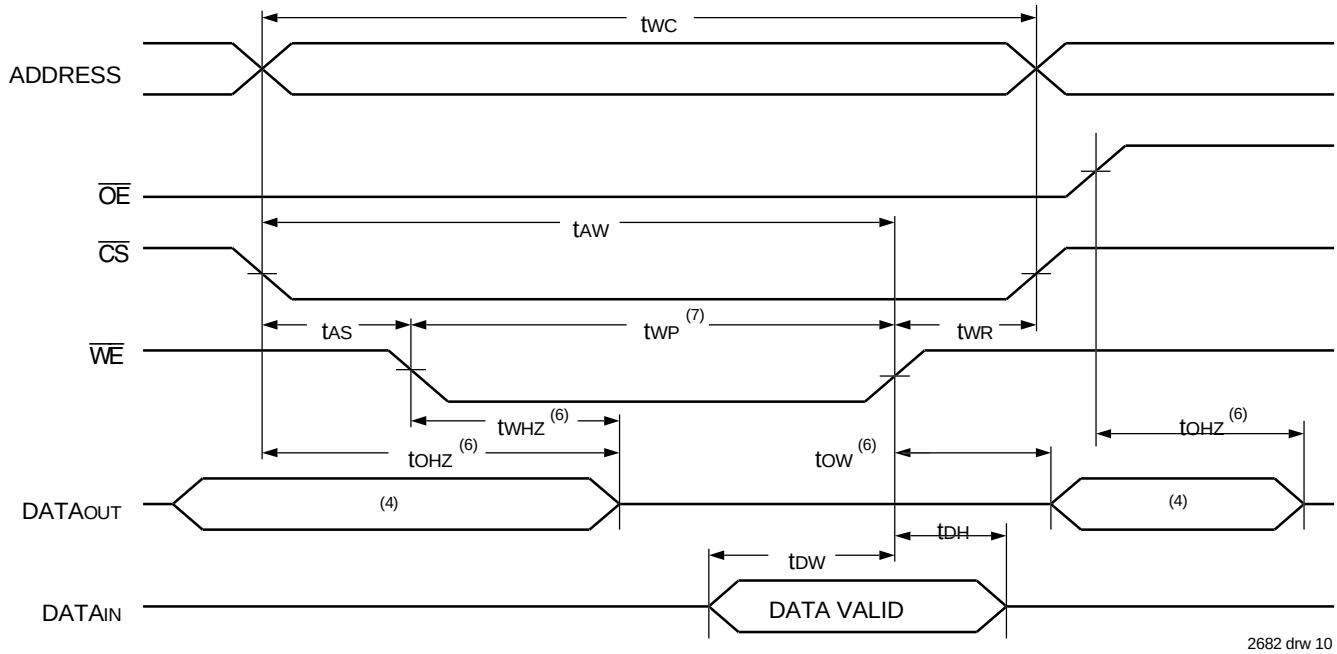
NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,3,7)



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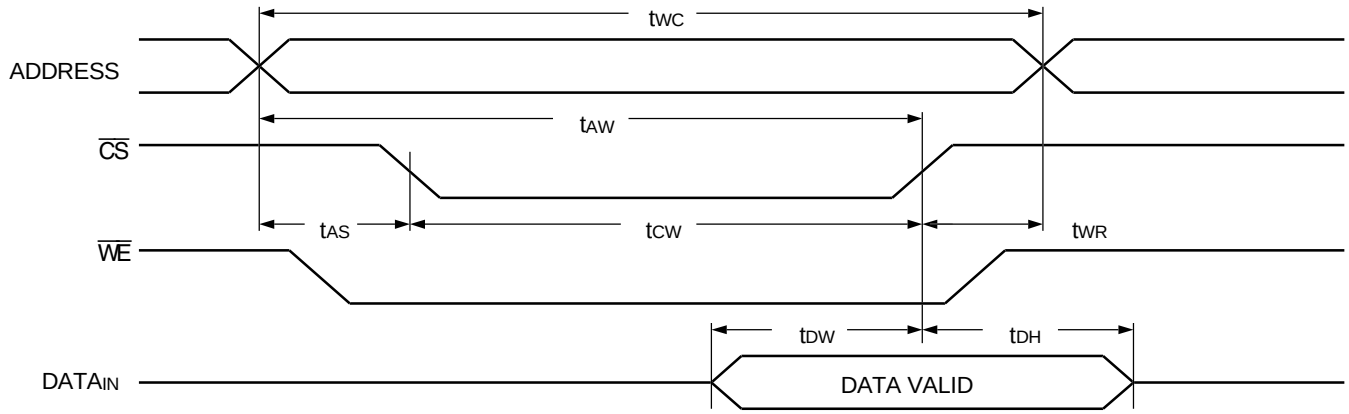
Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,2,3,5)



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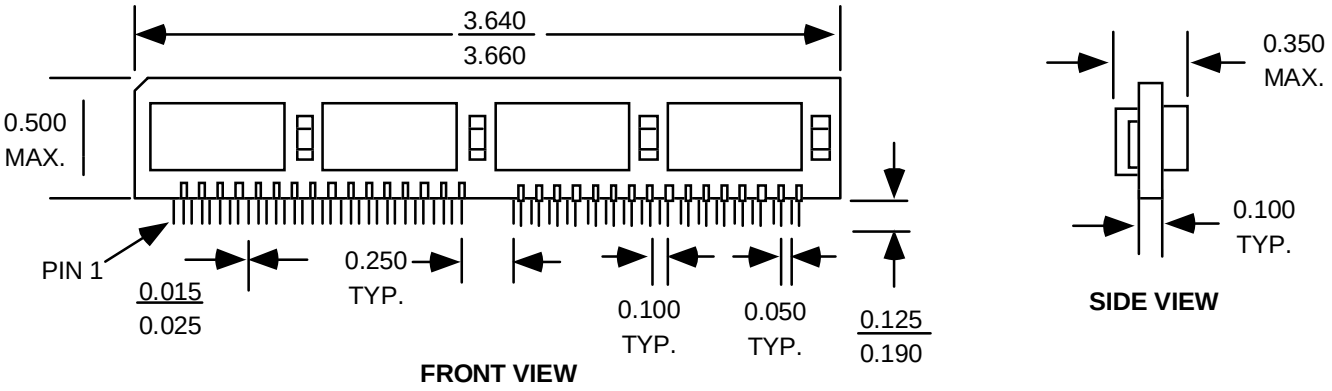
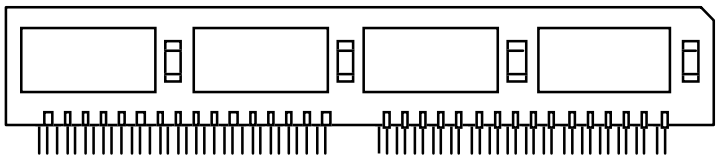
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but, not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Package Dimensions

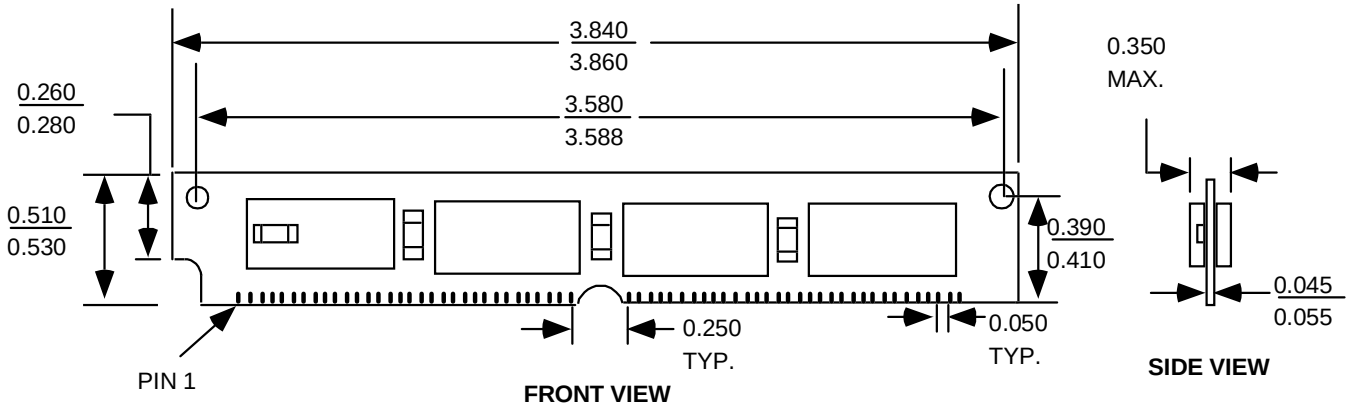
ZIP VERSION

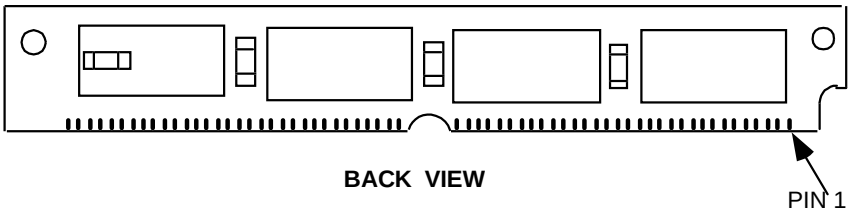




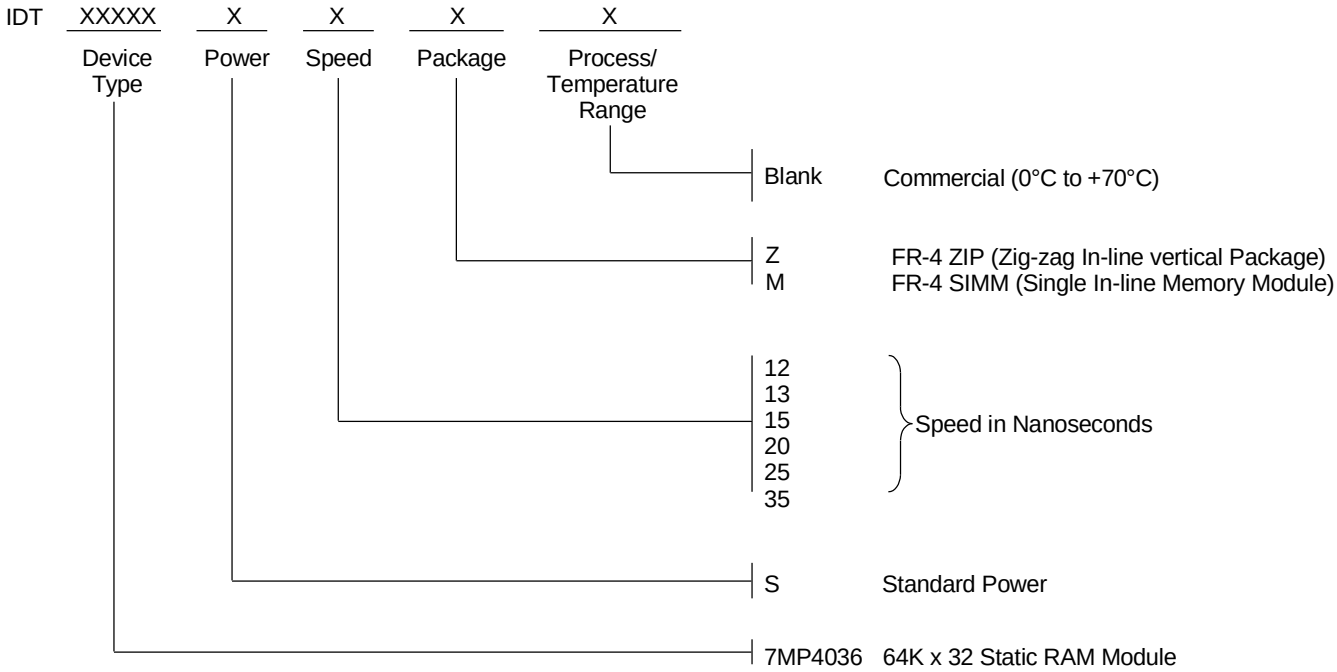
BACK VIEW

SIMM VERSION





Ordering Information



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