



## PROGRAMMABLE FLEXPC™ CLOCK FOR P4 PROCESSOR

**IDTCV115C**

### FEATURES:

- One high precision N and SSC programmable PLL for SRC/PCI
- One high precision N and SSC programmable PLL for CPU
- One high precision SSC programmable PLL for SATA
- One high precision PLL for 96MHz/48MHz
- Band-gap circuit for differential outputs
- Support multiple spread spectrum modulation, down and center
- Support SMBus block read/write, index read/write
- Selectable output strength for REF, PCI, and USB48MHz
- Available in SSOP package

### KEY SPECIFICATION:

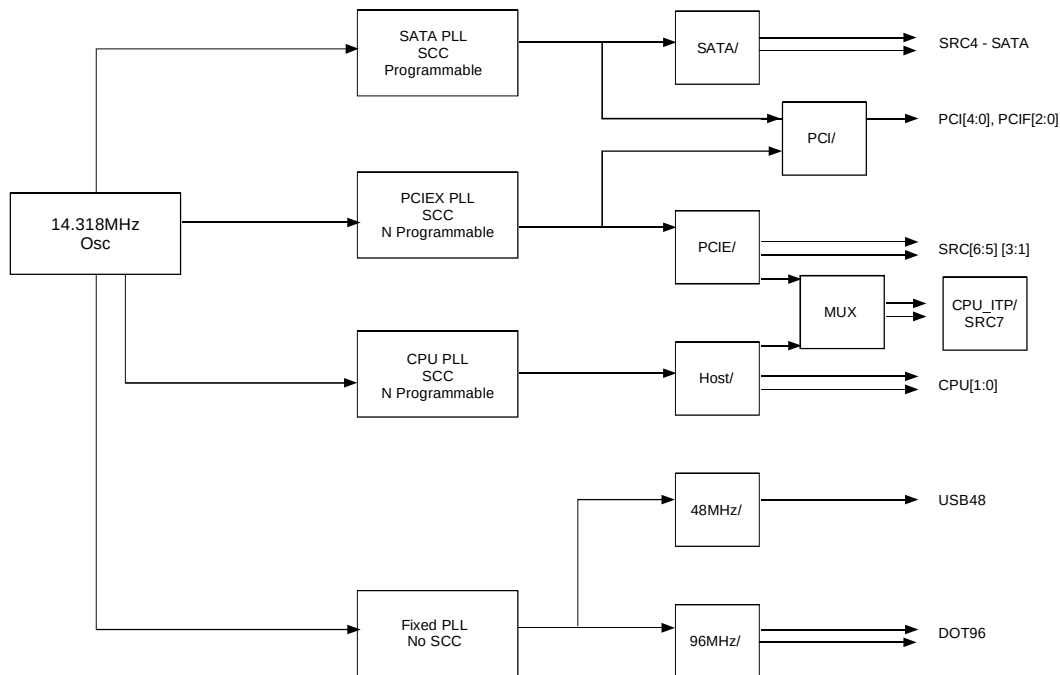
- CPU/SRC CLK cycle to cycle jitter < 85ps
- SATA CLK cycle to cycle jitter < 85ps
- Static PLL frequency divide error < 114 ppm
- Static PLL frequency divide error for 48MHz < 5 ppm

### DESCRIPTION:

IDTCV115C is a 56 pin clock device, complying the latest Intel CK410 requirements, for Intel advance P4 processors. The CPU output buffer is designed to support up to 400MHz processor. One dedicated PLL for Serial ATA clock provides high accuracy frequency. This device also implements Band-gap referenced I<sub>REF</sub> to reduce the impact of V<sub>DD</sub> variation on differential outputs, which can provide more robust system performance.

Each CPU/SRC/PCI, SATA clock has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

### FUNCTIONAL BLOCK DIAGRAM



### OUTPUT TABLE

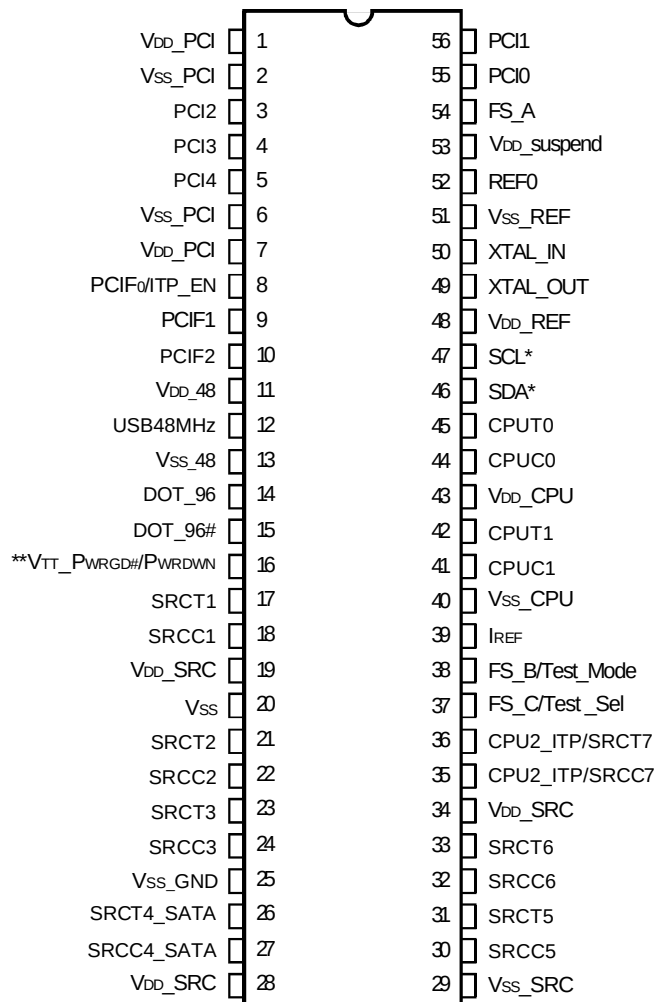
| CPU | CPU_ITP/SRC | SRC | SATA | PCI/PCIF | REF | DOT96 | 48MHz |
|-----|-------------|-----|------|----------|-----|-------|-------|
| 2   | 1           | 5   | 1    | 8        | 1   | 1     | 1     |

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COMMERCIAL TEMPERATURE RANGE

MAY 2004

## PIN CONFIGURATION



\* = ~ 130KΩ internal pull-up.

\*\* = ~ 130KΩ internal pull-down.

## SSOP TOP VIEW

## HW FREQUENCY SELECTION TABLE

| FSC, B, A | CPU     | SRC4_SATA | SRC[3:1], SCR[7:5] | PCI  | USB | DOT | REF    |
|-----------|---------|-----------|--------------------|------|-----|-----|--------|
| 101       | 100     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 001       | 133     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 011       | 166     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 010       | 200     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 000       | 266     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 100       | 333     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 110       | 400     | 100       | 100                | 33.3 | 48  | 96  | 14.318 |
| 111       | Reserve | 100       | 100                | 33.3 | 48  | 96  | 14.318 |

## TEST MODE SELECT<sup>(1)</sup>

If TEST\_SEL sampled above 2V at VTT\_PWRGD active LOW

| Pin38<br>(test_mode) | CPU   | SRC   | PCI/F | REF  | DOT96 | USB   |
|----------------------|-------|-------|-------|------|-------|-------|
| 1                    | REF/N | REF/N | REF/N | REF  | REF/N | REF/N |
| 0                    | Hi-Z  | Hi-Z  | Hi-Z  | Hi-Z | Hi-Z  | Hi-Z  |

### NOTE:

1. Once test clock operation has been invoked, TEST\_MODE pin will select between the Hi-Z and REF/N.

## ITP\_EN

| ITP_EN | pin 38    | pin 39    |
|--------|-----------|-----------|
| 1      | CPUC2_ITP | CPUC1_ITP |
| 0      | SRCC7     | SRCT7     |

## PIN DESCRIPTION

| Pin Number | Name                             | Type | Description                                                                                                                                                                                                                                       |
|------------|----------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | V <sub>DD</sub> _PCI             | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 2          | V <sub>SS</sub> _PCI             | GND  | GND                                                                                                                                                                                                                                               |
| 3          | PCI2                             | OUT  | PCI clock                                                                                                                                                                                                                                         |
| 4          | PCI3                             | OUT  | PCI clock                                                                                                                                                                                                                                         |
| 5          | PCI4                             | OUT  | PCI clock                                                                                                                                                                                                                                         |
| 6          | V <sub>SS</sub> _PCI             | GND  | GND                                                                                                                                                                                                                                               |
| 7          | V <sub>DD</sub> _PCI             | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 8          | PCIF0/ITP_EN                     | I/O  | PCI clock, free running. CPU_2 select (sampled at V <sub>TT</sub> _PWRGD# assertion), HIGH = CPU_2.                                                                                                                                               |
| 9          | PCIF1                            | OUT  | PCI clock,                                                                                                                                                                                                                                        |
| 10         | PCIF2                            | OUT  | PCI clock,                                                                                                                                                                                                                                        |
| 11         | V <sub>DD</sub> _48              | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 12         | USB48                            | OUT  | 48MHz clock                                                                                                                                                                                                                                       |
| 13         | V <sub>SS</sub> _48              | GND  | GND                                                                                                                                                                                                                                               |
| 14         | DOT_96T                          | OUT  | 96MHz 0.7V current mode differential clock output                                                                                                                                                                                                 |
| 15         | DOT_96C                          | OUT  | 96MHz 0.7V current mode differential clock output                                                                                                                                                                                                 |
| 16         | **V <sub>TT</sub> _PWRGD#/PWRDWN | I/O  | 3.3V LVTTTL input is a level-sensitive strobe used to latch the FS_A, FS_B, FS_C/TEST_SEL and PCIF_0/ITP_EN inputs. After V <sub>TT</sub> _PWRGD# assertion, becomes a real-time input for asserting power down (active high). Internal pull LOW. |
| 17         | SRCT1                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 18         | SRCC1                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 19         | V <sub>DD</sub> _SRC             | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 20         | V <sub>SS</sub>                  | GND  | GND                                                                                                                                                                                                                                               |
| 21         | SRCT2                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 22         | SRCC2                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 23         | SRCT3                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 24         | SRCC3                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 25         | V <sub>SS</sub>                  | GND  | GND                                                                                                                                                                                                                                               |
| 26         | SRCT4_SATA                       | OUT  | SATA clock                                                                                                                                                                                                                                        |
| 27         | SRCC4_SATA                       | OUT  | SATA clock                                                                                                                                                                                                                                        |
| 28         | V <sub>DD</sub> _SRC             | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 29         | V <sub>SS</sub> _SRC             | GND  | GND                                                                                                                                                                                                                                               |
| 30         | SRCC5                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 31         | SRCT5                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 32         | SRCC6                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 33         | SRCT6                            | OUT  | Differential Serial reference clock                                                                                                                                                                                                               |
| 34         | V <sub>DD</sub> _SRC             | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 35         | CPUC2_ITP/ SRCC7                 | OUT  | Selectable CPU or SRC differential clock output. ITP_EN=0 @ V <sub>TT</sub> _PWRGD# assertion = SRC_7                                                                                                                                             |
| 36         | CPUT2_ITP/ SRCT7                 | OUT  | Selectable CPU or SRC differential clock output. ITP_EN=0 @ V <sub>TT</sub> _PWRGD# assertion = SRC_7                                                                                                                                             |
| 37         | FS_C/Test_Sel                    | I/O  | CPU frequency selection. Selects test mode if pulled above 2V when V <sub>TT</sub> _PWRGD# is asserted.                                                                                                                                           |
| 38         | FS_B/Test_Mode                   | I/O  | CPU frequency selection. In test mode, 1=Hi-Z, 0=REF/N.                                                                                                                                                                                           |
| 39         | IREF                             | OUT  | Reference current for differential output buffer                                                                                                                                                                                                  |
| 40         | V <sub>SS</sub>                  | GND  | GND                                                                                                                                                                                                                                               |
| 41         | CPUC1                            | OUT  | Host 0.7V current mode differential clock output                                                                                                                                                                                                  |
| 42         | CPUT1                            | OUT  | Host 0.7V current mode differential clock output                                                                                                                                                                                                  |
| 43         | V <sub>DD</sub> _CPU             | PWR  | 3.3V                                                                                                                                                                                                                                              |
| 44         | CPUC0                            | OUT  | Host 0.7V current mode differential clock output                                                                                                                                                                                                  |
| 45         | CPUT0                            | OUT  | Host 0.7V current mode differential clock output                                                                                                                                                                                                  |
| 46         | *SDA                             | I/O  | SMBus data                                                                                                                                                                                                                                        |

## PIN DESCRIPTION (CONT.)

| Pin Number | Name                     | Type | Description                                                                                                           |
|------------|--------------------------|------|-----------------------------------------------------------------------------------------------------------------------|
| 47         | *SCL                     | IN   | SMBus CLK                                                                                                             |
| 48         | V <sub>DD</sub> _REF     | PWR  | 3.3V                                                                                                                  |
| 49         | XTAL_OUT                 | OUT  | Xtal output                                                                                                           |
| 50         | XTAL_IN                  | IN   | Xtal input                                                                                                            |
| 51         | V <sub>SS</sub> _REF     | GND  | GND                                                                                                                   |
| 52         | REF0                     | OUT  | 14.318 MHz reference clock output                                                                                     |
| 53         | V <sub>DD</sub> _Suspend | PWR  | In the power down mode, supply 3.3V to SM control registers, <1mA. In the normal operation, regular V <sub>DD</sub> . |
| 54         | FS_A                     | IN   | CPU frequency selection                                                                                               |
| 55         | PCI0                     | OUT  | PCI clock                                                                                                             |
| 56         | PCI1                     | OUT  | PCI clock                                                                                                             |

## SM PROTOCOL

### INDEX BLOCK WRITE PROTOCOL

| Bit   | # of bits | From   | Description                          |
|-------|-----------|--------|--------------------------------------|
| 1     | 1         | Master | Start                                |
| 2-9   | 8         | Master | D2h                                  |
| 10    | 1         | Slave  | Ack (Acknowledge)                    |
| 11-18 | 8         | Master | Register offset byte (starting byte) |
| 19    | 1         | Slave  | Ack (Acknowledge)                    |
| 20-27 | 8         | Master | Byte count, N, (0 is not valid)      |
| 28    | 1         | Slave  | Ack (Acknowledge)                    |
| 29-36 | 8         | Master | first data byte (Offset data byte)   |
| 37    | 1         | Slave  | Ack (Acknowledge)                    |
| 38-45 | 8         | Master | 2nd data byte                        |
| 46    | 1         | Slave  | Ack (Acknowledge)                    |
|       |           |        | :                                    |
|       |           | Master | Nth data byte                        |
|       |           | Slave  | Acknowledge                          |
|       |           | Master | Stop                                 |

### INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

| Bit   | # of bits | From   | Description                                        |
|-------|-----------|--------|----------------------------------------------------|
| 1     | 1         | Master | Start                                              |
| 2-9   | 8         | Master | D2h                                                |
| 10    | 1         | Slave  | Ack (Acknowledge)                                  |
| 11-18 | 8         | Master | Register offset byte (starting byte)               |
| 19    | 1         | Slave  | Ack (Acknowledge)                                  |
| 20    | 1         | Master | Repeated Start                                     |
| 21-28 | 8         | Master | D3h                                                |
| 29    | 1         | Slave  | Ack (Acknowledge)                                  |
| 30-37 | 8         | Slave  | Byte count, N (block read back of N bytes), Byte 8 |
| 38    | 1         | Master | Ack (Acknowledge)                                  |
| 39-46 | 8         | Slave  | first data byte (Offset data byte)                 |
| 47    | 1         | Master | Ack (Acknowledge)                                  |
| 48-55 | 8         | Slave  | 2nd data byte                                      |
|       |           |        | Ack (Acknowledge)                                  |
|       |           |        | :                                                  |
|       |           | Master | Ack (Acknowledge)                                  |
|       |           | Slave  | Nth data byte                                      |
|       |           |        | Not acknowledge                                    |
|       |           | Master | Stop                                               |

### INDEX BYTE WRITE

Setting bit[11:18]= starting address, bit[20:27]= 01h.

### INDEX BYTE READ

Setting bit[11:18]= starting address. After reading back the first data byte, master issues Stop bit.

## S.E. CLOCK STRENGTH SELECTION (PCI, REF, USB48)

| Str[1:0] |    | Multiple loads | Single loads | USB48     |
|----------|----|----------------|--------------|-----------|
| 00       | 2L | Recommend      |              | Recommend |
| 01       | 1H |                | Recommend    |           |
| 10       | 1L |                | Recommend    |           |
| 11       | 2H | Recommend      |              | Recommend |

## SSC MAGNITUDE CONTROL, SMC

| SMC[2:0] | %      |
|----------|--------|
| 000      | OFF    |
| 001      | -0.25  |
| 010      | -0.5   |
| 011      | ±0.125 |
| 100      | ±0.25  |
| 101      | ±0.375 |
| 110      | ±0.5   |
| 111      | ±0.75  |

## PCI

When Byte5 bit6 = 0; otherwise, PCI = SRC frequency/3

| PCIS[1:0] | PCI   |
|-----------|-------|
| 00        | 33.33 |
| 01        | 36.36 |
| 10        | 40    |
| 11        |       |

## S\_CBS[1:0], H\_CBS[1:0] BAND SELECTION

| S_CBS/H_CBS[1:0] |                                            |
|------------------|--------------------------------------------|
| 00               | FS[C,B,A]                                  |
| 01               | CB1_[2:0], byte17, CPU PLL Mode selection1 |
| 10               | CB2_[2:0], byte17, CPU PLL Mode selection2 |
| 11               | Don'tcare                                  |

## S\_CNS, S\_PNS, H\_CNS, H\_PNS N SELECTION

| NS[1:0] |                                  |
|---------|----------------------------------|
| 00      | Standard of Each CPU Mode (Band) |
| 01      | N Selection 1                    |
| 10      | N Selection 2                    |
| 11      | Don'tcare                        |

## RESOLUTION

|                   | N Resolution (MHz) | %     | N=  |
|-------------------|--------------------|-------|-----|
| CPU = 100MHz mode | 0.666667           | 0.67% | 150 |
| CPU = 133MHz mode | 0.888889           | 0.67% | 150 |
| CPU = 166MHz mode | 1.333333           | 0.8%  | 125 |
| CPU = 200MHz mode | 1.333333           | 0.67% | 150 |
| CPU = 266MHz mode | 2.666667           | 1.00% | 100 |
| CPU = 333MHz mode | 2.666667           | 0.8%  | 125 |
| CPU = 400MHz mode | 2.666667           | 0.67% | 150 |
| SRC (PCI Express) | 0.666667           | 0.67% | 150 |

## CB1[2:0]. CB2[2:0], CPU MODE SELECTION

| CB[2:0] | CPU Mode, MHz |
|---------|---------------|
| 101     | 100           |
| 001     | 133           |
| 011     | 166           |
| 010     | 200           |
| 000     | 266           |
| 100     | 333           |
| 110     | 400           |
| 111     | Reserve       |

## BYTE 0

| Bit | Output(s) Affected            | Description/Function | 0        | 1      | Type | Power On |
|-----|-------------------------------|----------------------|----------|--------|------|----------|
| 7   | CPUT2, CPUC2/<br>SRCT7, SRCC7 | Output enable        | Tristate | Enable | RW   | 1        |
| 6   | SRCT6, SRCC6                  | Output enable        | Tristate | Enable | RW   | 1        |
| 5   | SRCT5, SRCC5                  | Output enable        | Tristate | Enable | RW   | 1        |
| 4   | SRCT4, SRCC4 (SATA)           | Output enable        | Tristate | Enable | RW   | 1        |
| 3   | SRCT3, SRCC3                  | Output enable        | Tristate | Enable | RW   | 1        |
| 2   | SRCT2, SRCC2                  | Output enable        | Tristate | Enable | RW   | 1        |
| 1   | SRCT1, SRCC1                  | Output enable        | Tristate | Enable | RW   | 1        |
| 0   | REF0 2x drive                 | 2x drive enable      | 1x       | 2x     | RW   | 1        |

## BYTE 1

| Bit | Output(s) Affected | Description/Function | 0        | 1      | Type | Power On | Recommended |
|-----|--------------------|----------------------|----------|--------|------|----------|-------------|
| 7   | DOT96T, DOT96C     | Output enable        | Tristate | Enable | RW   | 1        |             |
| 6   | Reserve            | Output enable        | Tristate | Enable | RW   | 1        | 0           |
| 5   | USB48              | Output enable        | Tristate | Enable | RW   | 1        |             |
| 4   | Reserve            | Output enable        | Tristate | Enable | RW   | 0        | 0           |
| 3   | REF0               | Output enable        | Tristate | Enable | RW   | 1        |             |
| 2   | CPUT1, CPUC1       | Output enable        | Tristate | Enable | RW   | 1        |             |
| 1   | CPUT0, CPUC0       | Output enable        | Tristate | Enable | RW   | 1        |             |
| 0   | Reserve            | Output enable        | Tristate | Enable | RW   | 0        | 0           |

## BYTE 2

| Bit | Output(s) Affected | Description/Function | 0        | 1      | Type | Power On |
|-----|--------------------|----------------------|----------|--------|------|----------|
| 7   | PCI4               | Output enable        | Tristate | Enable | RW   | 1        |
| 6   | PCI3               | Output enable        | Tristate | Enable | RW   | 1        |
| 5   | PCI2               | Output enable        | Tristate | Enable | RW   | 1        |
| 4   | PCI1               | Output enable        | Tristate | Enable | RW   | 1        |
| 3   | PCI0               | Output enable        | Tristate | Enable | RW   | 1        |
| 2   | PCIF2              | Output enable        | Tristate | Enable | RW   | 1        |
| 1   | PCIF1              | Output enable        | Tristate | Enable | RW   | 1        |
| 0   | PCIF0              | Output enable        | Tristate | Enable | RW   | 1        |

## BYTE 3

| Bit | Output(s) Affected | Description / Function        | 0                    | 1                      | Type | Power On |
|-----|--------------------|-------------------------------|----------------------|------------------------|------|----------|
| 7   |                    | FSC latched value on power up |                      |                        | R    |          |
| 6   |                    | FSB latched value on power up |                      |                        | R    |          |
| 5   |                    | FSA latched value on power up |                      |                        | R    |          |
| 4   | SRCT[7:1]          | SRCT PWRDWN drive mode        | Driven in power down | Tristate in power down | RW   | 0        |
| 3   | CPUT2              | CPUT2 PWRDWN drive mode       | Driven in power down | Tristate in power down | RW   | 0        |
| 2   | CPUT1              | CPUT1 PWRDWN drive mode       | Driven in power down | Tristate in power down | RW   | 0        |
| 1   | CPUT0              | CPUT0 PWRDWN drive mode       | Driven in power down | Tristate in power down | RW   | 0        |
| 0   | DOT96T             | DOT96 PWRDWN drive mode       | Driven in power down | Tristate               | RW   | 0        |

## BYTE 4

| Bit | Output(s) Affected | Description / Function       | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------------|---|---|------|----------|
| 7   | PCIFStr1           | PCIF strength selection      |   |   |      | 0        |
| 6   | PCIFStr0           | see SE Clock Strength table  |   |   |      | 0        |
| 5   | PCIStr1            | PCI strength selection       |   |   |      | 0        |
| 4   | PCIStr0            | see SE Clock Strength table  |   |   |      | 1        |
| 3   | REFStr1            | REF strength selection       |   |   |      | 0        |
| 2   | REFStr0            | see SE Clock Strength table  |   |   |      | 0        |
| 1   | 48MHStr1           | USB48MHz0 strength selection |   |   |      | 1        |
| 0   | 48MHzStr0          | see SE Clock Strength table  |   |   |      | 1        |

## BYTE 5

| Bit | Output(s) Affected                            | Description / Function                                         | 0                   | 1                          | Type | Power On |
|-----|-----------------------------------------------|----------------------------------------------------------------|---------------------|----------------------------|------|----------|
| 7   |                                               |                                                                |                     |                            |      |          |
| 6   | PCIPLLS                                       | PCI PLL select                                                 | SATA PLL            | PCI EX PLL                 | RW   | 0        |
| 5   | PCIS1                                         | See PCIS table, only valid when Byte5 bit 6 = 0 See PCIS Table |                     |                            | RW   | 0        |
| 4   | PCIS0                                         |                                                                |                     |                            | RW   | 0        |
| 3   | SM control registers contents Power Down mode | During the Power Down                                          | Reset SM to default | SM contents have no change | RW   | 1        |
| 2   | SATA_SMC2                                     | SATA PLL spread spectrum                                       |                     |                            | RW   | 0        |
| 1   | SATA_SMC1                                     | magnitude control select                                       |                     |                            | RW   | 1        |
| 0   | SATA_SMC0                                     | see SMC table                                                  |                     |                            | RW   | 0        |

## BYTE 6

| Bit | Output(s) Affected | Description / Function                        | 0 | 1 | Type | Power On |
|-----|--------------------|-----------------------------------------------|---|---|------|----------|
| 7   | WDHRB              | Hard Alarm read back, reset by WD disable     |   |   | R    |          |
| 6   | WDSRB              | Soft Alarm read back, rest by WD disable      |   |   | R    |          |
| 5   | SRC_SMC2           | SRC(PCIExpress) PLL spread spectrum magnitude |   |   | RW   | 0        |
| 4   | SRC_SMC1           | control select see SMC table                  |   |   | RW   | 1        |
| 3   | SRC_SMC0           |                                               |   |   | RW   | 0        |
| 2   | CPU_SMC2           | CPU PLL spread spectrum                       |   |   | RW   | 1        |
| 1   | CPU_SMC1           | control magnitude select                      |   |   | RW   | 0        |
| 0   | CPU_SMC0           | see SMC table                                 |   |   | RW   | 0        |

## BYTE 7

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7   |                    | Revision ID            |   |   |      | 0        |
| 6   |                    | Revision ID            |   |   |      | 0        |
| 5   |                    | Revision ID            |   |   |      | 0        |
| 4   |                    | Revision ID            |   |   |      | 0        |
| 3   |                    | Vendor ID              |   |   |      | 0        |
| 2   |                    | Vendor ID              |   |   |      | 1        |
| 1   |                    | Vendor ID              |   |   |      | 0        |
| 0   |                    | Vendor ID              |   |   |      | 1        |

## BYTE 8

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7   |                    |                        |   |   | RW   | 0        |
| 6   |                    |                        |   |   | RW   | 0        |
| 5   |                    |                        |   |   | RW   | 0        |
| 4   |                    |                        |   |   | RW   | 0        |
| 3   |                    |                        |   |   | RW   | 1        |
| 2   |                    |                        |   |   | RW   | 1        |
| 1   |                    |                        |   |   | RW   | 1        |
| 0   |                    |                        |   |   | RW   | 1        |

BYTES 9 - 16 ARE DUMMY BITES

## BYTE 17

| Bit | Output(s) Affected | Description / Function                                   | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------------------------------------------|---|---|------|----------|
| 7   | CB1_2              | CPU PLL Mode Selection 1<br>See CPU Mode Selection table |   |   | RW   | 0        |
| 6   | CB1_1              |                                                          |   |   | RW   | 0        |
| 5   | CB1_0              |                                                          |   |   | RW   | 0        |
| 4   |                    |                                                          |   |   | RW   |          |
| 3   | CB2_2              | CPU PLL Mode Selection 2<br>See CPU Mode Selection table |   |   | RW   | 0        |
| 2   | CB2_1              |                                                          |   |   | RW   | 0        |
| 1   | CB2_0              |                                                          |   |   | RW   | 0        |
| 0   | CN1_8, MSB         | CPU PLL N selection 1                                    |   |   | RW   | 0        |

## BYTE 18

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7   | CN1_7              | CPU PLL N selection 1  |   |   | RW   | 1        |
| 6   | CN1_6              |                        |   |   | RW   | 0        |
| 5   | CN1_5              |                        |   |   | RW   | 0        |
| 4   | CN1_4              |                        |   |   | RW   | 1        |
| 3   | CN1_3              |                        |   |   | RW   | 0        |
| 2   | CN1_2              |                        |   |   | RW   | 1        |
| 1   | CN1_1              |                        |   |   | RW   | 1        |
| 0   | CN1_0, LSB         |                        |   |   | RW   | 0        |



## BYTE 19

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7   | CN2_8, MSB         | CPU N selection 2      |   |   |      | 0        |
| 6   | CN2_7              |                        |   |   |      | 1        |
| 5   | CN2_6              |                        |   |   |      | 0        |
| 4   | CN2_5              |                        |   |   |      | 0        |
| 3   | CN2_4              |                        |   |   |      | 1        |
| 2   | CN2_3              |                        |   |   |      | 0        |
| 1   | CN2_2              |                        |   |   |      | 1        |
| 0   | CN2_1              |                        |   |   |      | 1        |

## BYTE 20

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7   | CN2_0, LSB         | CPU N selection 2      |   |   |      | 0        |
| 6   |                    |                        |   |   |      |          |
| 5   |                    |                        |   |   |      |          |
| 4   |                    |                        |   |   |      |          |
| 3   |                    |                        |   |   |      |          |
| 2   |                    |                        |   |   |      |          |
| 1   | PN1_8, MSB         |                        |   |   | RW   | 0        |
| 0   | PN1_7              |                        |   |   | RW   | 1        |

## BYTE 21

| Bit | Output(s) Affected | Description / Function                 | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------------------------|---|---|------|----------|
| 7   | PN1_6              | SRC PLL (PCI Express)<br>N Selection 1 |   |   | RW   | 0        |
| 6   | PN1_5              |                                        |   |   | RW   | 0        |
| 5   | PN1_4              |                                        |   |   | RW   | 1        |
| 4   | PN1_3              |                                        |   |   | RW   | 0        |
| 3   | PN1_2              |                                        |   |   | RW   | 1        |
| 2   | PN1_1              |                                        |   |   | RW   | 1        |
| 1   | PN1_0, LSB         |                                        |   |   | RW   | 0        |
| 0   | PN2_8, MSB         |                                        |   |   | RW   | 0        |

## BYTE 22

| Bit | Output(s) Affected | Description / Function                 | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------------------------|---|---|------|----------|
| 7   | PN2_7              | SRC PLL (PCI Express)<br>N Selection 2 |   |   | RW   | 1        |
| 6   | PN2_6              |                                        |   |   | RW   | 0        |
| 5   | PN2_5              |                                        |   |   | RW   | 0        |
| 4   | PN2_4              |                                        |   |   | RW   | 1        |
| 3   | PN2_3              |                                        |   |   | RW   | 0        |
| 2   | PN2_2              |                                        |   |   | RW   | 1        |
| 1   | PN2_1              |                                        |   |   | RW   | 1        |
| 0   | PN2_0, LSB         |                                        |   |   | RW   | 0        |

## BYTE 23

| Bit | Output(s) Affected | Description / Function                                                 | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------------------------------------------------------|---|---|------|----------|
| 7   | S_CBS1             | Soft Alarm CPU PLL mode select, see S_CBS Band Selection Table         |   |   | RW   | 0        |
| 6   | S_CBS0             |                                                                        |   |   | RW   | 0        |
| 5   | S_CNS1             | Soft Alarm CPU PLL N select, see S_CNS N Selection Table               |   |   | RW   | 0        |
| 4   | S_CNS0             |                                                                        |   |   | RW   | 0        |
| 3   | S_PNS1             | Soft Alarm SRC PLL (PCI Express) N select, see S_PNS N Selection Table |   |   | RW   | 0        |
| 2   | S_PNS0             |                                                                        |   |   | RW   | 0        |
| 1   |                    |                                                                        |   |   |      |          |
| 0   |                    |                                                                        |   |   |      |          |

## BYTE 24

| Bit | Output(s) Affected | Description / Function                                                 | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------------------------------------------------------|---|---|------|----------|
| 7   | H_CBS1             | Hard Alarm CPU PLL mode select, see H_CBS Band Selection Table         |   |   | RW   | 0        |
| 6   | H_CBS0             |                                                                        |   |   | RW   | 0        |
| 5   | H_CNS2             | Hard Alarm CPU PLL N select, see H_CNS N Selection Table               |   |   | RW   | 0        |
| 4   | H_CNS0             |                                                                        |   |   | RW   | 0        |
| 3   | H_PNS1             | Hard Alarm SRC PLL (PCI Express) N select, see H_PNS N selection table |   |   | RW   | 0        |
| 2   | H_PNS0             |                                                                        |   |   | RW   | 0        |
| 1   |                    |                                                                        |   |   |      |          |
| 0   |                    |                                                                        |   |   |      |          |

## BYTE 25

| Bit | Output(s) Affected | Description / Function                                                 | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------------------------------------------------------|---|---|------|----------|
| 7   | WD Timer 7         | Watchdog timer<br>Default is 11*290ms<br>Hard Alarm = WD timer * 290ms |   |   | RW   | 0        |
| 6   | WD Timer 6         |                                                                        |   |   | RW   | 0        |
| 5   | WD Timer 5         |                                                                        |   |   | RW   | 0        |
| 4   | WD Timer 4         |                                                                        |   |   | RW   | 0        |
| 3   | WD Timer 3         |                                                                        |   |   | RW   | 1        |
| 2   | WD Timer 2         |                                                                        |   |   | RW   | 0        |
| 1   | WD Timer 1         |                                                                        |   |   | RW   | 1        |
| 0   | WD Timer 0         |                                                                        |   |   | RW   | 1        |

## BYTE 26

| Bit | Output(s) Affected | Description / Function                              | 0 | 1 | Type | Power On |
|-----|--------------------|-----------------------------------------------------|---|---|------|----------|
| 7   |                    |                                                     |   |   | RW   |          |
| 6   |                    |                                                     |   |   | RW   |          |
| 5   |                    |                                                     |   |   | RW   |          |
| 4   |                    |                                                     |   |   | RW   |          |
| 3   | Soft Timer 3       | Soft Alarm timer<br>Soft Alarm = Soft timer * 290ms |   |   | RW   | 0        |
| 2   | Soft Timer 2       |                                                     |   |   | RW   | 0        |
| 1   | Soft Timer 1       |                                                     |   |   | RW   | 0        |
| 0   | Soft Timer 0       |                                                     |   |   | RW   | 1        |

## BYTE 27

| Bit | Output(s) Affected              | Description / Function               | 0       | 1       | Type | Power On |
|-----|---------------------------------|--------------------------------------|---------|---------|------|----------|
| 7   | Watch Dog Enable                | Watch Dog Enable                     | Disable | Enable  | RW   | 0        |
| 6   |                                 |                                      |         |         |      |          |
| 5   | Soft Alarm Enable               | Soft Alarm Enable                    | Disable | Enable  | RW   | 0        |
| 4   | Reserved                        |                                      |         |         | RW   | 0        |
| 3   | Hard Alarm Enable               | Hard Alarm Enable                    | Disable | Enable  | RW   | 0        |
| 2   | Reserved                        |                                      |         |         | RW   | 0        |
| 1   | Hard Alarm FS<br>Relatch Enable | Relatch FS[C, B, A]<br>at Hard Alarm | Disable | Relatch | RW   | 0        |
| 0   | Reserved                        |                                      |         |         | RW   | 0        |

BYTE 42, 43 SRC SPREAD MAGNITUDE <sup>(1)</sup>

BYTE 44 SRC SPREAD CENTER <sup>(1)</sup>

BYTE 38 SRC SPREAD CONTROL SWITCH (FROM BYTE 6 TO BYTES 42, 43, 44) <sup>(1)</sup>

**NOTE:**

1. Contact IDT for detailed application note.

## PLL FREQUENCY PROGRAMMING PROCEDURES

The user changes PLL frequency through Soft Alarm or Hard Alarm. The Watch Dog circuit has to be enabled. Based on their application, the user may enable either one or both of the alarms.

User presets the CPU PLL Mode and N, and SRC PLL N value:

1. Set CPU PLL Mode, CB1 and CB2, byte 17
2. Set CPU PLL N, CN1 and CN2, byte 18 and byte 19
3. Set SRC (PCI Express) PLL N, PN1 and PN2, byte 21, 22

User selects the frequency for Soft Alarm and Hard Alarm, if enabled respectively:

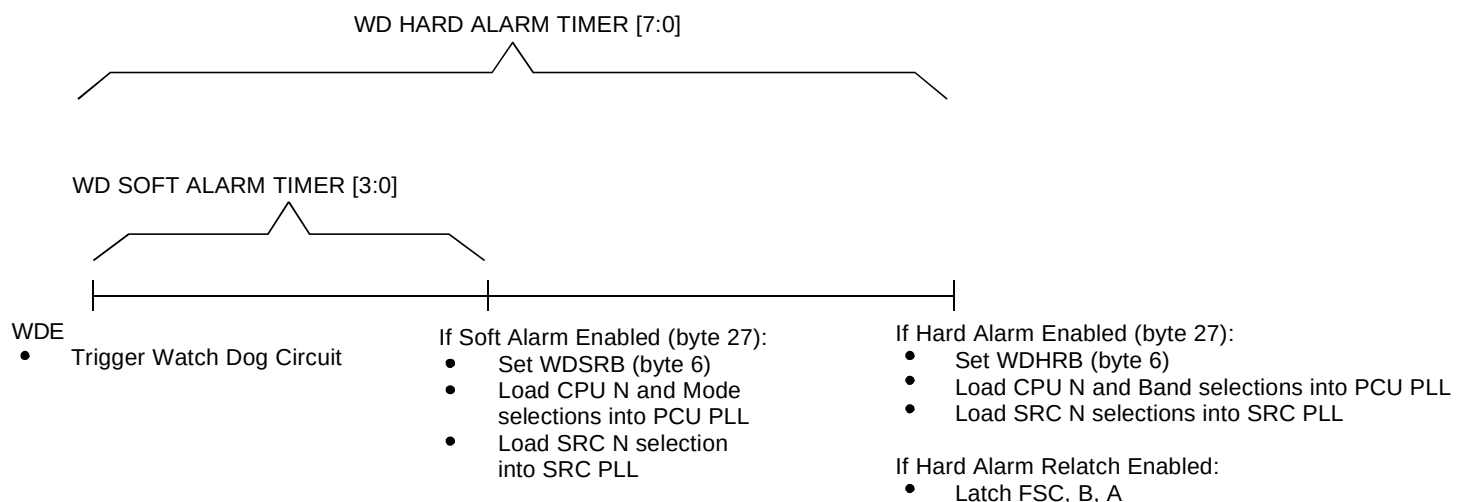
4. Select Soft Alarm frequency, byte 23
5. Select Hard Alarm frequency, byte 24

User sets the Timer and enables the WD circuit for frequency switch:

6. Set Hard Alarm Timer, byte 25
7. Set Soft Alarm Timer, byte 26
8. Enable Soft and Hard Alarm, byte 27
9. Enable Watch Dog (WDE), byte 27

- WDE Disable resets WDSRB and WDHRB.
- PCI CLK is selectable from SRC PLL or SATA PLL, byte 5 bit 6. If from SRC PLL, PCI frequency = 1/3 of SRC frequency. If from SATA, PCI is fixed to 3 selections, 33MHz, 36MHz and 40MHz, byte 5 bit[5:4].

## WD SOFT AND HARD ALARM/TIME OUT OPERATION



## ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$

| Symbol        | Parameter                            | Test Conditions                                              | Min.           | Typ.     | Max.           | Unit |
|---------------|--------------------------------------|--------------------------------------------------------------|----------------|----------|----------------|------|
| $V_{IH}$      | Input HIGH Voltage                   | $3.3\text{V} \pm 5\%$                                        | 2              | —        | $V_{DD} + 0.3$ | V    |
| $V_{IL}$      | Input LOW Voltage                    | $3.3\text{V} \pm 5\%$                                        | $V_{SS} - 0.3$ | —        | 0.8            | V    |
| $V_{IH\_FS}$  | FS Input HIGH Voltage                | For FSA,B,C and Test_Mode                                    | 0.7            | —        | $V_{DD} + 0.3$ | V    |
| $V_{IL\_FS}$  | FS Input LOW Voltage                 | For FSA,B,C and Test_Mode                                    | $V_{SS} - 0.3$ | —        | 0.35           | V    |
| $I_{IL}$      | Input Leakage Current                | $0 < V_{IN} < V_{DD}$ , no internal pull-up or pull-down     | -5             | —        | +5             | mA   |
| $I_{DD3.3OP}$ | Operating Supply Current             | Full active, $C_L$ = full load                               | —              | —        | 400            | mA   |
| $I_{DD3.3PD}$ | Powerdown Current                    | All differential pairs driven                                | —              | —        | 70             | mA   |
|               |                                      | All differential pairs tri-stated                            | —              | —        | 12             |      |
| $F_I$         | Input Frequency <sup>(1)</sup>       | $V_{DD} = 3.3\text{V}$                                       | —              | 14.31818 | —              | MHz  |
| $L_{PIN}$     | Pin Inductance <sup>(2)</sup>        |                                                              | —              | —        | 7              | nH   |
| $C_{IN}$      | Input Capacitance <sup>(2)</sup>     | Logic inputs                                                 | —              | —        | 5              | pF   |
| $C_{OUT}$     |                                      | Output pin capacitance                                       | —              | —        | 6              |      |
| $C_{INX}$     |                                      | X1 and X2 pins                                               | —              | —        | 5              |      |
| $T_{STAB}$    | Clock Stabilization <sup>(2,3)</sup> | From $V_{DD}$ power-up or de-assertion of PD# to first clock | —              | —        | 1.8            | ms   |
|               | Modulation Frequency <sup>(2)</sup>  | Triangular modulation                                        | 30             | —        | 33             | KHz  |
|               | $T_{DRIVE\_SRC}^{(2)}$               | SRC output enable after PCI_Stop# de-assertion               | —              | —        | 15             | ns   |
|               | $T_{DRIVE\_PD\#}^{(2)}$              | CPU output enable after PD# de-assertion                     | —              | —        | 300            | us   |
|               | $T_{FALL\_PD\#}^{(2)}$               | Fall time of PD#                                             | —              | —        | 5              | ns   |
|               | $T_{RISE\_PD\#}^{(3)}$               | Rise time of PD#                                             | —              | —        | 5              | ns   |
|               | $T_{DRIVE\_CPU\_Stop\#}^{(2)}$       | CPU output enable after CPU_Stop# de-assertion               | —              | —        | 10             | us   |
|               | $T_{FALL\_CPU\_Stop\#}^{(2)}$        | Fall time of PD#                                             | —              | —        | 5              | ns   |
|               | $T_{RISE\_CPU\_Stop\#}^{(3)}$        | Rise time of PD#                                             | —              | —        | 5              | ns   |

### NOTES:

- Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
- This parameter is guaranteed by design, but not 100% production tested.
- See TIMING DIAGRAMS for timing requirements.

# ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C, Supply Voltage: VDD = 3.3V ± 5%; CL = 2pF

| Symbol      | Parameter                                      | Test Conditions                                                                 | Min.    | Typ. | Max.    | Unit |
|-------------|------------------------------------------------|---------------------------------------------------------------------------------|---------|------|---------|------|
| ZO          | Current Source Output Impedance <sup>(2)</sup> | VO = Vx                                                                         | 3000    | —    | —       | Ω    |
| VOH3        | Output HIGH Voltage                            | IOH = -1mA                                                                      | 2.4     | —    | —       | V    |
| VOL3        | Output LOW Voltage                             | IOL = 1mA                                                                       | —       | —    | 0.4     | V    |
| VHIGH       | Voltage HIGH <sup>(2)</sup>                    | Statistical measurement on single-ended signal using oscilloscope math function | 660     | —    | 850     | mV   |
| VLOW        | Voltage LOW <sup>(2)</sup>                     |                                                                                 | -150    | —    | 150     |      |
| VOVS        | Max Voltage <sup>(2)</sup>                     | Measurement on single-ended signal using absolute value                         | —       | —    | 1150    | mV   |
| VUDS        | Min Voltage <sup>(2)</sup>                     |                                                                                 | -300    | —    | —       |      |
| VCROSS(ABS) | Crossing Voltage (abs) <sup>(2)</sup>          |                                                                                 | 250     | —    | 550     | mV   |
| d - VCROSS  | Crossing Voltage (var) <sup>(2)</sup>          | Variation of crossing over all edges                                            | —       | —    | 140     | mV   |
| ppm         | Long Accuracy <sup>(2,3)</sup>                 | See TPERIOD Min. - Max. values                                                  | -300    | —    | 300     | ppm  |
| TPERIOD     | Average Period <sup>(3)</sup>                  | 400MHz nominal/spread                                                           | 2.4993  | —    | 2.5008  | ns   |
|             |                                                | 333.33MHz nominal/spread                                                        | 2.9991  | —    | 3.0009  |      |
|             |                                                | 266.66MHz nominal/spread                                                        | 3.7489  | —    | 3.7511  |      |
|             |                                                | 200MHz nominal/spread                                                           | 4.9985  | —    | 5.0015  |      |
|             |                                                | 166.66MHz nominal/spread                                                        | 5.9982  | —    | 6.0018  |      |
|             |                                                | 133.33MHz nominal/spread                                                        | 7.4978  | —    | 7.5023  |      |
|             |                                                | 100MHz nominal/spread                                                           | 9.997   | —    | 10.003  |      |
|             |                                                | 96MHz nominal                                                                   | 10.4135 | —    | 10.4198 |      |
| TABSMIN     | Absolute Min Period <sup>(2,3)</sup>           | 400MHz nominal/spread                                                           | 2.4143  | —    | —       | ns   |
|             |                                                | 333.33MHz nominal/spread                                                        | 2.9141  | —    | —       |      |
|             |                                                | 266.66MHz nominal/spread                                                        | 3.6639  | —    | —       |      |
|             |                                                | 200MHz nominal/spread                                                           | 4.9135  | —    | —       |      |
|             |                                                | 166.66MHz nominal/spread                                                        | 5.9132  | —    | —       |      |
|             |                                                | 133.33MHz nominal/spread                                                        | 7.4128  | —    | —       |      |
|             |                                                | 100MHz nominal/spread                                                           | 9.912   | —    | —       |      |
|             |                                                | 96MHz nominal                                                                   | 10.1635 | —    | —       |      |
| tr          | Rise Time <sup>(2)</sup>                       | VOL = 0.175V, VOH = 0.525V                                                      | 175     | —    | 700     | ps   |
| tf          | Fall Time <sup>(2)</sup>                       | VOL = 0.175V, VOH = 0.525V                                                      | 175     | —    | 700     | ps   |
| d-tr        | Rise Time Variation <sup>(2)</sup>             |                                                                                 | —       | —    | 125     | ps   |
| d-tf        | Fall Time Variation <sup>(2)</sup>             |                                                                                 | —       | —    | 125     | ps   |
| dt3         | Duty Cycle <sup>(2)</sup>                      | Measurement from differential waveform                                          | 45      | —    | 55      | %    |
| tsk3        | Skew <sup>(2)</sup>                            | VT = 50%                                                                        | —       | —    | 100     | ps   |
| tCYC-CYC    | Jitter, Cycle to Cycle <sup>(2)</sup>          | Measurement from differential waveform                                          | —       | —    | 85      | ps   |

## NOTES:

- SRC clock outputs run only at 100MHz or 200MHz. Specs for 133.33 and 166.66 do not apply to SRC clock pair.
- This parameter is guaranteed by design, but not 100% production tested.
- All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

## ELECTRICAL CHARACTERISTICS - PCICK / PCICK\_F

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10 - 30\text{pF}$

| Symbol   | Parameter                      | Test Conditions                                 | Min.   | Typ. | Max.    | Unit |
|----------|--------------------------------|-------------------------------------------------|--------|------|---------|------|
| ppm      | Long Accuracy <sup>(1,2)</sup> | See Tperiod Min. - Max. values                  | —      | —    | 300     | ppm  |
| TPERIOD  | Clock Period <sup>(2)</sup>    | 33.33MHz output nominal                         | 29.991 | —    | 30.009  | ns   |
|          |                                | 33.33MHz output spread                          | 29.991 | —    | 30.1598 |      |
| VOH      | Output HIGH Voltage            | $I_{OH} = -1\text{mA}$                          | 2.4    | —    | —       | V    |
| VOL      | Output LOW Voltage             | $I_{OL} = 1\text{mA}$                           | —      | —    | 0.55    | V    |
| IOH      | Output HIGH Current            | $V_{OH}$ at Min. = 1V                           | -33    | —    | —       | mA   |
|          |                                | $V_{OH}$ at Max. = 3.135V                       | —      | —    | -33     |      |
| IOL      | Output LOW Current             | $V_{OL}$ at Min. = 1.95V                        | 30     | —    | —       | mA   |
|          |                                | $V_{OL}$ at Max. = 0.4V                         | —      | —    | 38      |      |
|          | Edge Rate <sup>(1)</sup>       | Rising edge rate                                | 1      | —    | 4       | V/ns |
|          | Edge Rate <sup>(1)</sup>       | Falling edge rate                               | 1      | —    | 4       | V/ns |
| tr1      | Rise Time <sup>(1)</sup>       | $V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ | 0.5    | —    | 2       | ns   |
| tf1      | Fall Time <sup>(1)</sup>       | $V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ | 0.5    | —    | 2       | ns   |
| dt1      | Duty Cycle <sup>(1)</sup>      | $V_T = 1.5\text{V}$                             | 45     | —    | 55      | %    |
| tsk1     | Skew <sup>(1)</sup>            | $V_T = 1.5\text{V}$                             | —      | —    | 500     | ps   |
| tCYC-CYC | Jitter <sup>(1)</sup>          | $V_T = 1.5\text{V}$                             | —      | —    | 250     | ps   |

### NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

## ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10 - 20\text{pF}$

| Symbol  | Parameter                      | Test Conditions                                 | Min.    | Typ. | Max.   | Unit |
|---------|--------------------------------|-------------------------------------------------|---------|------|--------|------|
| ppm     | Long Accuracy <sup>(1,2)</sup> | See Tperiod Min. - Max. values                  | —       | —    | 300    | ppm  |
| TPERIOD | Clock Period <sup>(2)</sup>    | 48MHz output nominal                            | 20.8257 | —    | 20.834 | ns   |
| VOH     | Output HIGH Voltage            | $I_{OH} = -1\text{mA}$                          | 2.4     | —    | —      | V    |
| VOL     | Output LOW Voltage             | $I_{OL} = 1\text{mA}$                           | —       | —    | 0.55   | V    |
| IOH     | Output HIGH Current            | $V_{OH}$ at Min. = 1V                           | -29     | —    | —      | mA   |
|         |                                | $V_{OH}$ at Max. = 3.135V                       | —       | —    | -23    |      |
| IOL     | Output LOW Current             | $V_{OL}$ at Min. = 1.95V                        | 29      | —    | —      | mA   |
|         |                                | $V_{OL}$ at Max. = 0.4V                         | —       | —    | 27     |      |
|         | Edge Rate <sup>(1)</sup>       | Rising edge rate                                | 1       | —    | 2      | V/ns |
|         | Edge Rate <sup>(1)</sup>       | Falling edge rate                               | 1       | —    | 2      | V/ns |
| tr1     | Rise Time <sup>(1)</sup>       | $V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ | 1       | —    | 2      | ns   |
| tf1     | Fall Time <sup>(1)</sup>       | $V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ | 1       | —    | 2      | ns   |
| dt1     | Duty Cycle <sup>(1)</sup>      | $V_T = 1.5\text{V}$                             | 45      | —    | 55     | %    |

### NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

## ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10 - 20\text{pF}$

| Symbol   | Parameter                          | Test Conditions                                   | Min.   | Typ. | Max.   | Unit |
|----------|------------------------------------|---------------------------------------------------|--------|------|--------|------|
| ppm      | Long Accuracy <sup>(1)</sup>       | See Tperiod Min. - Max. values                    | —      | —    | 300    | ppm  |
| TPERIOD  | Clock Period                       | 14.318MHz output nominal                          | 69.827 | —    | 69.855 | ns   |
| VOH      | Output HIGH Voltage <sup>(1)</sup> | $I_{OH} = -1\text{mA}$                            | 2.4    | —    | —      | V    |
| VOL      | Output LOW Voltage <sup>(1)</sup>  | $I_{OL} = 1\text{mA}$                             | —      | —    | 0.4    | V    |
| IOH      | Output HIGH Current <sup>(1)</sup> | $V_{OH}$ at Min. = 1V, $V_{OH}$ at Max. = 3.135V  | -33    | —    | -33    | mA   |
| IOL      | Output LOW Current <sup>(1)</sup>  | $V_{OL}$ at Min. = 1.95V, $V_{OL}$ at Max. = 0.4V | 30     | —    | 38     | mA   |
| tR1      | Rise Time <sup>(1)</sup>           | $V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$   | 1      | —    | 2      | ns   |
| tF1      | Fall Time <sup>(1)</sup>           | $V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$   | 1      | —    | 2      | ns   |
| tsk1     | Skew <sup>(1)</sup>                | $V_T = 1.5\text{V}$                               | —      | —    | 500    | ps   |
| dT1      | Duty Cycle <sup>(1)</sup>          | $V_T = 1.5\text{V}$                               | 45     | —    | 55     | %    |
| tCYC-CYC | Jitter <sup>(1)</sup>              | $V_T = 1.5\text{V}$                               | —      | —    | 1000   | ps   |

**NOTE:**

1. This parameter is guaranteed by design, but not 100% production tested.

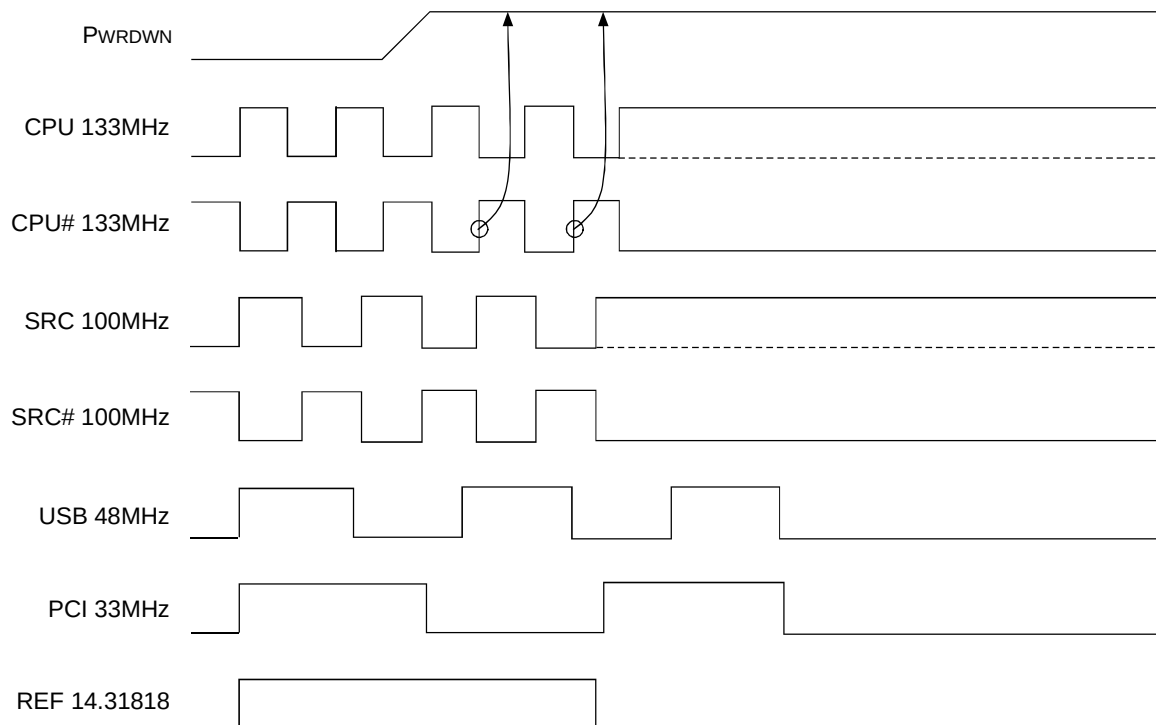


## PD, POWER DOWN

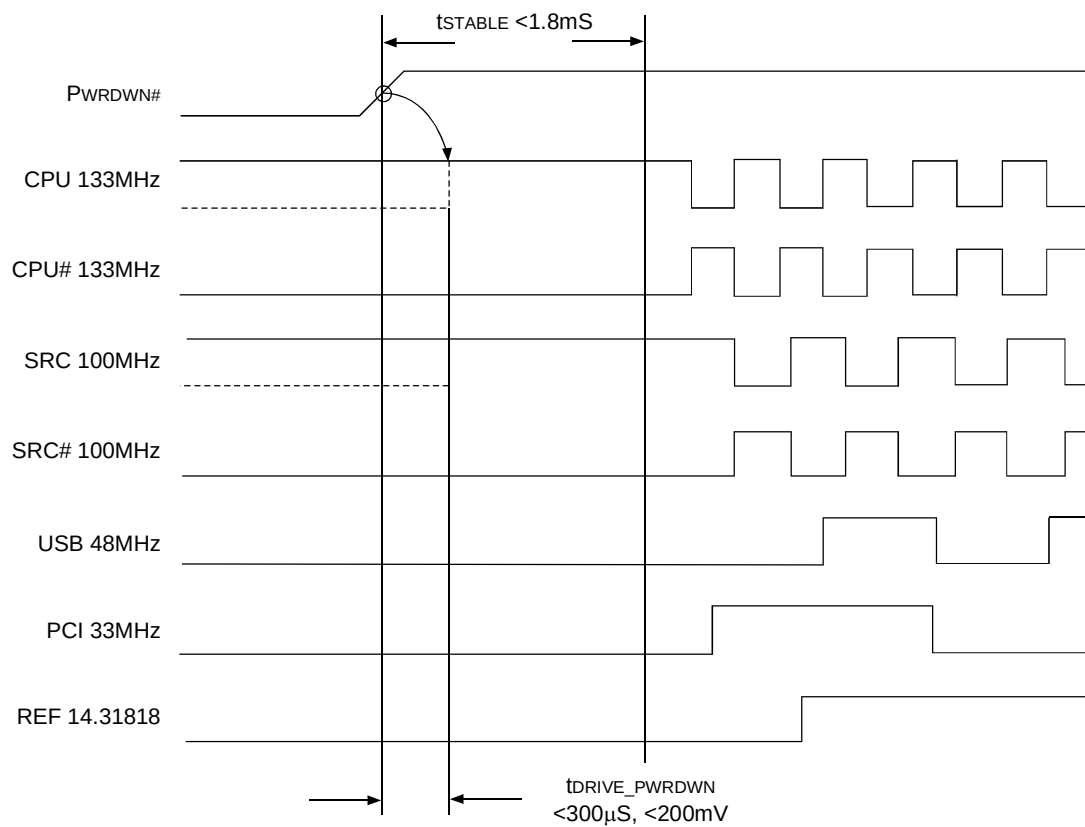
PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

| PWRDWN | CPU               | CPU#   | SRC               | SRC#   | PCIF/PCI | USB   | DOT96             | DOT96# | REF       |
|--------|-------------------|--------|-------------------|--------|----------|-------|-------------------|--------|-----------|
| 0      | Normal            | Normal | Normal            | Normal | 33MHz    | 48MHz | Normal            | Normal | 14.318MHz |
| 1      | IREF * 2 or float | Float  | IREF * 2 or float | Float  | Low      | Low   | IREF * 2 or float | Float  | Low       |

## PD ASSERTION



## PD DE-ASSERTION



## ORDERING INFORMATION

| IDTCV | XXX         | XX      | X         |  |                                                |
|-------|-------------|---------|-----------|--|------------------------------------------------|
|       | Device Type | Package | Grade     |  |                                                |
|       |             |         | Blank     |  | Commercial Temperature Range<br>(0°C to +70°C) |
|       |             |         | PV<br>PVG |  | Small Shrink Outline Package<br>SSOP - Green   |
|       |             |         | 115C      |  | Programmable FlexPC™ Clock for P4 Processor    |



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