QUICKSWITCH® PRODUCTS HIGH-SPEED CMOS BUS EXCHANGE SWITCH WITH ACTIVE TERMINATION (BUS HOLD)

IDTQS3L388

FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Active termination drives bus pins to rails when switches are off
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control pins
- Bus exchange allows nibble swap
- TTL-compatible input and output levels
- Bus-hold eliminates floating bus lines and reduces static power consumption
- Low-power version of QS3388
- Available in QSOP package

APPLICATIONS

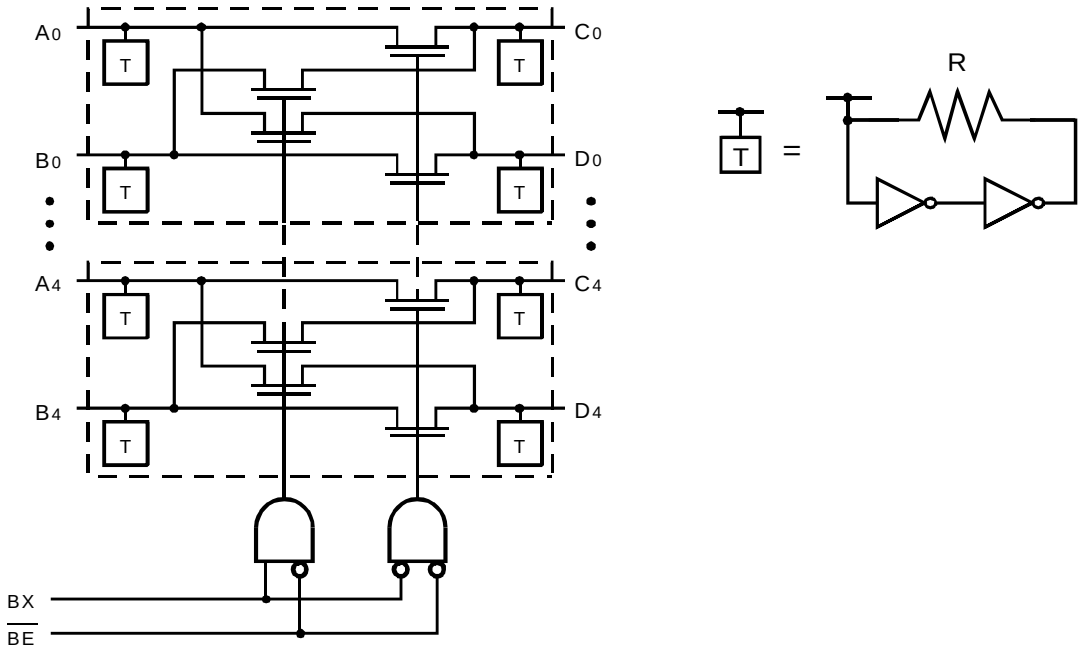
- Resource sharing
- Crossbar switching
- Last value latch (graphics and DSP)

DESCRIPTION:

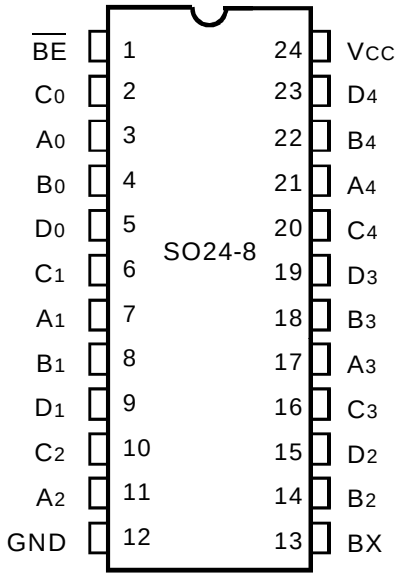
The QS3L388 is a low-power version of the QS3388. It provides ten high-speed CMOS TTL-compatible bus switches with active terminators on the bus switch I/O pins. The low ON resistance (5Ω) of the 3L388 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. When the switches are turned off, a low drive active terminator circuit drives the disconnected pins to Vcc or ground, away from the TTL threshold. This prevents undriven buses from floating. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a five-wide 2-to-1 multiplexer and to create low delay barrel shifters, etc.

The QS3L388 is characterized for operation at -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	– 0.5 to +7	V
V_{TERM}(3)	DC Switch Voltage V_S	– 0.5 to +7	V
V_{TERM}(3)	DC Input Voltage V_{IN}	– 0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation (T_A = 85°C)	.5	W
T_{STG}	Storage Temperature	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

CAPACITANCE (1)

(T_A = +25°C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins	Typ.	Max.	Unit
Control Inputs	3	5	pF
Quickswitch Channels (Switch OFF)	5	7	pF

NOTE:
1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
A_0 - A_4, B_0 - B_4	I/O	Buses A, B
C_0 - C_4, D_0 - D_4	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

FUNCTION TABLE (1)

$\overline{BE}$	BX	A_0 - A_4	B_0 - B_4	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C_0 - C_4	D_0 - D_4	Connect
L	H	D_0 - D_4	C_0 - C_4	Exchange

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't care
   Z = High-Impedence

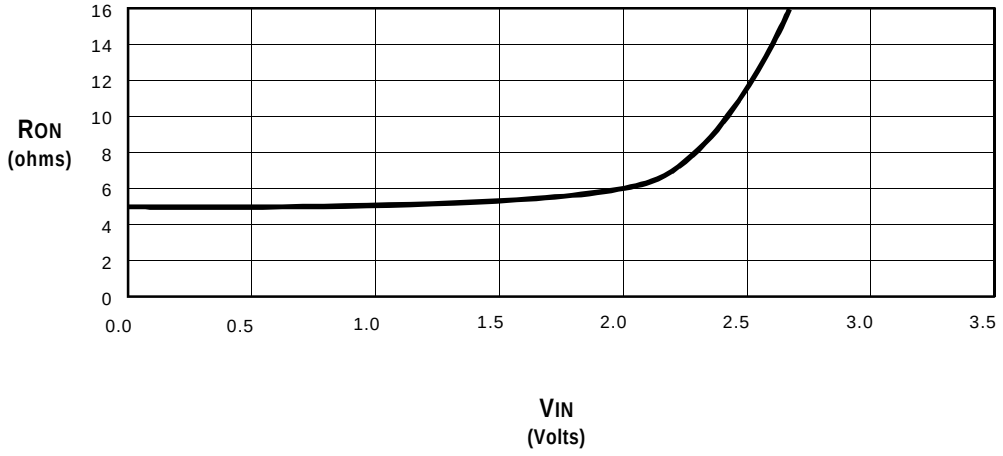
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IN}	Input Leakage Current (Control Inputs)	0V ≤ V_{IN} ≤ Vcc	—	.01	±1	µA
R_{ON}	Switch ON Resistance	Vcc = Min., V_{IN} = 0V, I_{ON} = 30mA	—	5	7	Ω
		Vcc = Min., V_{IN} = 2.4V, I_{ON} = 15mA	—	10	15	
I_{BH}	Input Current (2)	Vcc = Max., V_{IN} = 0V or Vcc	—	—	±20	µA
	Switch Pins	Vcc = Max., 0.8V < V_{IN} < 2V	—	—	±500	
I_{BHH}	Bus Hold Sustaining Source Current - HIGH(3)	Vcc = Min., V_{IN} = 2V	– 60	—	—	µA
I_{BHL}	Bus Hold Sustaining Sink Current - LOW(4)	Vcc = Min., V_{IN} = 0.8V	+ 60	—	—	

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Input current specified under two conditions:
   a) Input voltage at GND or Vcc. This indicates the input current under steady-state condition.
   b) Input voltage between 0.8V and 2V (TTL input threshold range). This indicates the maximum input current during transient condition. The driver connected to the input must overcome this current requirement in order to switch the logic state of the bus-hold circuit.
3. I_{BHH} represents the latching capability of the bus-hold circuit in logic HIGH state.
4. I_{BHL} represents the latching capability of the bus-hold circuit in logic LOW state.

TYPICAL ON RESISTANCE vs V_{IN} AT Vcc = 5.0V



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions [1]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc, f = 0	3	µA
ΔI_{CC}	Power Supply Current per Control Input HIGH [2]	V_{CC} = Max., V_{IN} = 3.4V, f = 0	2.5	mA
I_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A, B, C, D pins open Control Inputs Toggling at 50% Duty Cycle	0.25	mA/MHz

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven control input. (V_{IN} = 3.4V, Control Pins only.) A, B, C, D pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A, B, C, D inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 5%

C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

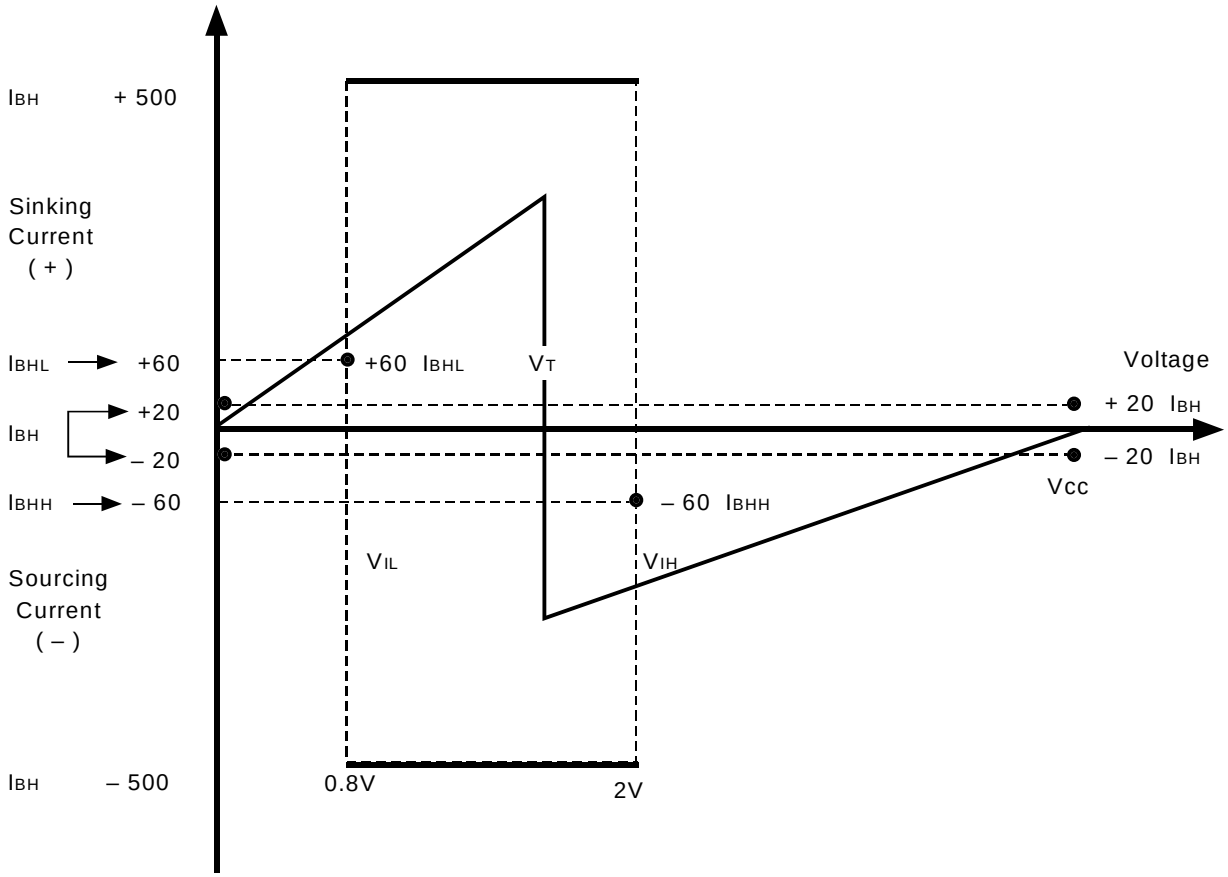
Symbol	Parameter	Min. [1]	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay [1,2] AxBx to CxDx, CxDx to AxBx	—	—	0.25	ns
t_{PZL} t_{PZH}	Switch Turn-On Delay $\overline{BE}$ to Ax, Bx, Cx, Dx	1.5	—	6.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-Off Delay [1] $\overline{BE}$ to Ax, Bx, Cx, Dx	1.5	—	5.5	ns
t_{BX}	Switch Multiplex Delay BX to Ax, Bx, Cx, Dx	1.5	—	6.5	ns

NOTES:
1. This parameter is guaranteed but not production tested.
2. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

ACTIVE TERMINATOR OR 'BUS-HOLD' CIRCUIT

The Active Terminator circuit, also known as the Bus-hold circuit, is configured as a "weak latch" with positive feedback. When connected to a TTL or CMOS input port, the Bus-hold circuit holds the last logic state at the input when the input is "disconnected" from the driver. When the output of a device connected to such an input attempts a logic level transition, it will over-drive the Bus-hold circuit. The primary benefit of this circuit is that it prevents CMOS inputs from floating, a situation which should be avoided to prevent spurious switching of inputs and unnecessary power dissipation. Bus-hold is a better solution than the traditional approach of using resistive termination to V_{CC} or GND to prevent bus floating, because the Bus-hold circuit does not consume any static power.

V-I CHARACTERISTICS OF BUS-HOLD CIRCUIT

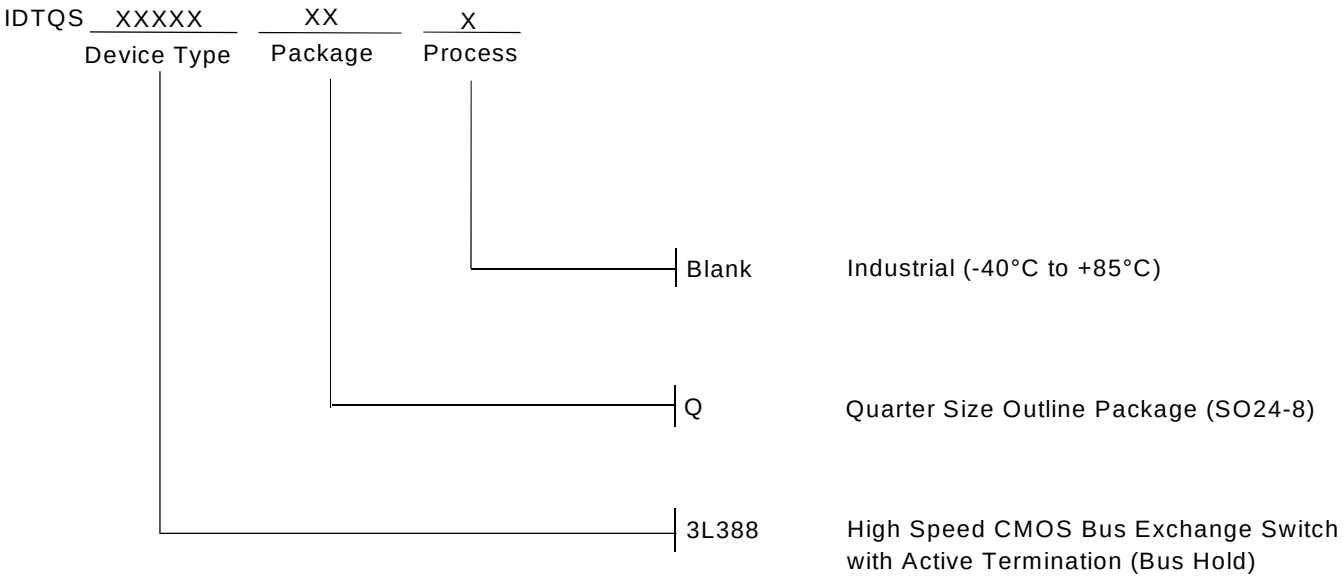


$V_T \equiv$ Threshold Voltage $\approx 1.5V$

$V_{IL} \approx .8$ $V_{IH} \approx 2V$

The figure above shows the input V-I characteristics of a Bus-hold implementation. The input characteristics resemble a resistor. As the input voltage is increased from 0 volts, the 'sink' current increases linearly. When the TTL threshold of the circuit is reached (typically 1 .5 volts), the latch changes the logic state due to positive feedback and the direction of current is reversed. As the voltage is further increased towards V_{CC}, the input 'source' current begins to decrease, reaching the lowest level at $V_{IN} = V_{CC}$.

ORDERING INFORMATION



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