Preliminary data

SPU01N60S5
SPD01N60S5

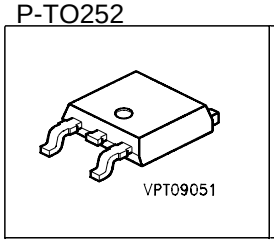
Cool MOS™ Power Transistor

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme d*v*/d*t* rated
- Optimized capacitances
- Improved noise immunity
- Former development designation:
  SPUx7N60S5/SPDx7N60S5

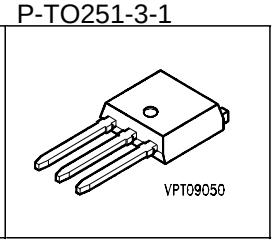
Product Summary

V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	6	Ω
I_D	0.8	A

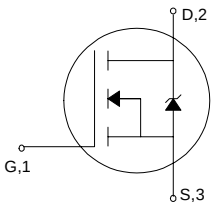
P-TO252



P-TO251-3-1



Type	Package	Ordering Code	Marking
SPU01N60S5	P-TO251-3-1	Q67040-S4193	01N60S5
SPD01N60S5	P-TO252	Q67040-S4188	01N60S5



Maximum Ratings,at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_C=25°C T_C=100°C	I_D	 0.8 0.5	A
Pulsed drain current [1] T_C=25°C	$I_{D\ puls}$	1.6	
Avalanche energy, single pulse I_D = 0.64 A, V_{DD} = 50 V	E_{AS}	20	mJ
Avalanche energy (repetitive, limited by T_{jmax}) I_D = 0.8 A , V_{DD} = 50 V	E_{AR}	0.01	
Avalanche current (repetitive, limited by T_{jmax})	I_{AR}	0.8	A
Reverse diode d*v*/d*t* I_S=0.8A, V_{DS}<V_{DSS}, d*i*/d*t*=100A/µs, T_{jmax}=150°C	d*v*/d*t*	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C=25°C	P_{tot}	11	W
Operating and storage temperature	T_j , T_{stg}	-55... +150	°C

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	11	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	R_{thJA}	-	-	75	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	75	
@ 6 cm^2 cooling area [2)]		-	-	50	

Static Characteristics, at T_j = 25 °C, unless otherwise specified

Drain-source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	-	-	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 250 µA, T_j = 25 °C	$V_{GS(th)}$	2.3	3	3.7	
Zero gate voltage drain current, V_{DS}=V_{DSS}	I_{DSS}				µA
V_{GS} = 0 V, T_j = 25 °C		-	0.5	1	
V_{GS} = 0 V, T_j = 150 °C		-	-	50	
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	-	-	100	nA
Drain-source on-state resistance V_{GS} = 10 V, I_D = 0.5 A	$R_{DS(on)}$	-	5.6	6	Ω

[1] current limited by T_{jmax}

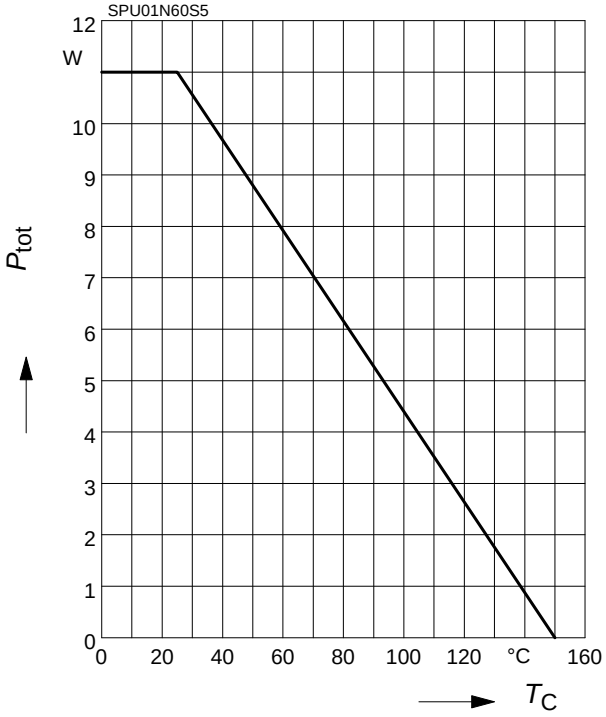
[2] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6 cm^2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics						
Transconductance	g_{fs}	$V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D=0.5A	-	0.75	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	100	-	pF
Output capacitance	C_{oss}		-	40	-	
Reverse transfer capacitance	C_{rss}		-	2.5	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=350V, V_{GS}=10V, I_D=0.8A, R_G=100Ω	-	30	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	55	82	
Fall time	t_f		-	30	45	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=350V, I_D=0.8A	-	0.9	-	nC
Gate to drain charge	Q_{gd}		-	2.2	-	
Total gate charge	Q_g	V_{DD}=350V, I_D=0.8A, V_{GS}=0 to 10V	-	3.9	5	
Reverse Diode						
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	0.8	A
Inverse diode direct current,pulsed	I_{SM}		-	-	1.6	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, I_F=0.8A	-	1	1.2	V
Reverse recovery time	t_{rr}	V_R=100V, I_F=I_S, di_F/dt=100A/µs	-	570	970	ns
Reverse recovery charge	Q_{rr}		-	0.75	-	µC

Power dissipation

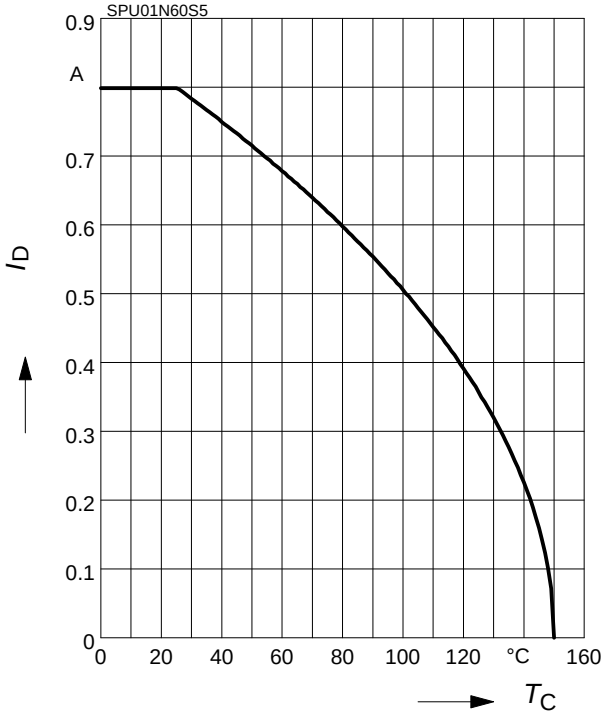
$P_{tot} = f(T_C)$



Drain current

$I_D = f(T_C)$

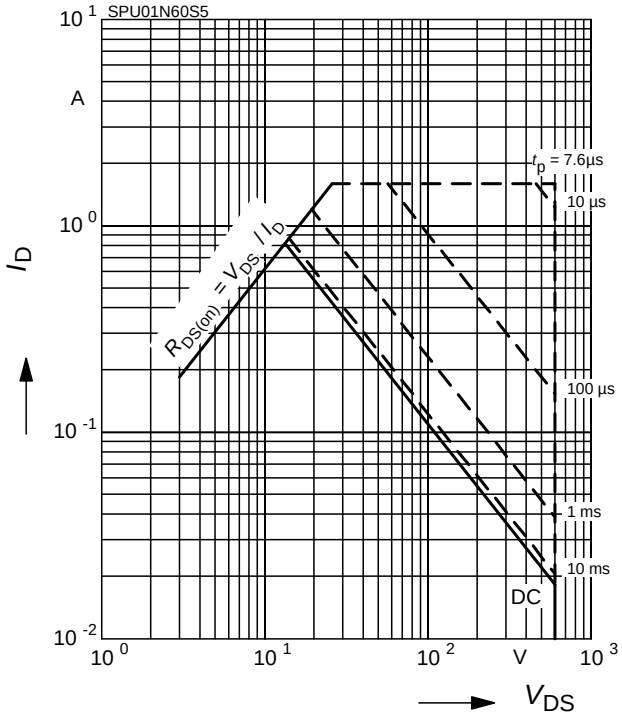
parameter: $V_{GS} \geq 10$ V



Safe operating area

$I_D = f(V_{DS})$

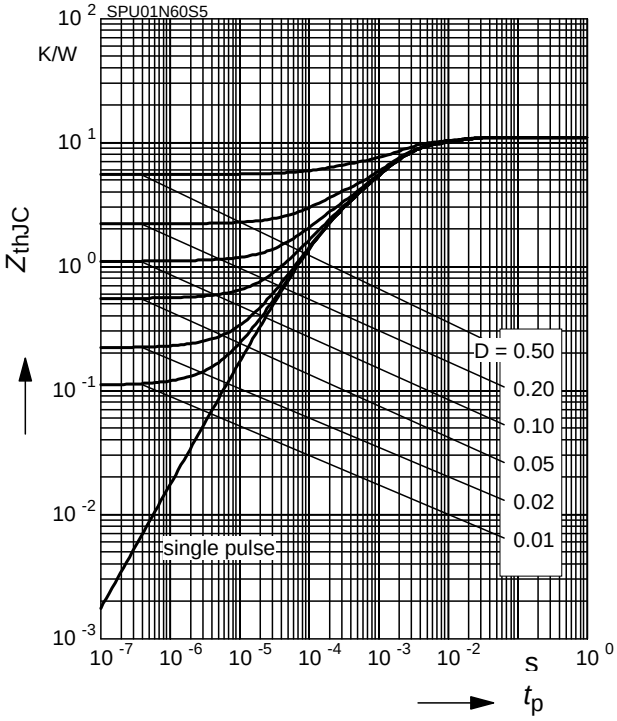
parameter: D=0.01, T_C=25°C



Transient thermal impedance

$Z_{thJC} = f(t_p)$

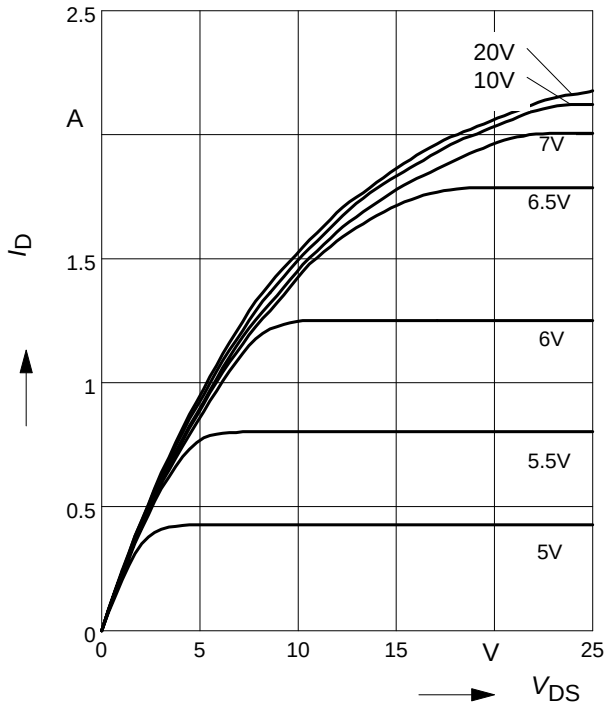
parameter : $D = t_p/T$



Typ. output characteristic

I_D = f (V_{DS})

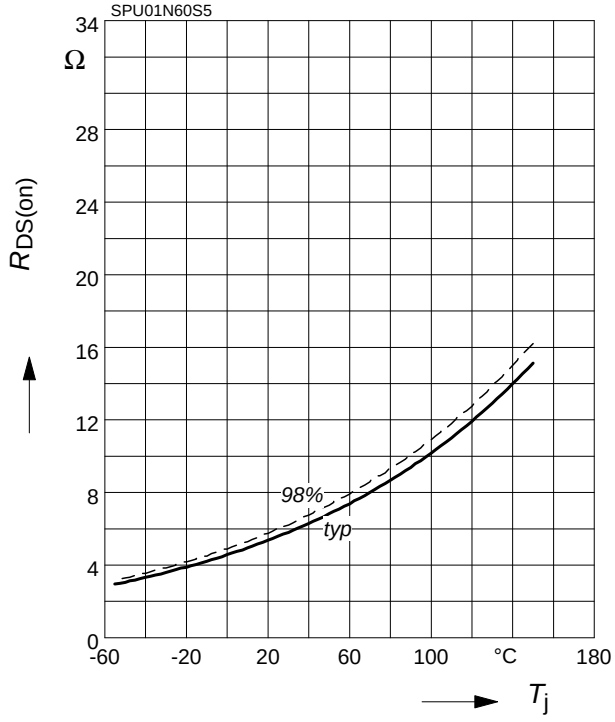
Parameter: V_{GS}, T_j = 25 °C



Drain-source on-resistance

$R_{DS(on)} = f(T_j)$

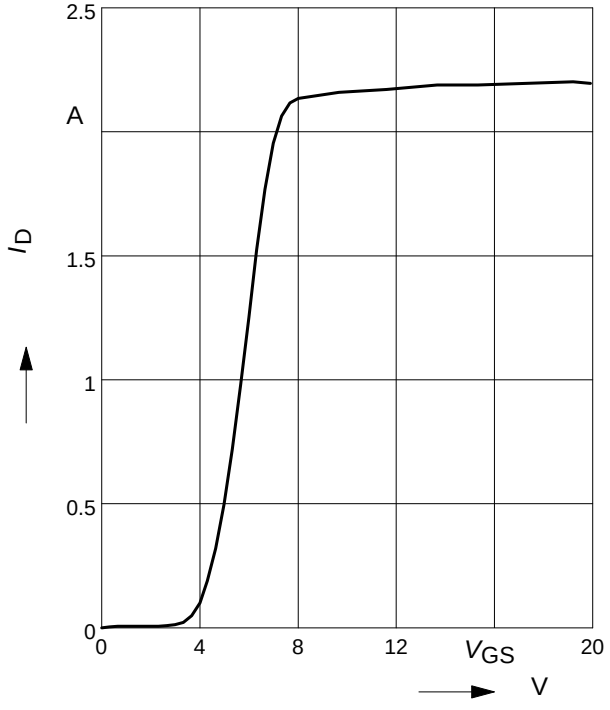
parameter : I_D = 0.5 A, V_{GS} = 10 V



Typ. transfer characteristics

$I_D = f(V_{GS})$

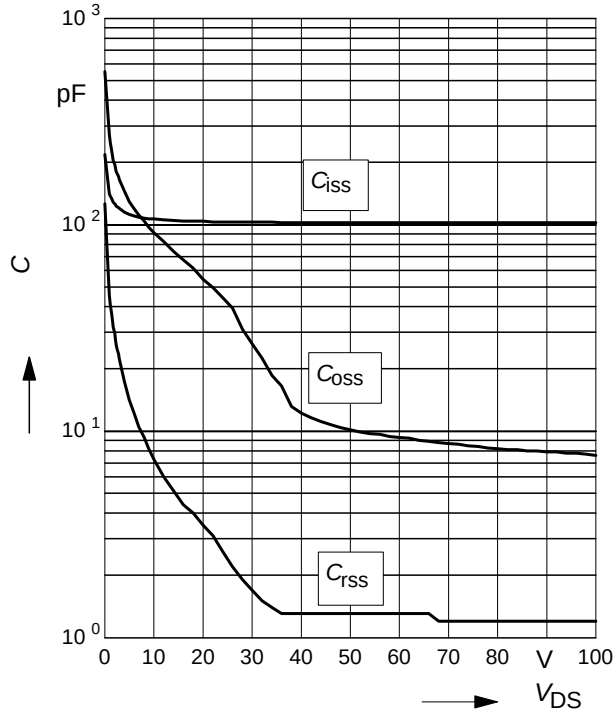
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



Typ. capacitances

$C = f(V_{DS})$

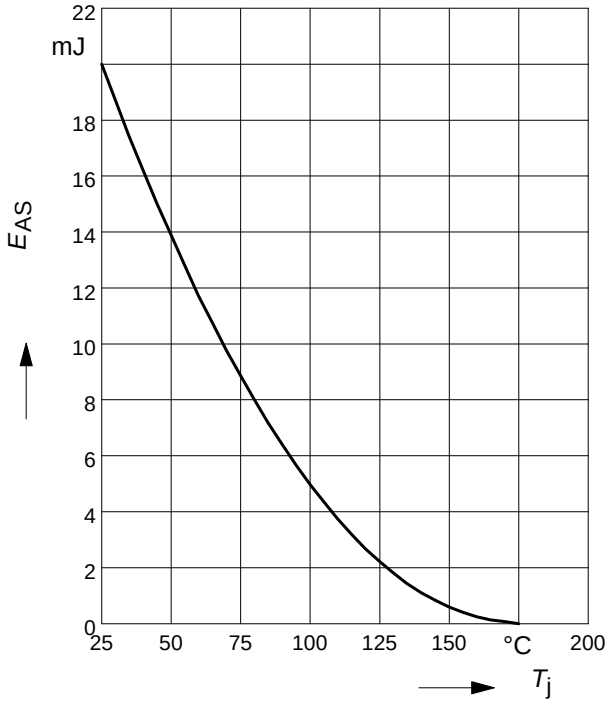
parameter: V_{GS}=0 V, f=1 MHz



Avalanche energy

$E_{AS} = f(T_j)$

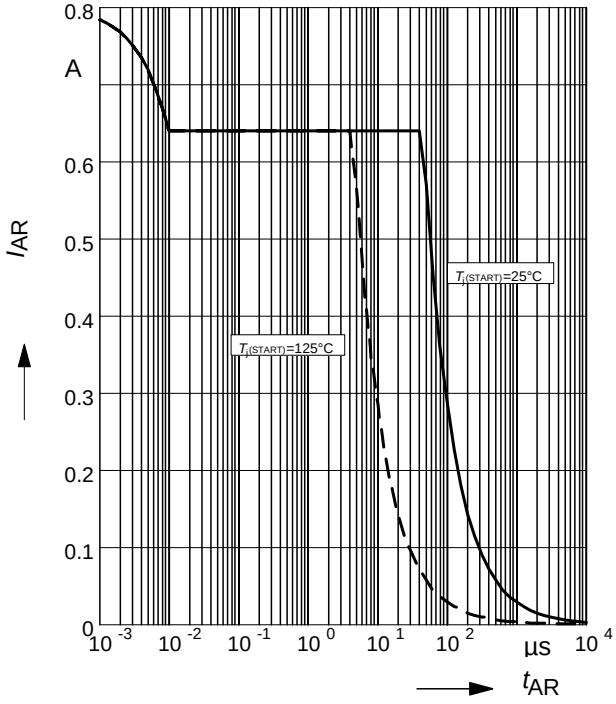
par.: I_D=0.64A, V_{DD}=50V



Avalanche SOA

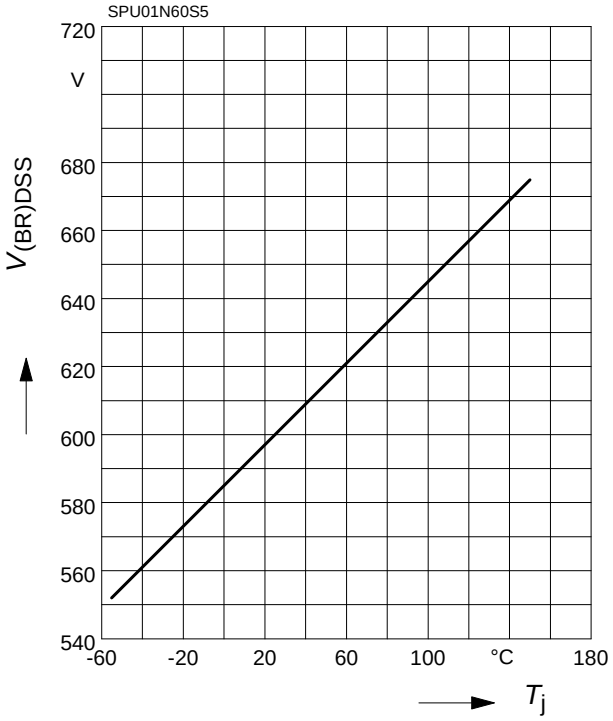
$I_{AR} = f(t_{AR})$

par.: $T_j \leq 150$ °C



Drain-source breakdown voltage

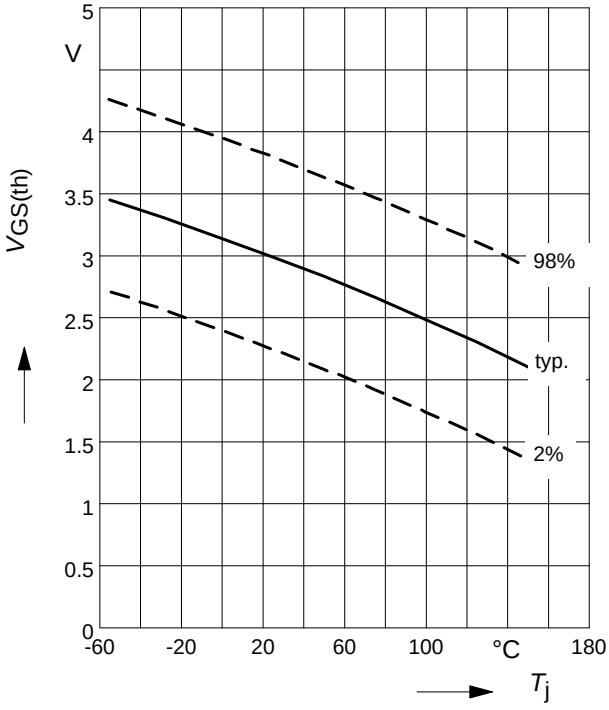
$V_{(BR)DSS} = f(T_j)$



Gate threshold voltage

$V_{GS(th)} = f(T_j)$

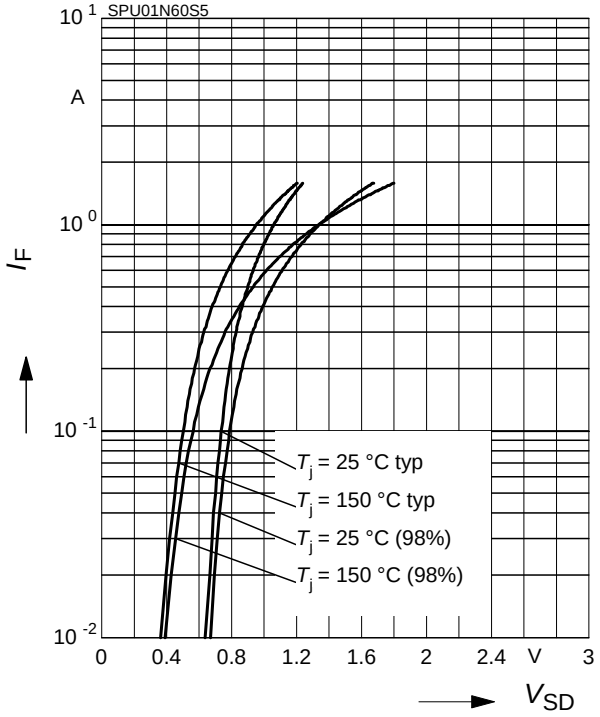
parameter: $V_{GS} = V_{DS}$, I_D = 250 µA



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

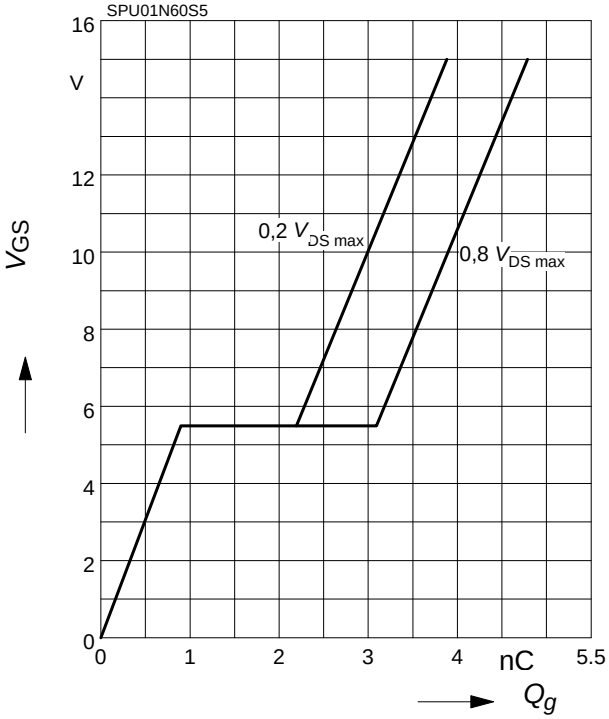
parameter: T_j , tp = 10 µs



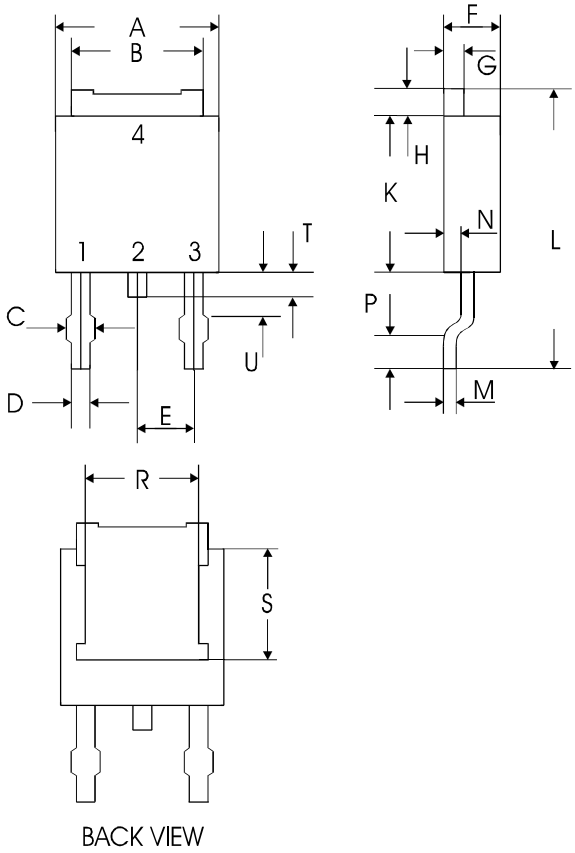
Typ. gate charge

$V_{GS} = f\ (Q_{Gate})$

parameter: I_D = 0.8 A pulsed

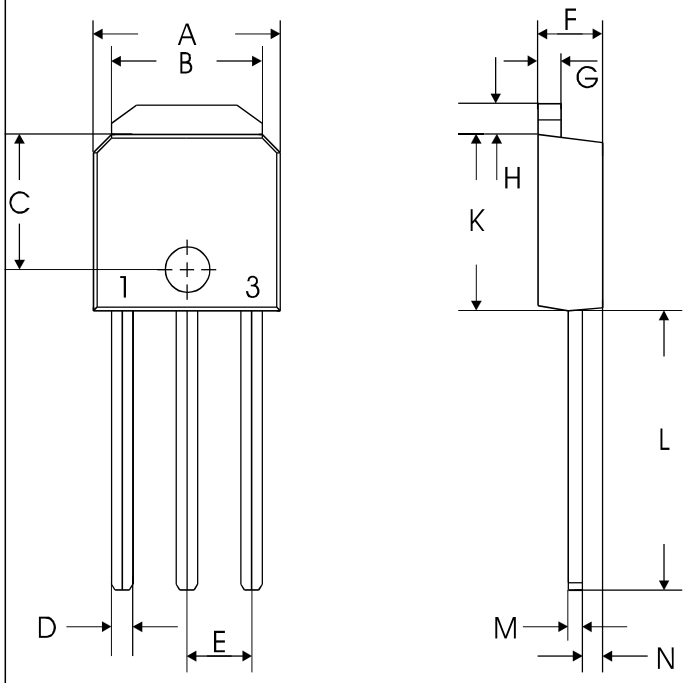


P-TO252 (D-Pak)



symbol	dimensions [mm]		dimensions [inch]	
	min	max	min	max
A	6.40	6.73	0.2520	0.2650
B	5.25	5.50	0.2067	0.2165
C	(0.65)	(1.15)	(0.0256)	(0.0453)
D	0.63	0.89	0.0248	0.0350
E	2.28		0.2520	
F	2.19	2.39	0.0862	0.0941
G	0.76	0.98	0.0299	0.0386
H	0.90	1.21	0.0354	0.0476
K	5.97	6.23	0.2350	0.2453
L	9.40	10.40	0.3701	0.4094
M	0.46	0.58	0.0181	0.0228
N	0.87	1.15	0.0343	0.0453
P	0.51	-	0.0201	-
R	5.00	-	0.1969	-
S	4.17	-	0.1642	-
T	0.26	1.02	0.0102	0.0402
U	-	-	-	-

P-TO251 (I-Pak)



symbol	dimensions [mm]		dimensions [inch]	
	min	max	min	max
A	6.47	6.73	0.2547	0.2650
B	5.25	5.41	0.2067	0.2130
C	4.19	4.43	0.1650	0.1744
D	0.63	0.89	0.0248	0.0350
E	2.29 typ.		0.0902 typ.	
F	2.18	2.39	0.0858	0.0941
G	0.76	0.86	0.0299	0.0339
H	1.01	1.11	0.0398	0.0437
K	5.97	6.23	0.2350	0.2453
L	9.14	9.65	0.3598	0.3799
M	0.46	0.56	0.0181	0.0220
N	0.98	1.15	0.0386	0.0453

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