LXT3008

T1/E1/J1 N+1 Protection Interface Unit

Preliminary Datasheet

The Intel® Protection Interface Unit (Intel® PIU), LXT3008, is a multiplexing element to be used in lieu of relays for more reliable and faster switching in a protection environment. It incorporates eight receivers and eight drivers in a single 160 ball PBGA package. The PIU is used in an N+1 redundancy scheme for Short Haul (SH) applications. It is used in conjunction with the Intel® LXT38x family of Line Interface Units (LIUs).

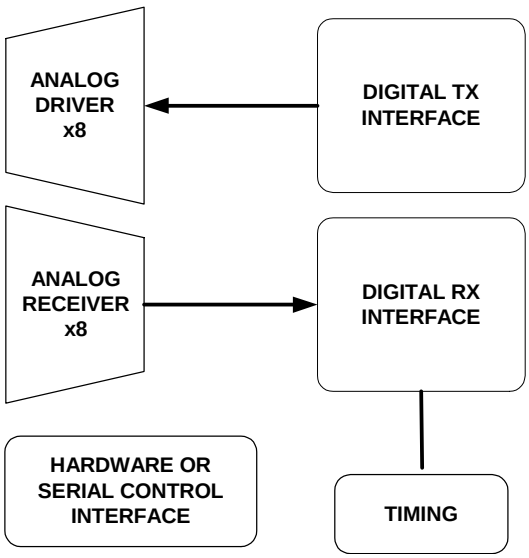
Each PIU contains eight three-state drivers and high impedance receivers. On the analog side, these devices interface to the primary T1/E1 bus and can either drive it or stay in a non-intrusive, high impedance state. On the digital side, the PIU provides recovered clock and data and also accepts transmit input clock and data. The receive output clock and data signals can be tri-stated. Therefore, multiple PIU elements can be connected in parallel.

Intel PIUs are controlled by hardware and therefore require no dedicated microprocessor. A 1x reference clock (1.544 MHz for T1 and 2.048 MHz for E1) is required for clock recovery. A single reference clock can feed all the PIUs in a protection matrix. Both the output analog drivers and the receive clock and data digital buffers can be tri-stated. PIUs also include three line build-out inputs (LEN0-2) for T1 DSX applications.

For further information on N+1 Protection, please see Application Note: N+1 Protection Without Relays Using Intel® Protection Interface Units (Intel® PIUs) - Intel® LXT3008 for T1/E1/J1 (Order Number 249532).

- LOS per ITU G.775, ETS 300 233 and T1.231
- 4 wire serial control interface
- Hardware or serial host control mode
- JTAG Boundary Scan test port per IEEE 1149.1
- 160 ball PBGA package
- Tri-stateable analog and digital short haul interface

LXT3008 Block Diagram



Order Number: 249531-003
June 2001

Preliminary Datasheet

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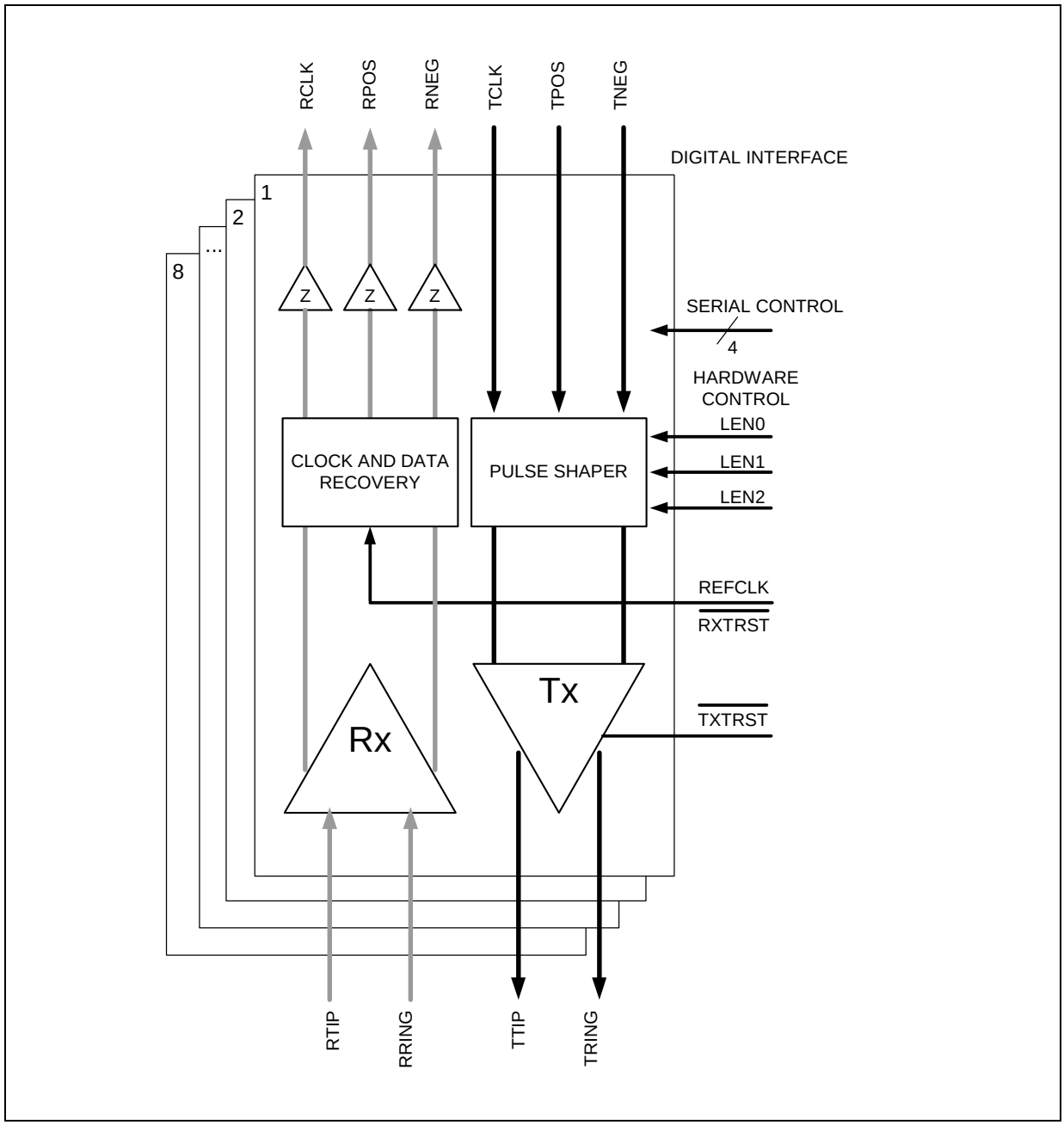
Revision History

Revision	Date	Description
-002	4/5/2001	Graphics improvements, timing diagram improvements, specification corrections.
-003	5/7/2001	Removed erroneous information. Re-arranged pin description table. Added sections on power requirements and architecture; added TBD characteristics.

Applications

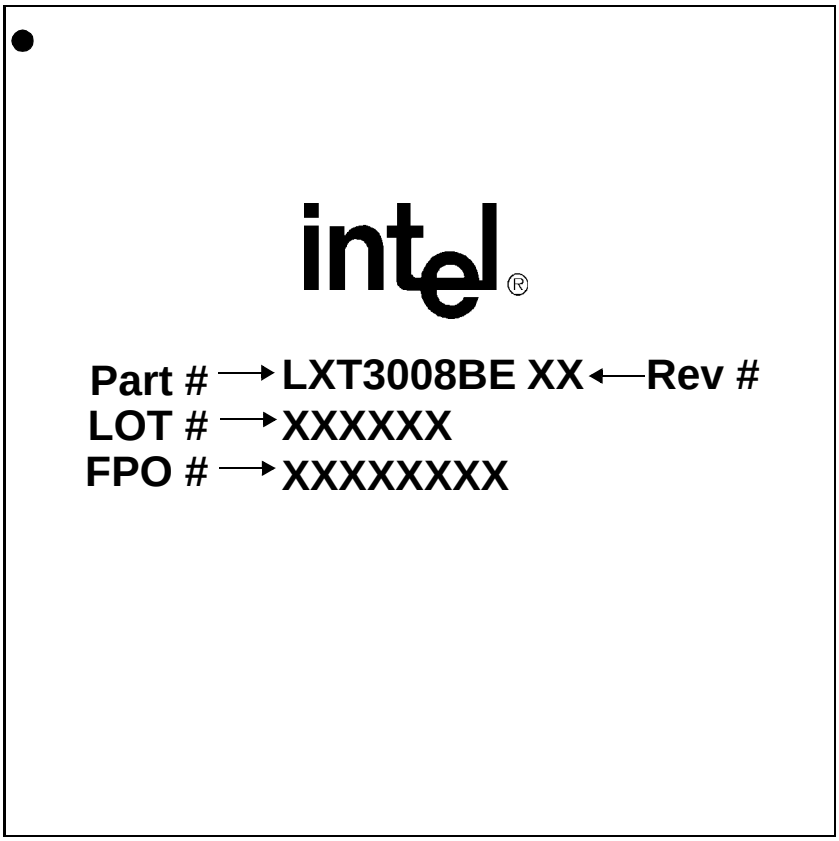
- SONET/SDH tributary interfaces
- Digital cross connects
- Public/private switching trunk line interfaces
- Microwave transmission systems
- M13, E1-E3 MUX

Figure 1. LXT3008 Detailed Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT3008 Plastic Ball Grid array (PBGA) Package Markings



Package Topside Markings	
Marking	**Definition**
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Figure 3. LXT3008 Plastic Ball Grid Array (PBGA) Package Pin Assignments

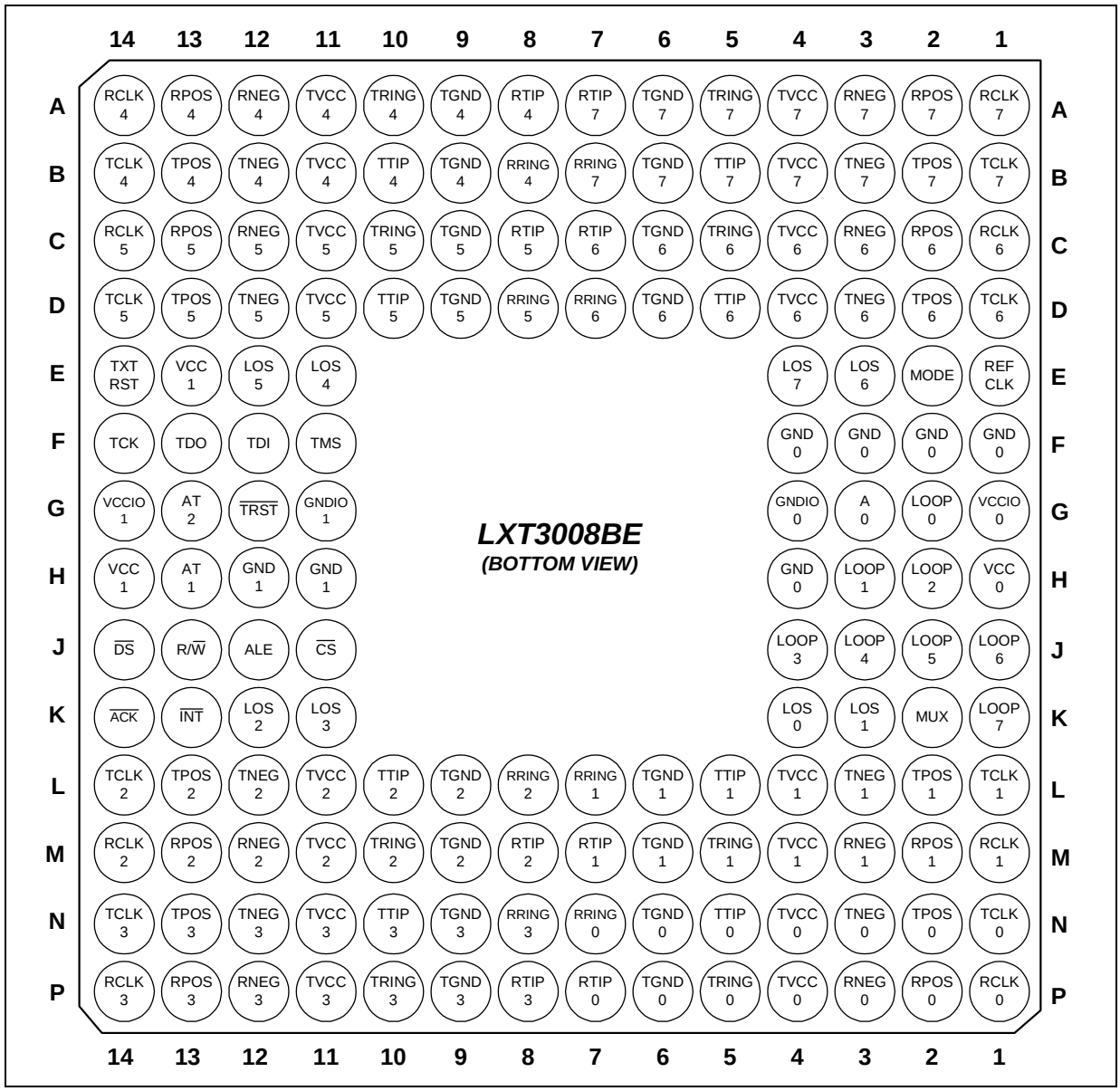


Table 1. LXT3008 Pin Description (Sheet 1 of 7)

Ball # PBGA	Symbol	I/O[1]	Description
			POWER Connections
H1	VCC0	S	**Power (Core).**
E13	VCC0	S	**Power (Core).**
F4	GND0	S	**Ground (Core).**
F3	GND0	S	**Ground (Core).**
F2	GND0	S	**Ground (Core).**
F1	GND0	S	**Ground (Core).**
G3	GND0	S	**Ground (Core).**
H4	GND0	S	**Ground (Core).**
H12	GND0	S	**Ground (Core).**
H14	VCC1	S	**Power (Core).**
H11	GND1	S	**Ground (Core).**
G1	VCCIO0	S	**Power (I/O).**
G4	GNDIO0	S	**Ground (I/O).**
G14	VCCIO1	S	**Power (I/O).**
G11	GNDIO1	S	**Ground (I/O).**
N4, P4	TVCC0	S	**Transmit Driver Power Supply.** Power supply pin for the output driver. TVCC pins can be connected to either a 3.3V or 5V power supply. Please refer to the Transmitter description.
N6, P6	TGND0	S	**Transmit Driver Ground.** Ground pin for the output driver.
L4, M4	TVCC1	S	**Transmit Driver Power Supply.**
L6, M6	TGND1	S	**Transmit Driver Ground.**
L11, M11	TVCC2	S	**Transmit Driver Power Supply.**
L9, M9	TGND2	S	**Transmit Driver Ground.**
N11, P11	TVCC3	S	**Transmit Driver Power Supply.**
N9, P9	TGND3	S	**Transmit Driver Ground.**
A11, B11	TVCC4	S	**Transmit Driver Power Supply.**
A9, B9	TGND4	S	**Transmit Driver Ground.**
C11, D11	TVCC5	S	**Transmit Driver Power Supply.**
C9, D9	TGND5	S	**Transmit Driver Ground.**
C4, D4	TVCC6	S	**Transmit Driver Power Supply.**
C6, D6	TGND6	S	**Transmit Driver Ground.**
A4, B4	TVCC7	S	**Transmit Driver Power Supply.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT3008 Pin Description (Sheet 2 of 7)

<table>
<tr><th>Ball # PBGA</th><th>Symbol</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>A6, B6</td><td>TGND7</td><td>S</td><td>Transmit Driver Ground.</td></tr>
<tr><td></td><td></td><td></td><td>Digital Interface Connections.</td></tr>
<tr><td>P1</td><td>RCLK0</td><td>DO</td><td>Receive Clock Output.
This pin provides the recovered clock from the signal received at RTIP and RRING. Under LOS conditions there is a transition from RCLK signal (derived from the recovered data) to MCLK signal at the RCLK output.</td></tr>
<tr><td>P2
P3</td><td>RPOS0
RNEG0</td><td>DO
DO</td><td>Receive Positive Data.
Receive Negative Data.
Bipolar Mode:
These pins act as active High bipolar Non Return to Zero (NRZ) receive signal outputs. A High signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A High signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. These signals are valid on the falling or rising edges of RCLK depending on the CLKE input.
Hardware Mode:
During a LOS condition, RPOS and RNEG will remain active.
Serial Host Mode:
RPOS and RNEG will either remain active or insert AIS into the receive path. Selection is determined by the RAISEN bit in the GCR register.</td></tr>
<tr><td>N1</td><td>TCLK0</td><td>DI</td><td>Transmit Clock Input. During normal operation TCLK is active, and TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is Low, the output drivers enter a low power high-Z mode. If TCLK is High for more than 16 clock cycles, the pulse shaping circuit is disabled and the transmit output pulse widths are determined by the TPOS and TNEG duty cycles.
<table>
<tr><th>TCLK</th><th>Operating Mode</th></tr>
<tr><td>Clocked</td><td>Normal operation</td></tr>
<tr><td>L</td><td>Driver outputs enter tri-state</td></tr>
</table>
When pulse shaping is disabled, it is possible to overheat and damage the LXT3008 device by leaving transmit inputs high continuously. For example, a programmable ASIC might leave all outputs high until it is programmed. To prevent this, clock one of these signals: TPOS, TNEG, TCLK or MCLK. Another solution is to set one of these signals low: TPOS, TNEG, TCLK, or OE.</td></tr>
<tr><td>N2
N3</td><td>TPOS0
TNEG0</td><td>DI
DI</td><td>Transmit Positive Data Input.
Transmit Negative Data Input.
Bipolar Mode:
TPOS/TNEG are active High NRZ inputs. TPOS indicates the transmission of a positive pulse, whereas TNEG indicates the transmission of a negative pulse.
<table>
<tr><th>TPOS</th><th>TNEG</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>1</td><td>0</td><td>Positive Mark</td></tr>
<tr><td>0</td><td>1</td><td>Negative Mark</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table></td></tr>
<tr><td colspan="4">1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output
S: Power Supply; N.C.: Not Connected.</td></tr>
</table>

Table 1. LXT3008 Pin Description (Sheet 3 of 7)

Ball # PBGA	Symbol	I/O[1]	Description
M1	RCLK1	DO	**Receive Clock Output.**
M2	RPOS1	DO	**Receive Positive Data Output.**
M3	RNEG1	DO	**Receive Negative Data Output.**
L1	TCLK1	DI	**Transmit Clock Input.**
L2	TPOS1	DI	**Transmit Positive Data Input.**
L3	TNEG1	DI	**Transmit Negative Data Input.**
M14	RCLK2	DO	**Receive Clock Output.**
M13	RPOS2	DO	**Receive Positive Data Output.**
M12	RNEG2	DO	**Receive Negative Data Output.**
L14	TCLK2	DI	**Transmit Clock Input.**
L13	TPOS2	DI	**Transmit Positive Data Input.**
L12	TNEG2	DI	**Transmit Negative Data Input.**
P14	RCLK3	DO	**Receive Clock Output.**
P13	RPOS3	DO	**Receive Positive Data Output.**
P12	RNEG3	DO	**Receive Negative Data Output.**
N14	TCLK3	DI	**Transmit Clock Input.**
N13	TPOS3	DI	**Transmit Positive Data Input.**
N12	TNEG3	DI	**Transmit Negative Data Input.**
A14	RCLK4	DO	**Receive Clock Output.**
A13	RPOS4	DO	**Receive Positive Data Output.**
A12	RNEG4	DO	**Receive Negative Data Output.**
B14	TCLK4	DI	**Transmit Clock Input.**
B13	TPOS4	DI	**Transmit Positive Data Input.**
B12	TNEG4	DI	**Transmit Negative Data Input.**
C14	RCLK5	DO	**Receive Clock Output.**
C13	RPOS5	DO	**Receive Positive Data Output.**
C12	RNEG5	DO	**Receive Negative Data Output.**
D14	TCLK5	DI	**Transmit Clock Input.**
D13	TPOS5	DI	**Transmit Positive Data Input.**
D12	TNEG5	DI	**Transmit Negative Data Input.**
C1	RCLK6	DO	**Receive Clock Output.**
C2	RPOS6	DO	**Receive Positive Data Output.**
C3	RNEG6	DO	**Receive Negative Data Output.**
D1	TCLK6	DI	**Transmit Clock Input.**
D2	TPOS6	DI	**Transmit Positive Data Input.**
D3	TNEG6	DI	**Transmit Negative Data Input.**
A1	RCLK7	DO	**Receive Clock Output.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT3008 Pin Description (Sheet 4 of 7)

Ball # PBGA	Symbol	I/O[1]	Description
A2 A3	RPOS7 RNEG7	DO DO	**Receive Positive Data Output.** **Receive Negative Data Output.**
B1	TCLK7	DI	**Transmit Clock Input.**
B2 B2	TPOS7 TDATA7	DI DI	**Transmit Positive Data Input.** **Transmit Data Input.**
B3	TNEG7	DI	**Transmit Negative Data Input.**
			Analog Interface Connections
P7 N7	RTIP0 RRING0	AI AI	**Receive TIP Input.** **Receive Ring Input.** These pins are the inputs to the differential line receiver. Data and clock are recovered and output on the RPOS/RNEG and RCLK pins.
N5 P5	TTIP0 TRING0	AO AO	**Transmit Tip Output.** **Transmit Ring Output.** These pins are differential line driver outputs. TTIP and TRING will be in high impedance state if the TCLK pin is Low or the OE pin is Low. In serial host mode, TTIP and TRING can be three-stated on a port-by-port basis by writing a ‘1’ to the OEx bit in the Output Enable Register (OER).
M7 L7	RTIP1 RRING1	AI AI	**Receive Tip Input.** **Receive Ring Input.**
L5 M5	TTIP1 TRING1	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
M8 L8	RTIP2 RRING2	AI AI	**Receive Tip Input.** **Receive Ring Input.**
L10 M10	TTIP2 TRING2	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
P8 N8	RTIP3 RRING3	AI AI	**Receive Tip Input.** **Receive Ring Input.**
N10 P10	TTIP3 TRING3	AO AO	**Transmit Tip.** **Transmit Ring Output.**
A8 B8	RTIP4 RRING4	AI AI	**Receive Tip Input.** **Receive Ring Input.**
B10 A10	TTIP4 TRING4	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
C8 D8	RTIP5 RRING5	AI AI	**Receive Tip Input.** **Receive Ring Input.**
D10 C10	TTIP5 TRING5	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
C7 D7	RTIP6 RRING6	AI AI	**Receive Tip Input.** **Receive Ring Input.**
D5 C5	TTIP6 TRING6	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT3008 Pin Description (Sheet 5 of 7)

Ball # PBGA	Symbol	I/O[1]	Description
A7 B7	RTIP7 RRING7	AI AI	**Receive Tip Input.** **Receive Ring Input.**
B5 A5	TTIP7 TRING7	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
			Control and Status Connections
E1	$\overline{\text{REFCLK}}$/ RXTRST	DI	**Master Clock Input.** $\overline{\text{REFCLK}}$/RXTRST is an independent, free-running reference clock. It's frequency should be 1.544 MHz for T1 operation and 2.048 MHz for E1 operation. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit • Generation of RCLK signal during a loss of signal condition If $\overline{\text{REFCLK}}$/RXTRST is High, the PLL clock recovery circuit is disabled. In this mode, the LXT3008 operates as a simple data receiver. If $\overline{\text{REFCLK}}$/RXTRST is Low, the complete receive path is powered down and the output pins RCLK, RPOS and RNEG are switched to tri-state mode.
E2	MODE	DI	**Mode Select Input.** This pin is used to select the operating mode of the LXT3008. In Hardware Mode, the parallel processor interface is disabled and hardwired pins are used to control configuration and report status. In Serial Host mode, the serial interface pins: SDI, SDO, SCLK and $\overline{\text{CS}}$ are used. **MODE** / **Operating Mode** Low / Hardware Mode High / NOT USED Vcc/2 / Serial Host Mode For Serial Host Mode, the pin should connected to a resistive divider consisting of two 10 kΩ resistors across Vcc and Ground.
G2 H3 H2 J4 J3 J2 J1 K1	LOOP0 LOOP LOOP2 LOOP3 LOOP4 LOOP5 LOOP6 LOOP7	DI DI DI DI DI DI DI DI	**Loopback Mode Select/Parallel Data bus Input &Output.** Serial Host Mode In serial host mode, D0-7 should be grounded. Hardware Mode In hardware mode, the LXT3008 works in normal operation if these pins are left open (unconnected). The LXT3008 enters remote loopback mode when each pin for each designated channel is Low. In this mode, data on TPOS and TNEG is ignored and data received on RTIP and RRING is looped around and retransmitted on TTIP and TRING. The LXT3008 enters analog local loopback mode, if these pins are High. In this mode, data received on RTIP and RRING is ignored and data transmitted on TTIP and TRING is internally looped around and routed back to the receive inputs. ***Note:*** When these inputs are left open, they stay in a high impedance state. Therefore, the layout design should not route signals with fast transitions near the LOOP pins. This practice will minimize capacitive coupling.
K2	UNUSED	DI	**Unused Input.Tie this unused input low.**

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Table 1. LXT3008 Pin Description (Sheet 6 of 7)

Ball # PBGA	Symbol	I/O[1]	Description
K13	$\overline{\text{INT}}$	DO	**Interrupt.** This active Low, maskable, open drain output requires an external 10k pull up resistor. If the corresponding interrupt enable bit is enabled, $\overline{\text{INT}}$ goes Low to flag the host when the LXT3008 changes state (see details in the interrupt handling section). The microprocessor INT input should be set to level triggering.
K14	SDO	DO	**Serial Data Output (Serial Host Mode).** Serial Mode If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes into High Z state during a serial port write access. Hardware Mode Do not connect in hardware mode.
J14 J14	SDI LEN0	DI DI	**Serial Data Input (Serial Mode).** **Line Length Equalizer Input (Hardware Mode).** Serial Host Mode In serial host mode, this pin is used as Serial Data Input. Hardware Mode This pin determines the shape and amplitude of the transmit pulse. Please refer to Table 2.
J13	LEN1	DI	**Line Length Equalizer Input (Hardware Mode).** Serial Host Mode Connect to ground. Hardware Mode This pin determines the shape and amplitude of the transmit pulse. Please refer to Table 2.
J12 J12	SCLK LEN2	DI DI	**Shift Clock Input (Serial Host Mode).** **Line Length Equalizer Input (Hardware Mode).** Serial Host Mode In serial Host mode, this pin acts as serial shift clock. Hardware Mode This pin determines the shape and amplitude of the transmit pulse. Please refer to Table 2.
J11	$\overline{\text{CS}}$	DI	**Chip Select/Jitter Attenuator Select Input**. Serial Host Mode This active Low input is used to access the serial interface. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low. Hardware Mode Reserved.
G13	AT2	AO	**JTAG Analog Output Test Port 2.**
H13	AT1	AI	**JTAG Analog Input Test Port 1.**
G12	$\overline{\text{TRST}}$		**JTAG Controller Reset Input.** Input is used to reset the JTAG controller. $\overline{\text{TRST}}$ is pulled up internally and may be left disconnected.
F11	TMS	DI	**JTAG Test Mode Select Input.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT3008 Pin Description (Sheet 7 of 7)

Ball # PBGA	Symbol	I/O[1]	Description
F14	TCK	DI	**JTAG Clock Input.** Clock input for JTAG. Connect to GND when not used.
F13	TDO	DO	**JTAG Data Output.** Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. Updated on falling edge of TCK.
F12	TDI	DI	**JTAG Data Input.** Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.
E14	$\overline{\text{TXTRST}}$	DI	**Output Driver Enable Input.** If this pin is asserted Low all analog driver outputs immediately enter a high impedance mode to support redundancy applications without external mechanical relays. All other internal circuitry stays active. In serial host mode, TTIP and TRING can be tristated on a port-by-port basis by writing a '1' to the $\overline{\text{TXTRST}}$x bit in the Output Enable Register (OER).
K4	LOS0	DO	**Loss of Signal Output.** LOS output is High, indicating a loss of signal, when the incoming signal has no transitions for a specified time interval. The LOS condition is cleared and the output pin returns to Low when the incoming signal has sufficient number of transitions in a specified time interval (details in LOS functional description).
K3	LOS1	DO	**Loss of Signal Output.**
K12	LOS2	DO	**Loss of Signal Output.**
K11	LOS3	DO	**Loss of Signal Output.**
E11	LOS4	DO	**Loss of Signal Output.**
E12	LOS5	DO	**Loss of Signal Output.**
E3	LOS6	DO	**Loss of Signal Output.**
E4	LOS7	DO	**Loss of Signal Output.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

2.0 Functional Description

Figure 1 is a block diagram of the LXT3008. The LXT3008 is a fully integrated octal Protection Interface Unit (PIU) designed for T1 1.544 Mbps and E1 2.048 Mbps short-haul applications.

The transmitter timing reference is TCLKx, and the receiver reference clock is $\overline{\text{REFCLK}}$/RXTRST. The $\overline{\text{REFCLK}}$/RXTRST signal enables the output from the receiver signal. The $\overline{\text{TXTRST}}$ signal enables the transmitter outputs.

2.1 Introduction

2.1.1 N+1 and 1+1 redundancy

In a 1+1 redundancy scheme, there is **one** primary card **plus one** backup card for each desired redundancy in a design. In an N+1 scheme, there are **N** primary cards or elements **plus one** backup card or element (to backup the N number of cards or elements) in the design. The LXT384 allows 1+1 implementation without relays. The LXT3008 can be used in conjunction with the LXT384 to

implement a protection matrix in an N+1 redundancy application.The PIU converts clock and data signals to/from the multiplexed bus from/to analog interface signals, and is capable of driving twisted pair or coaxial lines. These PIUs operate only in T1, E1, or J1 mode and at short haul distances (up to 655 feet). An architectural example of N+1 redundancy, using the Intel PIUs, is shown in Figure 4.

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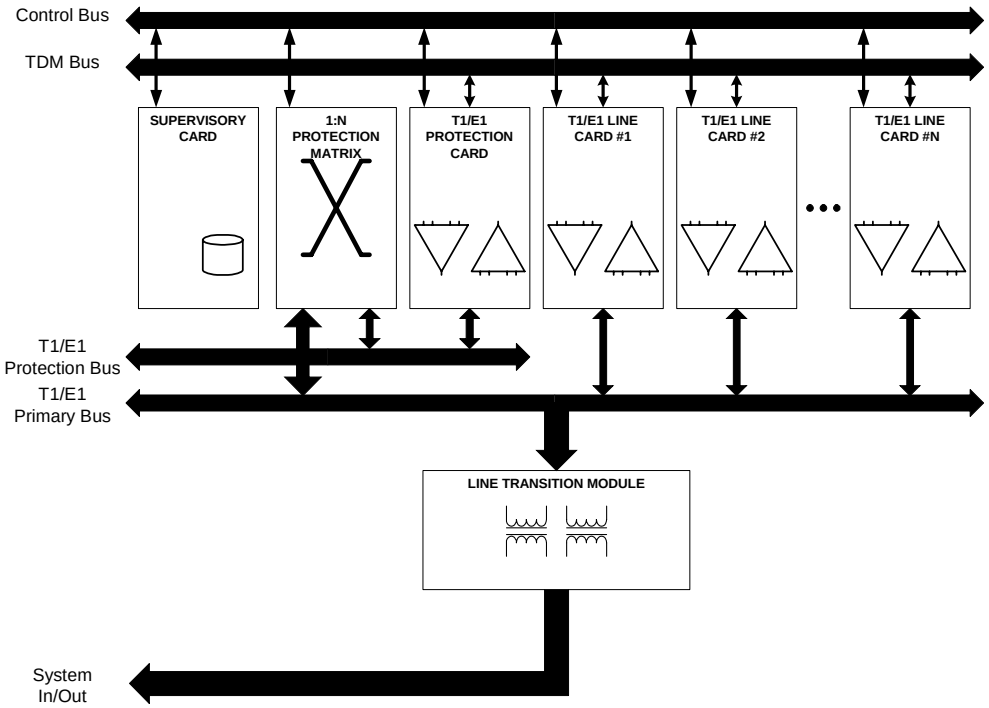
Figure 4. N+1 System Architecture



With this architecture, there is a primary T1/E1/J1 bus running across the backplane. The primary bus carries all the analog TIP/RING signals from each of the N line cards. The protection matrix connects to all these signals and is normally set to a high impedance, non-intrusive state. There is a bus connecting the protection switching matrix to the protection board. Whenever one of the line cards is deemed to be faulty by the supervisory card, its output drivers are switched to a high impedance state. At this point, the protection matrix replaces the missing signal in the primary T1/E1/J1 bus with the signal from the protection card. A common line transition module contains all the isolation transformers, line side protection and receive side termination. See application note “N+1 Protection Without Relays” for more detailed information.

Figure 5, “Line Card to Protection Matrix Interface, Receive Direction” on page 18, Figure 6, “Line card to Protection Matrix Interface, Transmit Direction” on page 19, and Figure 7, “Low Power Interface To The Protection Card” on page 20, are examples of Protection Interface Matrix implementations.

Figure 5. Line Card to Protection Matrix Interface, Receive Direction

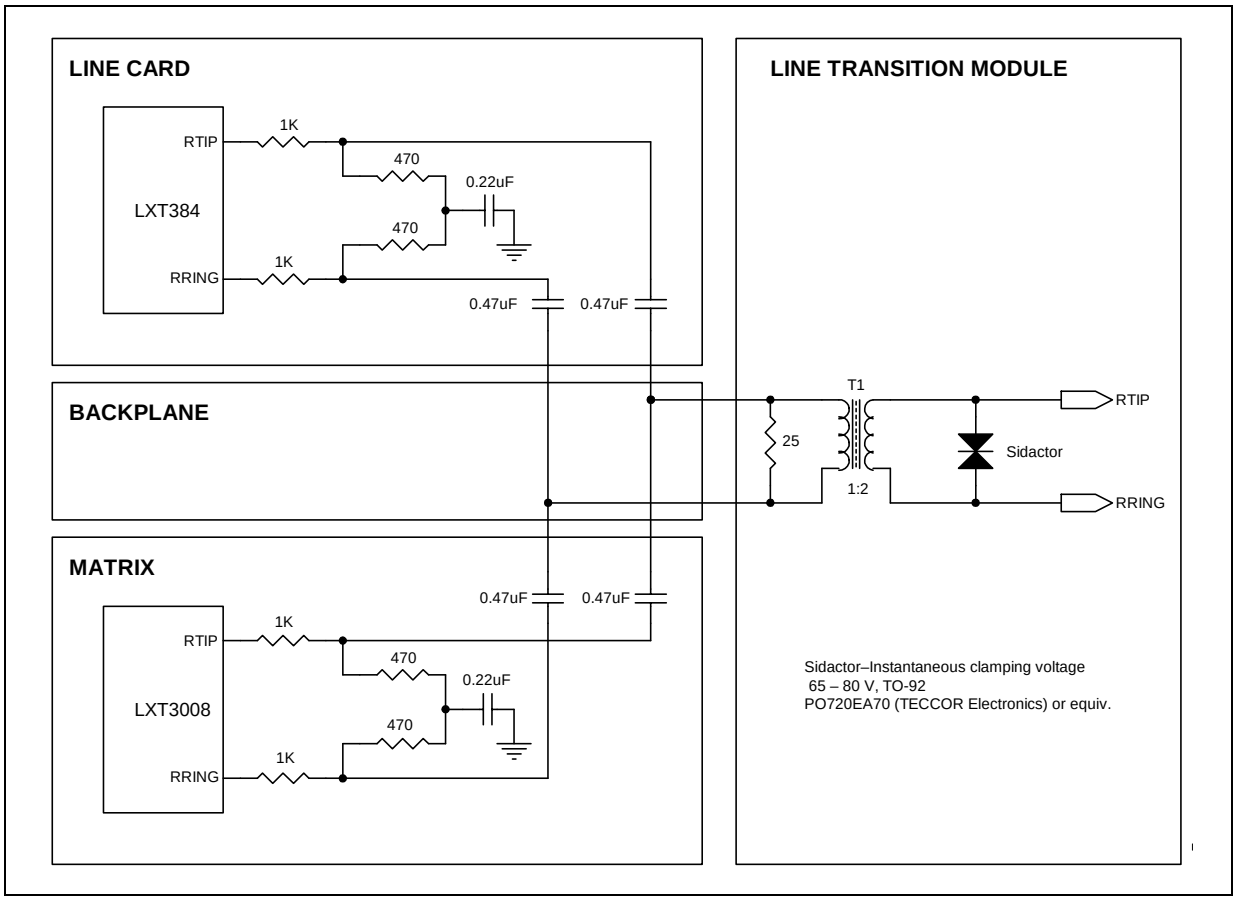


Figure 6. Line card to Protection Matrix Interface, Transmit Direction

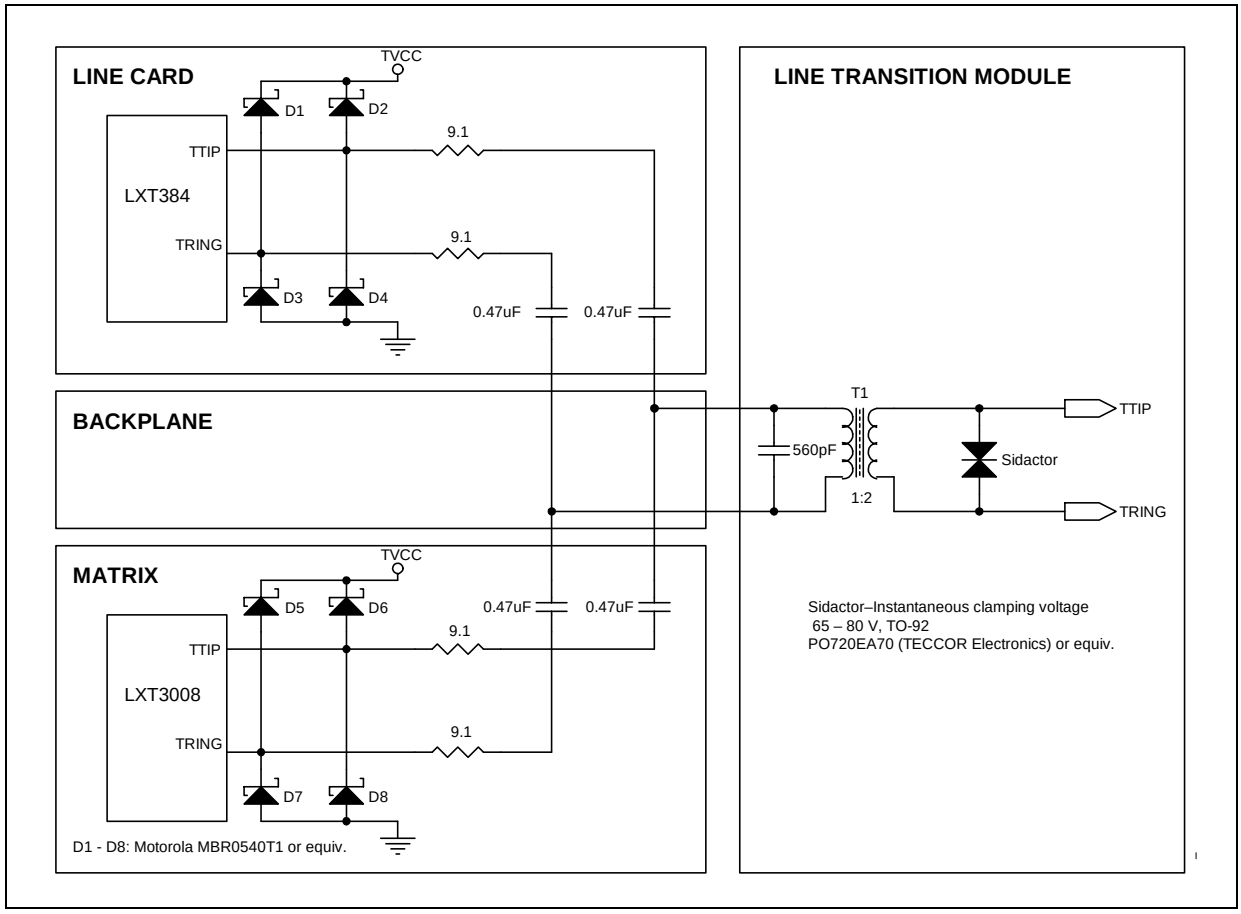
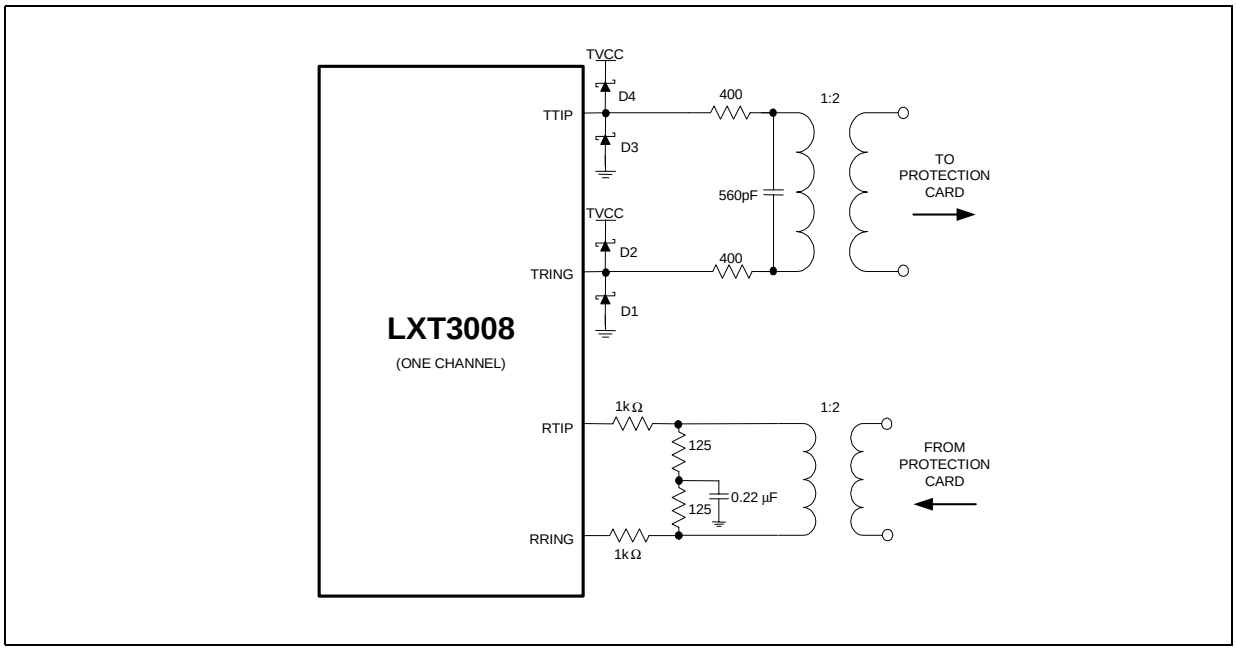


Figure 7. Low Power Interface To The Protection Card



2.2 Initialization

During power-up, the transceiver remains static until the power supply reaches approximately 60% of VCC. During power-up, an internal reset sets all registers to their default values and resets the status and state machines for the LOS.

2.2.1 Reset Operation

Writing to the RESet register (RES) initiates a 1 microsecond reset cycle. This operation sets all LXT3008 registers to their default values.

2.3 Receiver

The eight receivers in the LXT3008 are identical. The following paragraphs describe the operation of one.

The twisted-pair input is received via a 1:2 step down transformer. Positive pulses are received at RTIP, negative pulses at RRING. Recovered data is output at RPOS and RNEG in the bipolar mode and at RDATA in the unipolar mode. The recovered clock is output at RCLK. RPOS/RNEG validation relative to RCLK is pin selectable (CLKE).

The receive signal is processed through the peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN2-0 from 011 to 111) the threshold is set to 70% (typical) of

the peak value. This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LEN2-0 = 000), the threshold is 50% (typical).

After processing through the data slicers, the received signal goes to the data and timing recovery section. The data and timing recovery circuits provide an input jitter tolerance better than required by Pub 62411 and ITU G.823.

2.3.1 Loss of Signal Detector

The loss of signal detector in the LXT3008 uses a dedicated analog and digital loss of signal detection circuit. It is independent of its internal data slicer comparators and complies to the latest ITU G.775 and ANSI T1.231 recommendations. Under serial control, the detector can be configured to comply to the ETSI ETS 300 233 specification (LACS Register). In hardware mode, the LXT3008 supports LOS per G.775 for E1 and ANSI T1.231 for T1 operation.

When the LOS condition is cleared, the LOS flag is reset and another transition replaces $\overline{\text{REFCLK}}$/RXTRST with the recovered clock at RCLK. RPOS/RNEG will reflect the data content at the receiver input during the entire LOS detection period for that channel.

2.3.1.1 E1 Mode

In G.775 mode, a loss of signal is detected if the signal is below 200 mV typ. for 32 consecutive pulse intervals. When the received signal reaches 12.5% ones density (4 marks in a sliding 32-bit period) with no more than 15 consecutive zeros and the signal level exceeds 250 mV typ., the LOS flag is reset and another transition replaces $\overline{\text{REFCLK}}$/RXTRST with the recovered clock at RCLK.

In ETSI 300 233 mode, a loss of signal is detected if the signal is below 200 mV for 2048 consecutive intervals (1 ms). The LOS condition is cleared and the output pin returns to Low when the incoming signal has transitions when the signal level is equal or greater than 250 mV for more than 32 consecutive pulse intervals.

2.3.1.2 T1 Mode

The T1.231 LOS detection criterion is employed. LOS is detected if the signal is below 200 mV for 175 contiguous pulse positions. The LOS condition is terminated upon detecting an average pulse density of 12.5% over a period of 175 contiguous pulse positions starting with the receipt of a pulse. The incoming signal is considered to have transitions when the signal level is equal or greater than 250 mV.

2.4 Driver

The eight drivers of the LXT3008 are identical. Transmit data is clocked serially into the device at TPOS/TNEG in the bipolar mode. The transmit clock (TCLK) supplies the input synchronization. The driver samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. Refer to the Test Specifications Section for $\overline{\text{REFCLK}}$/RXTRST and TCLK timing characteristics. If TCLK is not supplied, the driver remains powered down and the TTIP/TRING outputs are held in a High Z state. In addition, fast output tristatability is also available through the $\overline{\text{TXTRST}}$ pin (all ports) and/or the port's OEx bit in the Output Enable Register (OER).

2.4.1 Driver Pulse Shaping

The transmitted pulse shape is internally generated using a high speed D/A converter. Shaped pulses are further applied to the line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance regardless of whether it is driving marks, spaces or if it is in transition. This well controlled dynamic impedance provides excellent return loss when used with external precision resistors (± 1% accuracy) in series with the transformer.

2.4.1.1 Hardware Mode

In hardware mode, pins LEN0-2 determine the pulse shaping as described in Table 2. The LEN settings also determine whether the operating mode is T1 or E1.

Note: In hardware mode, all eight ports will share the same pulse shaping setting. Independent pulse shaping for each channel is available in host mode.

2.4.1.2 Serial Host Mode

In Serial Host Mode, the contents of the Pulse Shaping Data Register (PSDAT) determines the shape of pulse output at TTIP/TRING. Please refer to Table 22 and Table 23.

Table 2. Line Length Equalizer Inputs

LEN2	LEN1	LEN0	Line Length[1]	Cable Loss[2]	Operation Mode
0	1	1	0 - 133 ft. ABAM	0.6 dB	T1
1	0	0	133 - 266 ft. ABAM	1.2 dB	
1	0	1	266 - 399 ft. ABAM	1.8 dB	
1	1	0	399 - 533 ft. ABAM	2.4 dB	
1	1	1	533 - 655 ft. ABAM	3.0 dB	
0	0	0	E1 G.703, 75Ω coaxial cable and 120 Ω twisted pair cable.		E1

1. Line length from LXT3008 to DSX-1 cross-connect point. ABAM = 22AWG insulated twisted pair wire.
2. Maximum cable loss at 772 KHz.

2.4.1.3 Output Driver Power Supply

The output driver power supply (TVCC pins) can be either 3.3V (for E1) or 5V (for E1 or T1) nominal. When TVCC=5V, the LXT3008 drives E1 (75Ω/120Ω) and T1 100Ω lines through a 1:2 transformer and 11Ω/9.1Ω series resistors. The 9.1Ω series resistors may be used for both E1 and T1 twisted pair operation, which is slightly lower than the recommended value for E1 of 11Ω.

When TVCC=3.3V, the LXT3008 drives E1 (75Ω/120Ω) lines through a 1:2 transformer and 11Ω series resistor.

2.5 Line Protection

Figure 7 on page 20 shows recommended receive line interface circuitry. In the receive side, the 1K Ω series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (70K Ω typical), the resistors do not affect the receiver sensitivity. In the

transmit side, Figure 7 on page 20, the Schottky diodes D1-D4 and D5-D8 protect the output driver.While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

2.6 Loopbacks

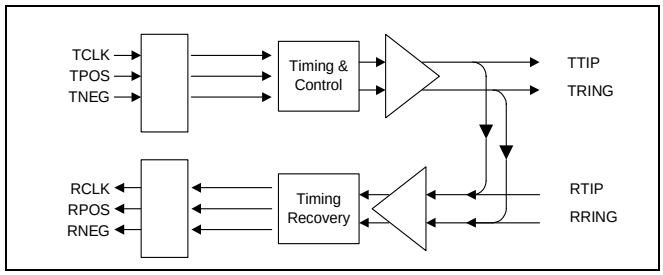
The LXT3008 offers three loopback modes for diagnostic purposes. In hardware mode, the loopback mode is selected with the LOOPn pins. In serial software mode, the ALOOP, DLOOP and RLOOP registers are employed.

2.6.1 Analog Loopback

When selected, the transmitter outputs (TTIP & TRING) are connected internally to the receiver inputs (RTIP & RRING) as shown in Figure 8. Data and clock are output at RCLK, RPOS & RNEG pins for the corresponding transceiver.

Note: Signals on the RTIP & RRING pins are ignored during analog loopback.

Figure 8. Analog Loopback

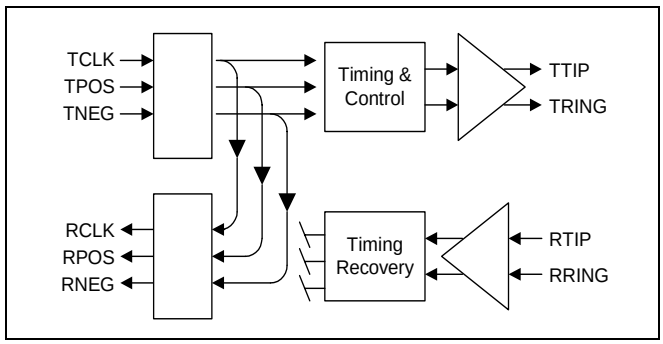


2.6.2 Digital Loopback

The digital loopback function is available in serial host mode only. When selected, the transmit clock and data inputs (TCLK, TPOS & TNEG) are looped back and output on the RCLK, RPOS & RNEG pins (see Figure 9). The data presented on TCLK, TPOS & TNEG is also output on the TTIP & TRING pins.

Note: Signals on the RTIP & RRING pins are ignored during digital loopback.

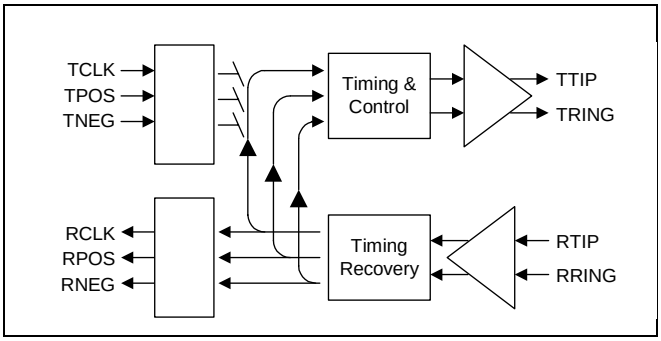
Figure 9. Digital Loopback



2.6.3 Remote Loopback

During remote loopback (see Figure 10), the RCLK, RPOS & RNEG outputs routed to the transmit circuits and output on the TTIP & TRING pins. Note: input signals on the TCLK, TPOS & TNEG pins are ignored during remote loopback.

Figure 10. Remote Loopback



2.7 Operation Mode Summary

Table 3 lists summarizes all the LXT3008 hardware settings and corresponding operating modes.

Table 3. Operation Mode Summary

$\overline{\text{REFCLK}}$/ RXTRST	TCLK	LOOP[1]	Receive Mode	Transmit Mode	Loopback
L	Clocked	Open	Power Down	Pulse Shaping ON	No Loopback
L	Clocked	L	Power Down	Pulse Shaping ON	No Remote Loopback
L	Clocked	H	Power Down	Pulse Shaping ON	No effect on op.
L	L	X	Power Down	Power down	No Loopback
1. Hardware mode only.					

2.8 Interrupt Handling

2.8.1 Interrupt Sources

An interrupt comes from a status change in the LOS (Loss of Signal) status register (04H). The LXT3008 analog/digital loss of signal processor continuously monitors the receiver signal and updates the specific LOS status bit to indicate presence or absence of a LOS condition.

2.8.2 Interrupt Enable

The LXT3008 provides a latched interrupt output ($\overline{\text{INT}}$). An interrupt occurs any time there is a transition on any enabled bit in the status register. Registers 06H and 07H are the LOS, and DFM interrupt enable registers (respectively). Writing a logic “1” into the mask register will enable the respective bit in the respective Interrupt status register to generate an interrupt. The power-on default value is all zeroes. The setting of the interrupt enable bit does not affect the operation of the status registers.

Registers 08H and 09H are the LOS and DFM (respectively) interrupt status registers. When there is a transition on any enabled bit in a status register, the associated bit of the interrupt status register is set and an interrupt is generated (if one is not already pending). When an interrupt occurs, the $\overline{INT}$ pin is asserted Low. The output stage of the $\overline{INT}$ pin consists only of a pull-down device; an external pull-up resistor of approximately 10K ohm is required to support wired-OR operation.

2.8.3 Interrupt Clear

When an interrupt occurs, the Interrupt Service Routine (ISR) should read the *interrupt status registers* (08H and 09H) to identify the interrupt source. Reading the Interrupt Status register clears the "sticky" bit set by the interrupt. Automatically clearing the register prepares it for the next interrupt.

The ISR should then read the corresponding *status monitor register* to obtain the current status of the device.

Note: There are two status monitor registers: the LOS (04H) and the DFM (05H). Reading either status monitors register will clear its corresponding interrupts on the rising edge of the read or data strobe. When all pending interrupts are cleared, the $\overline{INT}$ pin goes High.

2.9 Power requirements

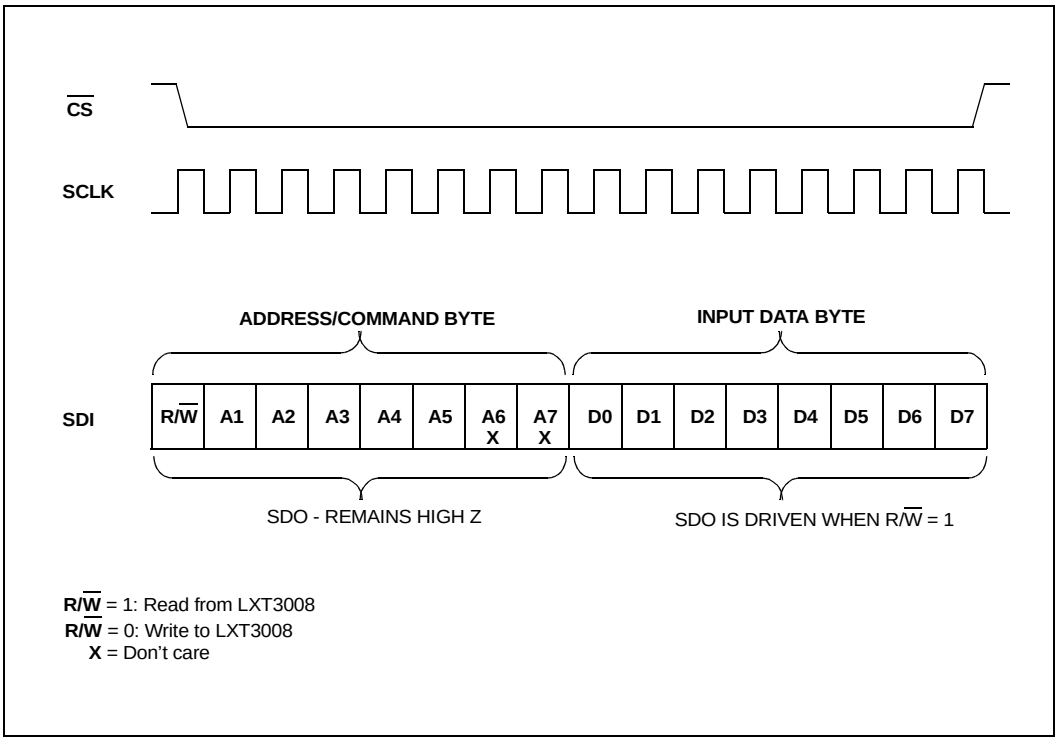
Refer to Table 33 on page 40 for the following. PIUs do not drive the line unless in backup mode. The PIU only requires the digital supply voltage for the standby mode. When the PIU is in the backup mode, it uses the same amount of power as the primary transmitters were utilizing, i.e. transferring the power utilization from the primary LIU to the backup PIU. Each PIU typically uses about 300 mW of digital power while in the standby mode (seeTable 33 on page 40).

In an N+1 configuration, there is a corresponding PIU for every LIU. In addition, there is a backup LIU (on a backup line card, for instance) and a backup PIU to the backup LIU. Neither of these are active until the system goes to the backup mode, but remain in the standby mode. In addition to the power required for the corresponding PIUs (for each of the primary LIUs), digital power for the backup LIU/PIU pair is required. When the system goes into the backup mode, the additional transmitter power for the backup LIU/PIU pair will also be added to the total power requirement.

2.10 Serial Host Mode

The LXT3008 operates in Serial Host Mode when the MODE pin is tied to VCCIO÷2. Figure 11 shows the SIO data structure. The registers are accessible through a 16 bit word: an 8 bit Command/Address byte (bits R/$\overline{W}$ and A1-A7) and a subsequent 8 bit data byte (bits D0-7). Bit R/$\overline{W}$ determines whether a read or a write operation occurs. Bits A5-0 in the Command/Address byte address specific registers (the address decoder ignores bits A7-6). The data byte depends on both the value of bit R/$\overline{W}$ and the address of the register as set in the Command/Address byte.

Figure 11. Serial Host Mode Timing



3.0 Register Descriptions

Table 4. Serial Port Register Addresses (Sheet 1 of 2)

Name	Symbol	Address Serial Port A7-A1	Mode
ID Register	ID	xx00000	R
Analog Loopback	ALOOP	xx00001	R/W
Remote Loopback	RLOOP	xx00010	R/W
Reserved	RSVD	xx00011	R/W
LOS Status Monitor	LOS	xx00100	R
Reserved	RSVD	xx00101	R
LOS Interrupt Enable	LIE	xx00110	R/W
Reserved	RSVD	xx00111	R/W
LOS Interrupt Status	LIS	xx01000	R
Reserved	RSVD	xx01001	R
Software Reset Register	RES	xx01010	R/W
Reserved	RSVD	xx01011	R/W

Table 4. Serial Port Register Addresses (Sheet 2 of 2)

Name	Symbol	Address Serial Port A7-A1	Mode
Digital Loopback	DL	xx01100	R/W
Reserved	RSVD	xx01101	R/W
Reserved	RSVD	xx01110	R/W
Global Control Register	GCR	xx01111	R/W
Pulse Shaping Indirect Address Register	PSIAD	xx10000	R/W
Pulse Shaping Data Register	PSDAT	xx10001	R/W
Output Enable Register	OER	xx10010	R/W
Reserved	RSVD	xx10011	R
Reserved	RSVD	xx10100	R/W
Reserved	RSVD	xx10101	R

Table 5. Register Bit Names (Sheet 1 of 2)

Register			Bit							
Name	Sym	RW	7	6	5	4	3	2	1	0
ID Register	ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Analog Loopback	ALOOP	R/W	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
Remote Loopback	RLOOP	R/W	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
LOS Status Monitor	LOS	R	LOS7	LOS6	LOS5	LOS4	LOS3	LOS2	LOS1	LOS0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
LOS Interrupt Enable	LIE	R/W	LIE7	LIE6	LIE5	LIE4	LIE3	LIE2	LIE1	LIE0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
LOS Interrupt Status	LIS	R	LIS7	LIS6	LIS5	LIS4	LIS3	LIS2	LIS1	LIS0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
Software Reset Register	RES	R/W	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
Digital Loopback	DL	R/W	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
Global Control Register	GCR	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Pulse Shaping Indirect Address Register	PSIAD	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	LENAD2	LENAD1	LENAD0

Table 5. Register Bit Names (Sheet 2 of 2)

Register			Bit							
Name	**Sym**	**RW**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pulse Shaping Data Register	PSDAT	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	LEN2	LEN1	LEN0
Output Enable Register	OER	R/W	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x
Reserved	RSVD	R/W	x	x	x	x	x	x	x	x

Table 6. ID Register, ID (00h)

Bit	Name	Function
7-0	ID7-ID0	This register contains a unique revision code and is mask programmed. For Rev.B1, 21h

Table 7. Analog Loopback Register, ALOOP (01h)

Bit	Name	Function
7-0	AL7-AL0	Setting a bit to “1” enables analog local loopback for transceivers 7- 0 respectively.

Table 8. Remote Loopback Register, RLOOP (02h)

Bit	Name	Function
7-0	RL7-RL0	Setting a bit to “1” enables remote loopback for transceivers 7-0 respectively.

Table 9. Reserved, RSVD(03h)

Bit[1]	Name	Function[2]
0-7	Reserved	Reserved.

1. On power-up all register bits are set to “0”.
2. MCLK is used as timing reference. If MCLK is not available then the channel TCLK is used as the reference.This feature is not available in data recovery and line driver mode (MCLK= High and TCLK = High).

Table 10. LOS Status Monitor Register, LOS (04h)

Bit[1]	Name	Function
7-0	LOS7-LOS0	Respective bit(s) are set to “1” every time the LOS processor detects a valid loss of signal condition in transceivers 7-0.

1. On power-up all register bits are set to “0”. Any change in the state causes an interrupt. All LOS interrupts are cleared by a single read operation.

Table 11. Reserved, RSVD (05h)

Bit	Name	Function[1]
0-7	Reserved	Reserved.
1. On power-up all the register bits are set to “0”. All DFM interrupts are cleared by a single read operation.		

Table 12. LOS Interrupt Enable Register, LIE (06h)

Bit	Name	Function[1]
7-0	LIE7-LIE0	Transceiver 7-0 LOS interrupts are enabled by writing a “1” to the respective bit.
1. On power-up all the register bits are set to “0” and all interrupts are disabled.		

Table 13. Reserved, RSVD (07h)

Bit	Name	Function[1]
0-7	Reserved	Reserved.
1. On power-up all the register bits are set to “0” and all interrupts are disabled.		

Table 14. LOS Interrupt Status Register, LIS (08h)

Bit	Name	Function[1]
7-0	LIS7-LIS0	These bits are set to “1” every time a LOS status change has occurred since the last cleared interrupt in transceivers 7-0 respectively.
1. On power-up all register bits are set to “0”.		

Table 15. Reserved, RSVD (09h)

Bit	Name	Function[1]
0-7	Reserved	Reserved.
1. On power-up all register bits are set to “0”.		

Table 16. Software Reset Register, RES (0Ah)

Bit	Name	Function
7-0	RES7-RES0	Writing to this register initiates a 1 microsecond reset cycle, except in Intel non-multiplexed mode. This operation sets all LXT3008 registers to their default values. When using Intel non-multiplexed host mode, extend cycle time to 2 microseconds. Please refer to Host Mode section for details.

Table 17. Reserved, RSVD (0Bh)

Bit	Name	Function
0-7	Reserved	Reserved.

Table 18. Digital Loopback Register, DL (0Ch)

Bit[1]	Name	Function[2]
7-0	DL7-DL0	Setting a bit to “1” enables digital loopback for the respective transceiver.

1. On power-up all register bits are set to “0”.
2. During digital loopback LOS and TAOS stay active and independent of TCLK, while data received on TPOS/TNEG/CKLK is looped back to RPOS/RNEG/RCLK.

Table 19. Reserved, RSVD (0Dh)

Bit[1]	Name	Function
0-7	Reserved	Reserved.

1. On power-on reset the register is set to “0”.

Table 20. Reserved, RSVD (0Eh)

Bit[1]	Name	Function
0-7	Reserved	Reserved.

1. On power-on reset the register is set to “0”.
2. This feature is not available in data recovery and line driver mode (MCLK= High and TCLK = High).

Table 21. Global Control Register, GCR (0Fh)

Bit[1]	Name	Function
7-0	GCR7 - GCR0	Set to 0 for normal operation.

1. On power-on reset the register is set to “0”.

Table 22. Pulse Shaping Indirect Address Register, PSIAD (10h)

Bit[1]	Name	Function
0-2	LENAD 0-2	The three bit value written to these bits determine the channel to be addressed. Data can be read from (written to) the Pulse Shaping Data Register (PSDAT). LENAD 0-2 / Channel / LENAD 0-2 / Channel 0h / 0 / 4h / 4 1h / 1 / 5h / 5 2h / 2 / 6h / 6 3h / 3 / 7h / 7
3 - 7	-	Reserved.

1. On power-on reset the register is set to “0”.

Table 23. Pulse Shaping Data Register, PSDAT (11h)

<table>
<tr><th>Bit</th><th>Name</th><th colspan="6">Function</th></tr>
<tr><td rowspan="8">0-2</td><td rowspan="8">LEN 0-2[1, 3]</td><td colspan="6">LEN0-2 determine the LXT3008 operation mode: T1 or E1. In addition, for T1 operation, LEN2-0 set the pulse shaping to meet the T1.102 pulse template at the DSX-1 cross-connect point for various cable lengths:</td></tr>
<tr><td>LEN2</td><td>LEN1</td><td>LEN0</td><td>Line Length</td><td>Cable Loss[2]</td><td>Operation Mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0 - 133 ft. ABAM</td><td>0.6 dB</td><td rowspan="5">T1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>133 - 266 ft. ABAM</td><td>1.2 dB</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>266 - 399 ft. ABAM</td><td>1.8 dB</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>399 - 533 ft. ABAM</td><td>2.4 dB</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>533 - 655 ft. ABAM</td><td>3.0 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td colspan="2">E1 G.703, 75Ω coaxial cable and 120Ω twisted pair cable.</td><td>E1</td></tr>
<tr><td>3 - 7</td><td>Reserved</td><td colspan="6">Reserved.</td></tr>
<tr><td colspan="8">1. On power-on reset the register is set to “0”.
2. Maximum cable loss at 772 KHz.
3. When reading LEN, bit values appear inverted. “B2” revision silicon will fix this so the bits read back correctly.</td></tr>
</table>

Table 24. Output Enable Register, OER (12h)

Bit[1]	Name	Function
7-0	OE7 - OE0	Setting a bit to “1” tristates the output driver of the corresponding transceiver.
1. On power-up all the register bits are set to “0”.		

Table 25. Reserved, RSVD (13h)

Bit	Name	Function
7-0	Reserved	Reserved.

Table 26. Reserved, RSVD (14h)

Bit[1]	Name	Function
7-0	Reserved	Reserved.
1. On power-up all the register bits are set to “0”.		

Table 27. Reserved, RSVD (15h)

Bit[1]	Name	Function
7-0	Reserved	Reserved.
1. On power-up all the register bits are set to “0”.		

4.0 JTAG Boundary Scan

4.1 Overview

The LXT3008 supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

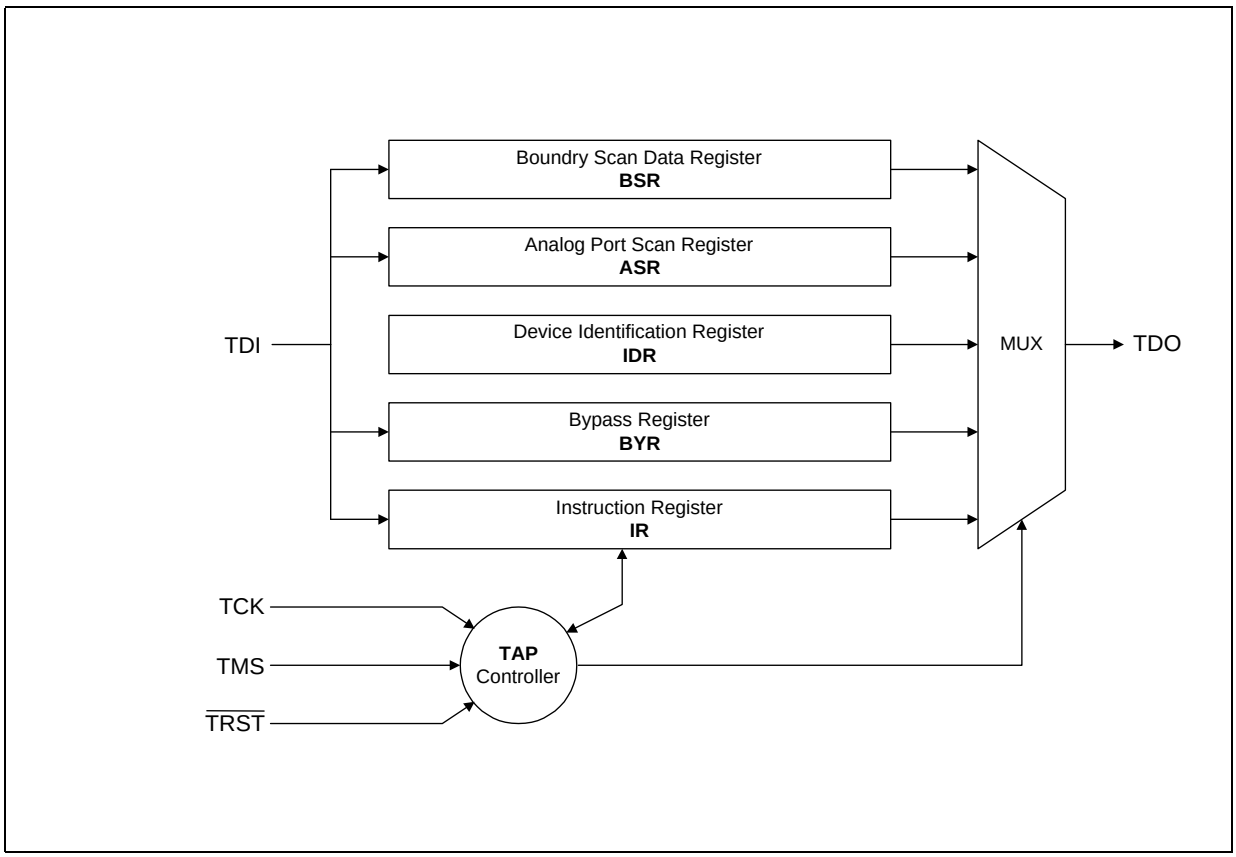
In addition to the traditional IEE1149.1 digital boundary scan capabilities, the LXT3008 also includes analog test port capabilities. This feature provides access to the TIP and RING signals in each channel (transmit and receive). This way, the signal path integrity across the primary winding of each coupling transformer can be tested.

4.2 Architecture

The basic JTAG architecture of the LXT3008 is illustrated in Figure 12.

The LXT3008 JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

Figure 12. JTAG Architecture



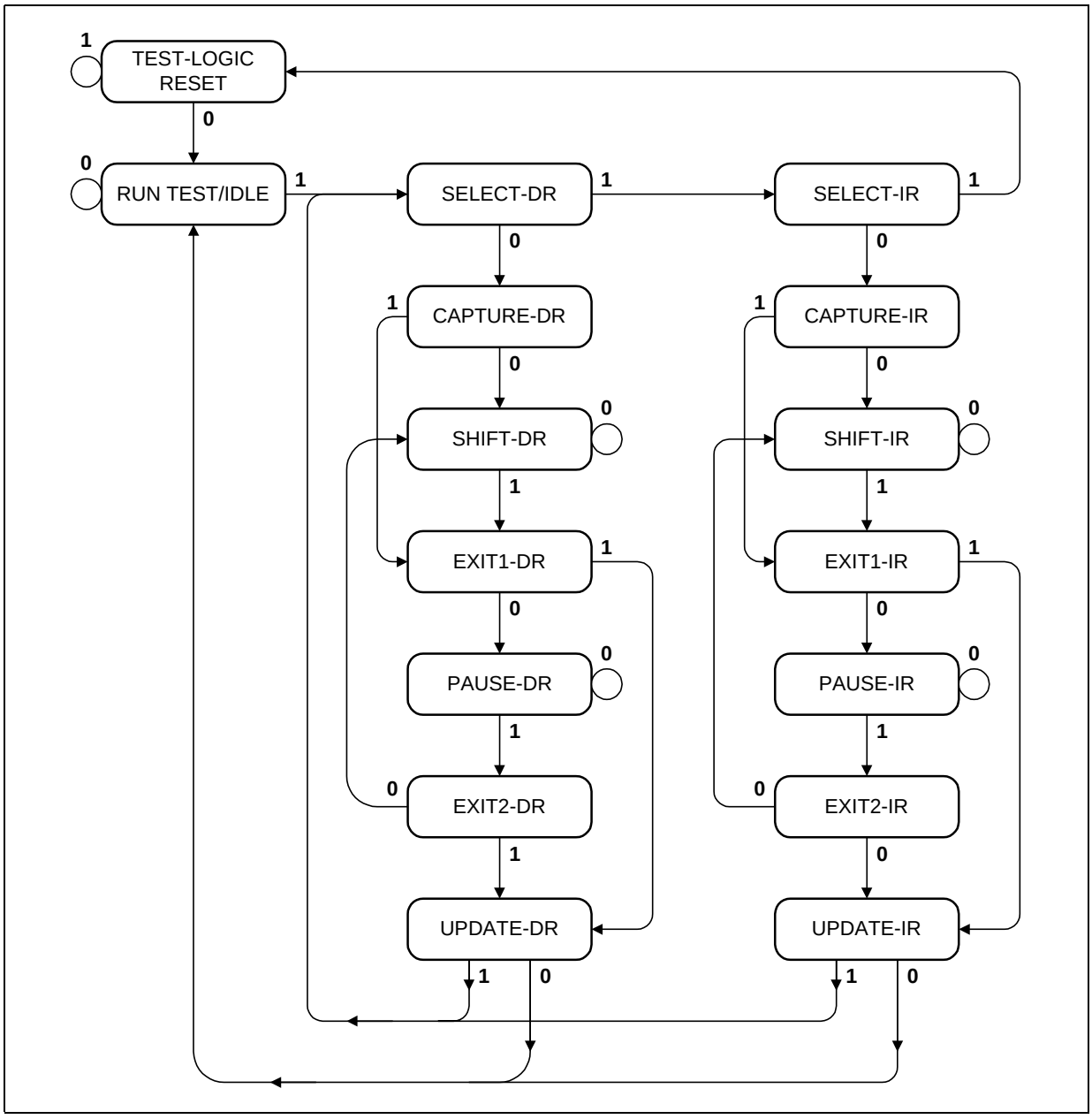
4.3 TAP Controller

The TAP controller is a 16-state synchronous state machine controlled by the TMS input and clocked by TCK (see Figure 13).The TAP controls whether the LXT3008 is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 28 describes in detail each of the states represented in Figure 13.

Table 28. TAP State Description

State	Description
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -Test / Idle	The TAP controller stays in this state as long as TMS is Low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift - DR	Shifts the selected test data registers by one stage tword its serial output.
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

Figure 13. JTAG State Diagram



4.4 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 12.

4.4.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristatable pins require more than one position in the register. Table 29 shows the BSR scan cells and their functions. Data into the BSR is shifted in LSB first.

The analog test port can be used to verify continuity across the coupling transformer's primary winding, as shown in Figure 14. By applying a stimulus to the AT1 input, a known voltage will appear at AT2 for a given load. This, in effect, tests the continuity of a receive or transmit interface.

Table 29. Boundary Scan Register (BSR) (Sheet 1 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
0	LOOP0	I/O	PADD0	
1	LOOP0	I/O	PDO0	
2	LOOP1	I/O	PADD1	
3	LOOP1	I/O	PDO1	
4	LOOP2	I/O	PADD2	
5	LOOP2	I/O	PDO2	
6	LOOP3	I/O	PADD3	
7	LOOP3	I/O	PDO3	
8	LOOP4	I/O	PADD4	
9	LOOP4	I/O	PDO4	
10	LOOP5	I/O	PADD5	
11	LOOP5	I/O	PDO5	
12	LOOP6	I/O	PADD6	
13	LOOP6	I/O	PDO6	
14	LOOP7	I/O	PADD7	
15	N/A	-	PDOENB	PDOENB controls the LOOP0 through LOOP7 pins. Setting PDOENB to "0" configures the pins as outputs. The output value to the pin is set in PDO[0..7]. Setting PDOENB to "1" tristates all the pins. The input value to the pins can be read in PADD[0..7].
16	LOOP7	I/O	PDO7	
17	TCLK1	I	TCLK1	
18	TPOS1	I	TPOS1	
19	TNEG1	I	TNEG1	
20	RCLK1	O	RCLK1	
21	RPOS1	O	RPOS1	
22	N/A	-	HIZ1	HIZ1 controls the RPOS1, RNEG1 and RCLK1 pins. Setting HIZ1 to "0" enables output on the pins. Setting HIZ1 to "1" tristates the pins.
23	RNEG1	O	RNEG1	
24	LOS1	O	LOS1	

Table 29. Boundary Scan Register (BSR) (Sheet 2 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
25	TCLK0	I	TCLK0	
26	TPOS0	I	TPOS0	
27	TNEG0	I	TNEG0	
28	RCLK0	O	RCLK0	
29	RPOS0	O	RPOS0	
30	N/A	-	HIZ0	HIZ0 controls the RPOS0, RNEG0 and RCLK0 pins. Setting HIZ0 to “0” enables output on the pins. Setting HIZ0 to “1” tristates the pins.
31	RNEG0	O	RNEG0	
32	LOS0	O	LOS0	
33	N/A	I	N/A	
34	LOS3	O	LOS3	
35	RNEG3	O	RNEG3	
36	N/A	-	HIZ3	HIZ3 controls the RPOS3, RNEG3 and RCLK3 pins. Setting HIZ3 to “0” enables output on the pins. Setting HIZ3 to “1” tristates the pins.
37	RPOS3	O	RPOS3	
38	RCLK3	O	RCLK3	
39	TNEG3	I	TNEG3	
40	TPOS3	I	TPOS3	
41	TCLK3	I	TCLK3	
42	LOS2	O	LOS2	
43	RNEG2	O	RNEG2	
44	N/A	-	HIZ2	HIZ2 controls the RPOS2, RNEG2 and RCLK2 pins. Setting HIZ2 to “0” enables output on the pins. Setting HIZ2 to “1” tristates the pins.
45	RPOS2	O	RPOS2	
46	RCLK2	O	RCLK2	
47	TNEG2	I	TNEG2	
48	TPOS2	I	TPOS2	
49	TCLK2	I	TCLK2	
50	$\overline{\text{INT}}$	O	INT	
51	N/A	-	SDOACKENB	SDOACKENB controls the $\overline{\text{ACK}}$ pin. Setting SDOACKEN to “0” enables output on $\overline{\text{ACK}}$ pin. Setting SDOACKEN to “1” tristates the pin.
52	SDO	O	SDO	
53	SDI	I	SDI	
54	LEN1	I	LEN1	
55	SCLK/ LEN2	I	SCLK	
56	$\overline{\text{CS}}$	I	CS	

Table 29. Boundary Scan Register (BSR) (Sheet 3 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
57	N/A	I	N/A	
58	TCLK5	I	TCLK5	
59	TPOS5	I	TPOS5	
60	TNEG5	I	TNEG5	
61	RCLK5	O	RCLK5	
62	RPOS5	O	RPOS5	
63	N/A	-	HIZ5	HIZ5 controls the RPOS5, RNEG5 and RCLK5 pins. Setting HIZ5 to “0” enables output on the pins. Setting HIZ5 to “1” tristates the pins.
64	RNEG5	O	RNEG5	
65	LOS5	O	LOS5	
66	TCLK4	I	TCLK4	
67	TPOS4	I	TPOS4	
68	TNEG4	I	TNEG4	
69	RCLK4	O	RCLK4	
70	RPOS4	O	RPOS4	
71	N/A	-	HIZ4	HIZ4 controls the RPOS4, RNEG4 and RCLK4 pins. Setting HIZ4 to “0” enables output on the pins. Setting HIZ4 to “1” tristates the pins.
72	RNEG4	O	RNEG4	
73	LOS4	O	LOS4	
74	$\overline{\text{TXTRST}}$	I	$\overline{\text{TXTRST}}$	
75	CLKE	I	CLKE	
76	LOS7	O	LOS7	
77	RNEG7	O	RNEG7	
78	N/A	-	HIZ7	HIZ7 controls the RPOS7, RNEG7 and RCLK7 pins. Setting HIZ7 to “0” enables output on the pins. Setting HIZ7 to “1” tristates the pins.
79	RPOS7	O	RPOS7	
80	RCLK7	O	RCLK7	
81	TNEG7	I	TNEG7	
82	TPOS7	I	TPOS7	
83	TCLK7	I	TCLK7	
84	LOS6	O	LOS6	
85	RNEG6	O	RNEG6	
86	N/A	-	HIZ6	HIZ6 controls the RPOS6, RNEG6 and RCLK6 pins. Setting HIZ6 to “0” enables output on the pins. Setting HIZ6 to “1” tristates the pins.
87	RPOS6	O	RPOS6	
88	RCLK6	O	RCLK6	

Table 29. Boundary Scan Register (BSR) (Sheet 4 of 4)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
89	TNEG6	I	TNEG6	
90	TPOS6	I	TPOS6	
91	TCLK6	I	TCLK6	
92	REFCLK/ $\overline{\text{RXTRST}}$	I	REFCLK	
93	MODE	I	MODE	
94	N/A	I	N/A	
95	N/A	I	N/A	
96	N/A	I	N/A	
97	N/A	I	N/A	
98	N/A	I	N/A	

4.4.2 Analog Port Scan Register (ASR)

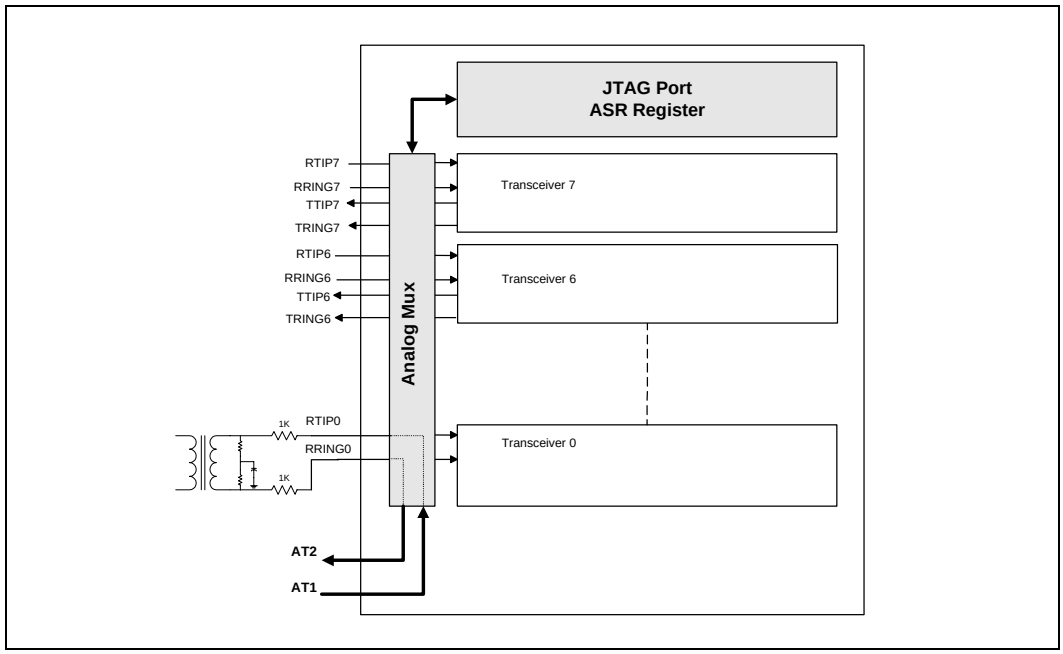
The ASR is a 5 bit shift register used to control the analog test port at pins AT1, AT2. When the INTEST_ANALOG instruction is selected, TDI connects to the ASR input and TDO connects to the ASR output. After 5 TCK rising edges, a 5 bit control code is loaded into the ASR. Data into the ASR is shifted in LSB first.

Table 30 shows the 16 possible control codes and the corresponding operation on the analog port.

Table 30. Analog Port Scan Register (ASR)

ASR Control Code	AT1 Forces Voltage To:	AT2 Senses Voltage From:
11111	TTIP0	TRING0
11110	TTIP1	TRING1
11101	TTIP2	TRING2
11100	TTIP3	TRING3
11011	TTIP4	TRING4
11010	TTIP5	TRING5
11001	TTIP6	TRING6
11000	TTIP7	TRING7
10111	RTIP0	RRING0
10110	RTIP1	RRING1
10101	RTIP2	RRING2
10100	RTIP3	RRING3
10011	RTIP4	RRING4
10010	RTIP5	RRING5
10001	RTIP6	RRING6
10000	RTIP7	RRING7

Figure 14. Analog Test Port Application



4.4.3 Bypass Register (BYR)

The Bypass Register is a 1-bit register that allows direct connection between the TDI input and the TDO output.

4.4.4 Instruction Register (IR)

The IR is a 3-bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 31 shows the valid instruction codes and the corresponding instruction description.

Table 31. Instruction Register (IR)

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/sensing through AT1 and AT2. Refer to Table 30.
SAMPLE / PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the LXT3008 logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

5.0 Test Specifications

Note: Table 32 through Table 45 and Figure 15 through Figure 21 represent the performance specifications of the LXT3008 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 34 through Table 45 are guaranteed over the recommended operating conditions specified in Table 33.

Table 32. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max	Unit
DC supply voltage	Vcc0, Vcc1, Vccio0, Vccio1	-0.5	4.0	V
DC supply voltage	Tvcc 0-7	-0.5	7.0	V
Input voltage on any digital pin	Vin	GND-0.5	5.5	V
Input voltage on RTIP, RRING[1]	Vin	GND-0.5	Vcc0 + 0.5 Vcc1 + 0.5	V
ESD voltage on any Pin [2]	Vin	2000	–	V
Transient latch-up current on any pin	Iin		100	mA
Input current on any digital pin [3]	Iin	-10	10	mA
DC input current on TTIP, TRING [3]	Iin	–	±100	mA
DC input current on RTIP, RRING [3]	Iin	–	±100	mA
Storage temperature	Tstor	-65	+150	°C
Maximum power dissipation in package	P_P		1.6	W
Case Temperature, 160 pin PBGA package	T_{case}		120	°C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Referenced to ground.
2. Human body model.
3. Constant input current.

Table 33. Recommended Operating Conditions

Parameter	LEN	Sym	Min.	Typ	Max	Unit	Test Condition
Digital supply voltage (VCC and VCCIO)	-	VCC	3.135	3.3	3.465	V	3.3V ± 5%
Transmitter supply voltage, TVCC=5V nominal	-	TVCC	4.75	5.0	5.25	V	5V ± 5%
Ambient operating temperature	-	Ta	-40	25	+85	°C	
Average transmitter power supply current, T1 Mode [1, 2,4]		I_{TVCC}	-	440 230	490 -	mA mA	100% 1's density 50% 1's density

1. Current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable length (LEN = 101).
3. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.
4. Only applicable when device is in backup mode.
5. Applicable in both standby and backup mode.

Table 33. Recommended Operating Conditions (Continued)

Parameter		LEN	Sym	Min.	Typ	Max	Unit	Test Condition
Average digital power supply current [1, 3,5]			I_{VCC}	-	90	120	mA	
Output load at TTIP and TRING			Rl	25	–	–	Ω	
Device Power Consumption								
Mode	**TVCC**	**Load**	**LEN**			**Typ**	**Max[1]**	**Unit**	**Test Conditions**
E1	5.0/3.3 V	75 Ω	000	-	-	760	-	mW	50% 1's
				-	-	1270	1420	mW	100% 1's
		120 Ω	000	-	-	640	-	mW	50% 1's
				-	-	1110	1280	mW	100% 1's
T1[2]	5.0V	100 Ω	101-111	-	-	1020	-	mW	50% 1's
				-	-	1820	2100	mW	100% 1's

1. Current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable length (LEN = 101).
3. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.
4. Only applicable when device is in backup mode.
5. Applicable in both standby and backup mode.

Table 34. DC Characteristics (Sheet 1 of 2)

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
High level input voltage		V_{IH}	2	–	–	V	
Low level input voltage		V_{IL}	–	–	0.8	V	
High level output voltage[1]		V_{OH}	2.4	–	VCCIO	V	I_{OUT}= 400µA
Low level output voltage[1]		V_{OL}	–	–	0.4	V	I_{OUT}= 1.6mA
MODE, LOOP0-7	Low level input voltage	Vinl	–	–	1/3VCC-0.2	V	The VCC supply refers to VCC0 or VCC1 only.
	Midrange level input voltage	Vinm	1/3VCC+0.2	1/2VCC	2/3VCC-0.2	V	
	High level input voltage	Vinh	2/3VCC+0.2	–	–	V	
	Low level input current	Iinl	–	–	50	µA	
	High level input current	Iinh	–	–	50	µA	
Input leakage current		Iil	-10		+10	µA	
Tri state leakage current		Ihz	-10		+10	µA	

1. Output drivers will output CMOS logic levels into CMOS loads.

Table 34. DC Characteristics (Sheet 2 of 2)

Parameter	Sym	Min.	Typ	Max	Unit	Test Condition
Tri state output current	Ihz	–	–	1	µA	TTIP, TRING
Line short circuit current	–	–	–	50	mA RMS	2 x 11 Ω series resistors and 1:2 transformer
Input leakage	TMS TDI TRST	–	–	50	µA	
1. Output drivers will output CMOS logic levels into CMOS loads.						

Table 35. E1 Transmit Transmission Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test Condition
Output pulse amplitude	75 Ω 120 Ω	–	2.14 2.7	2.37 3.0	2.60 3.3	V V	Tested at the line side
Peak voltage of a space	75 Ω 120 Ω	–	-0.237 -0.3		0.237 0.3	V V	
Transmit amplitude variation with supply		–	-1		+1	%	
Difference between pulse sequences		–			200	mV	For 17 consecutive pulses
Pulse width ratio of the positive and negative pulses		–	0.95		1.05		At the nominal half amplitude
Transmit transformer turns ratio for 75/120Ω characteristic impedance		–		1:2			Rt = 11 Ω ± 1%
Transmit return loss 75 Ω coaxial cable[1]	51 KHz to 102 KHz 102 KHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	17 17 17	–	dB dB dB	
Transmit return loss 120 Ω twisted pair cable[1]	51 KHz to 102 KHz 102 KHz to 2.048 MHz 2.048 MHz to 3.072 MHz	–	15 15 15	20 20 20	–	dB dB dB	Using components in the LXD3008 evaluation board
Transmit intrinsic jitter; 20 Hz to 100 KHz		–	–	0.03	0.05	U.I.	Tx path TCLK is jitter free
1. Guaranteed by design and other correlation methods.							

Table 36. E1 Receive Transmission Characteristics (Sheet 1 of 2)

Parameter	Sym	Min.	Typ	Max	Unit	Test Condition
Permissible cable attenuation	–	–	–	12	dB	@1024 kHz
Receiver dynamic range	DR	0.5	–	–	Vp	
Signal to noise interference margin	S/I	-15	–	–	dB	Per G.703, O.151 @ 6 dB cable Attenuation
1. Guaranteed by design and other correlation methods.						

Table 36. E1 Receive Transmission Characteristics (Sheet 2 of 2)

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Data decision threshold		SRE	43	50	57	%	Rel. to peak input voltage
Data slicer threshold		–	–	150	–	mV	
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	–	32	–	–	G.775 recommendation
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance [1]	1 Hz to 20 Hz 20 Hz to 2.4 KHz 18 KHz to 100 KHz	–	36 1.5 0.2	–	–	U.I. U.I. U.I.	G735 recommendation Note 1 Cable Attenuation is 6 dB
Differential receiver input impedance		–	–	70	–	k Ω	@1.024 MHz
Input termination resistor tolerance		–	–	–	±1	%	
Common mode input impedance to ground		–	–	20	–	K Ω	
LOS delay time		–	–	30	–	µs	Data recovery mode
LOS reset		–	10	–	255	marks	Data recovery mode
Receive intrinsic jitter, RCLK output		–	–	0.040	0.0625	U.I.	Wide band jitter
Receive path delay				1		U.I.	

1. Guaranteed by design and other correlation methods.

Table 37. T1 Transmit Transmission Characteristics

Parameter	Sym	Min.	Typ	Max	Unit	Test Condition
Output pulse amplitude	–	2.4	3.0	3.6	V	Measured at the DSX
Peak voltage of a space	–	-0.15	–	+0.15	V	
Driver output impedance[1]	–	–	1	–	Ω	@ 772 KHz
Transmit amplitude variation with power supply	–	-1	–	+1	%	
Ratio of positive to negative pulse amplitude	–	0.95	–	1.05	–	T1.102, isolated pulse
Difference between pulse sequences	–	–	–	200	mV	For 17 consecutive pulses, GR-499-CORE
Pulse width variation at half amplitude	–	–	–	20	ns	

1. Guaranteed by design and other correlation methods.
2. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 37. T1 Transmit Transmission Characteristics (Continued)

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Jitter added by Transmitter[1]	10 Hz - 8 KHz 8 KHz - 40 KHz 10 Hz - 40 KHz Wide Band	–	–	–	0.020 0.025 0.025 0.050	UI_{pk-pk}	AT&T Pub 62411 TCLK is jitter free
Output power levels[2]	@ 772 KHz @ 1544 KHz	–	12.6 -29	–	17.9	dBm dBm	T1.102 - 1993 Referenced to power at 772 KHz
Transmit path delay				2		U.I.	

1. Guaranteed by design and other correlation methods.
2. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 38. T1 Receive Transmission Characteristics

Parameter		Sym	Min.	Typ	Max	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@ 772 KHz
Receiver dynamic range		DR	0.5	–	–	Vp	
Signal to noise interference margin		S/I	-16.5	–	–	dB	@ 655 ft. of 22 ABAM cable
Data decision threshold		SRE	63	70	77	%	Rel. to peak input voltage
Data slicer threshold		–	–	150	–	mV	
Loss of signal threshold		–	–	200	–	mV	
LOS hysteresis		–	–	50	–	mV	
Consecutive zeros before loss of signal		–	100	175	250	–	T1.231 - 1993
LOS reset		–	12.5%	–	–	–	1's density
Low limit input jitter tolerance [1]	0.1 Hz to 1 Hz 4.9 Hz to 300 Hz 10 KHz to 100 KHz	-	138 28 0.4	-	-	U.I. U.I. U.I.	AT&T Pub. 62411
Differential receiver input impedance		-	-	70	-	KΩ	@772 kHz
Input termination resistor tolerance		-	-		±1	%	
Common mode input impedance to ground		-	-	20	-	KΩ	
Input return loss[1]	51 KHz - 102 KHz 102 - 2048 KHz 2048 KHz - 3072 KHz	-	20 20 20	-	-	dB dB dB	Measured against nominal impedance. Using components in the LXD3008 evaluation board.
LOS delay time		-	-	30	-	µs	Data recovery mode
LOS reset		-	10	-	255	-	Data recovery mode
Receive intrinsic jitter, RCLK output[1]		-	-	0.035	0.0625	U.I.	Wide band jitter
Receive path delay				1		U.I.	

1. Guaranteed by design and other correlation methods.

Table 39. Analog Test Port Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
3 dB bandwidth	At13dB	-	5	-	MHz	
Input voltage range	$AT1_{IV}$	0	-	VCC0 VCC1	V	
Output voltage range	$AT2_{OV}$	0	-	VCC0 VCC1	V	

Table 40. Transmit Timing Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test Condition
Master clock frequency	E1	MCLK	–	2.048	–	MHz	
	T1	MCLK	–	1.544	–	MHz	
Master clock tolerance		–	-100	–	100	ppm	
Master clock duty cycle		–	40	–	60	%	
Output pulse width	E1	t_W	219	244	269	ns	
	T1	t_W	291	324	356	ns	
Transmit clock frequency	E1	$TCLK_{E1}$	-	2.048	-	MHz	
	T1	$TCLK_{T1}$	-	1.544	-	MHz	
Transmit clock tolerance		$TCLK_T$	-50	–	+50	ppm	
Transmit clock duty cycle		t_{DC}	10	–	90	%	NRZ mode
TPOS/TNEG to TCLK setup time		t_{SUT}	20	-	-	ns	
TCLK to TPOS/TNEG hold time		t_{HT}	20	-	-	ns	
Delay time $\overline{TXTRST}$ Low to driver High Z		t_{OEZ}	-	-	1	µs	
Delay time TCLK Low to driver High Z		t_{TZ}	50	60	75	µs	

Figure 15. Transmit Clock Timing Diagram

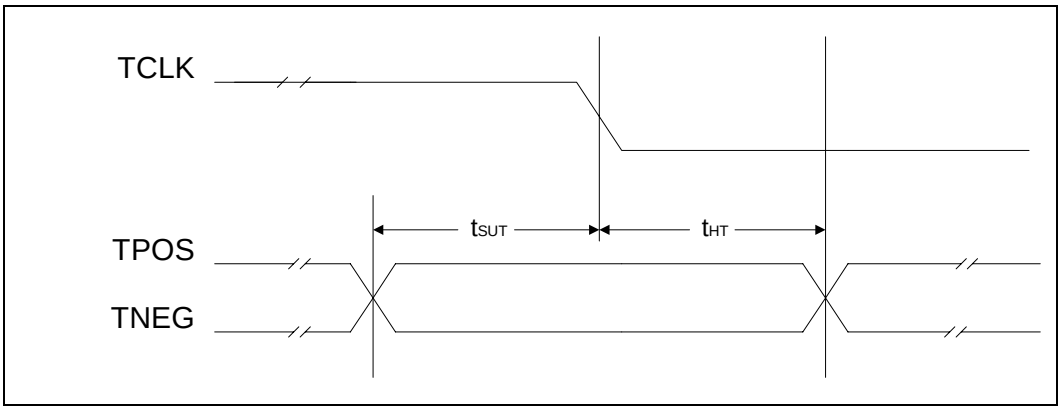


Table 41. Receive Timing Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test Condition
Clock recovery capture range	E1	–	–	±80	–	ppm	Relative to nominal frequency MCLK = ±100 ppm
	T1	–	–	±180	–	ppm	
Receive clock duty cycle [1]		DC_{RCLK}	40	50	60	%	
Receive clock pulse width [1]	E1	t_{PW}	447	488	529	ns	
	T1	t_{PW}	583	648	713	ns	
Receive clock pulse width Low time	E1	t_{PWL}	203	244	285	ns	
	T1	t_{PWL}	259	324	389	ns	
Receive clock pulse width High time	E1	t_{PWH}	203	244	285	ns	
	T1	t_{PWH}	259	324	389	ns	
Rise/fall time [2]		t_R	20	–	–	ns	@ CL=15 pF
RPOS/RNEG to RCLK rising setup time	E1	t_{SUR}	200	244	–	ns	
	T1		200	324	–	ns	
RCLK Rising to RPOS/RNEG hold time	E1	t_{HR}	200	244	–	ns	
	T1		200	324	–	ns	

1. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).
2. For all digital outputs.

Figure 16. Receive Clock Timing Diagram

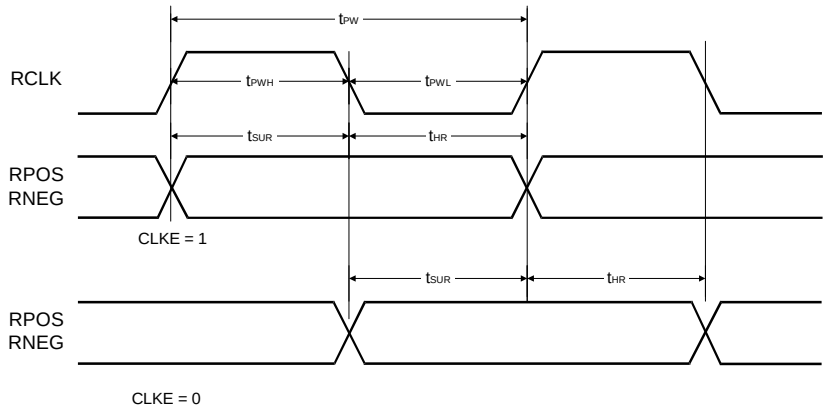


Table 42. JTAG Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Cycle time	t_{CYC}	200	-	-	ns	
J-TMS/J-TDI to J-TCK rising edge time	t_{SUT}	50	-	-	ns	
J-CLK rising to J-TMS/L-TDI hold time	t_{HT}	50	-	-	ns	
J-TCLK falling to J-TDO valid	t_{DOD}	-	-	50	ns	

Figure 17. JTAG Timing

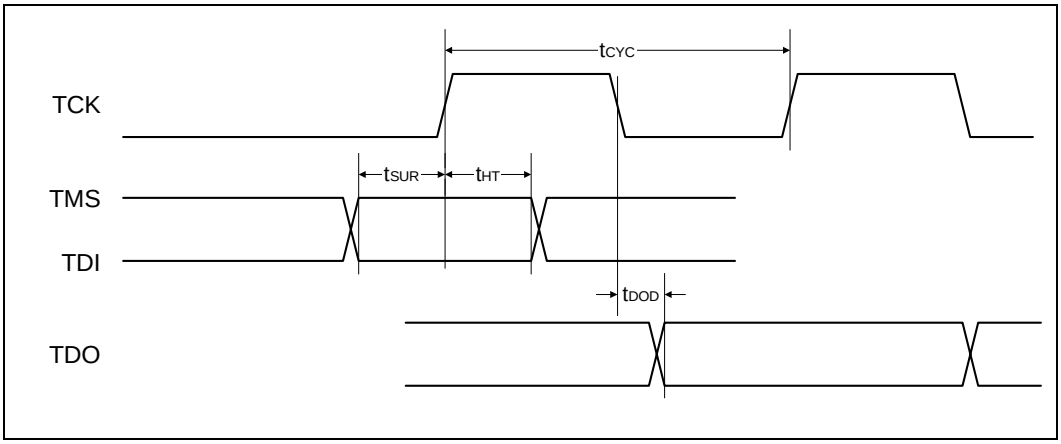


Table 43. Serial I/O Timing Characteristics

Parameter	Symbol	Min	Typ [1]	Max	Unit	Test Condition
Rise/fall time any pin	t_{RF}	-	-	100	ns	Load 1.6mA, 50 pF
SDI to SCLK setup time	t_{DC}	5	-	-	ns	
SCLK to SDI hold time	t_{CDH}	5	-	-	ns	
SCLK Low time	t_{CL}	25	-	-	ns	
SCLK High time	t_{CH}	25	-	-	ns	
SCLK rise and fall time	t_R, t_F	-	-	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	t_{CC}	10	-	-	ns	
Last SCLK edge to $\overline{CS}$ rising edge	t_{CCH}	10	-	-	ns	
$\overline{CS}$ inactive time	t_{CWH}	50	-	-	ns	
SCLK to SDO valid delay time	t_{CDV}	-	-	5	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO High-Z	t_{CDZ}	-	10	-	ns	
1. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 18. Serial Input Timing

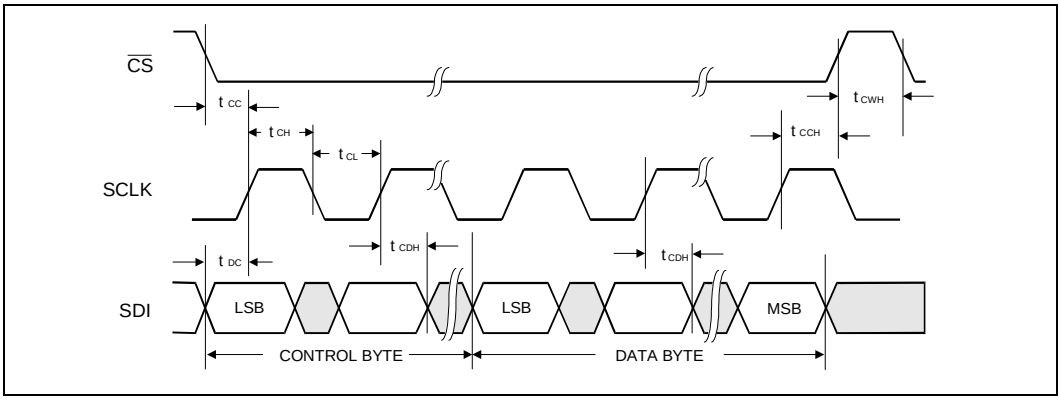


Figure 19. Serial Output Timing

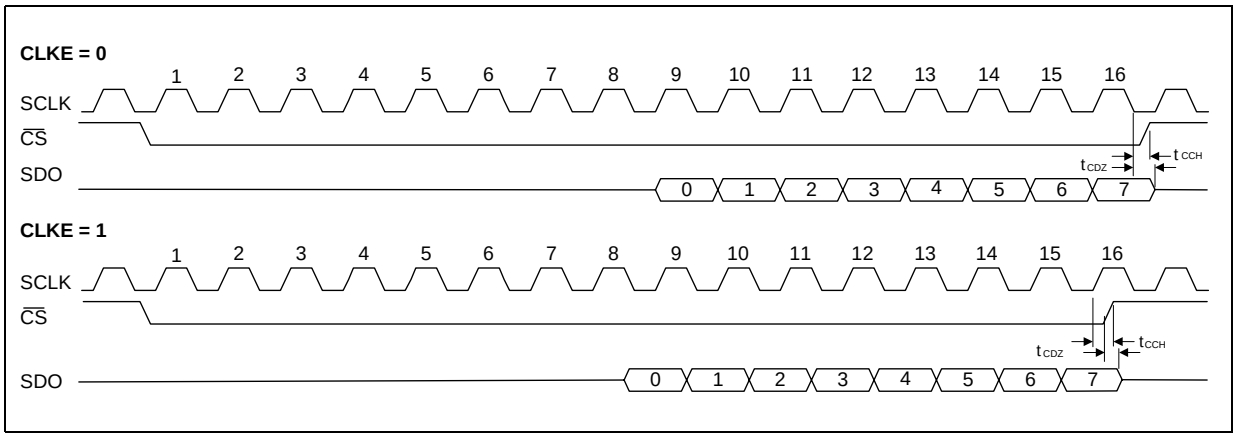


Table 44. G.703 2.048 Mbps Pulse Mask Specifications

Parameter	Cable		Unit
	TWP	Coax	
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 20. E1, G.703 Mask Templates

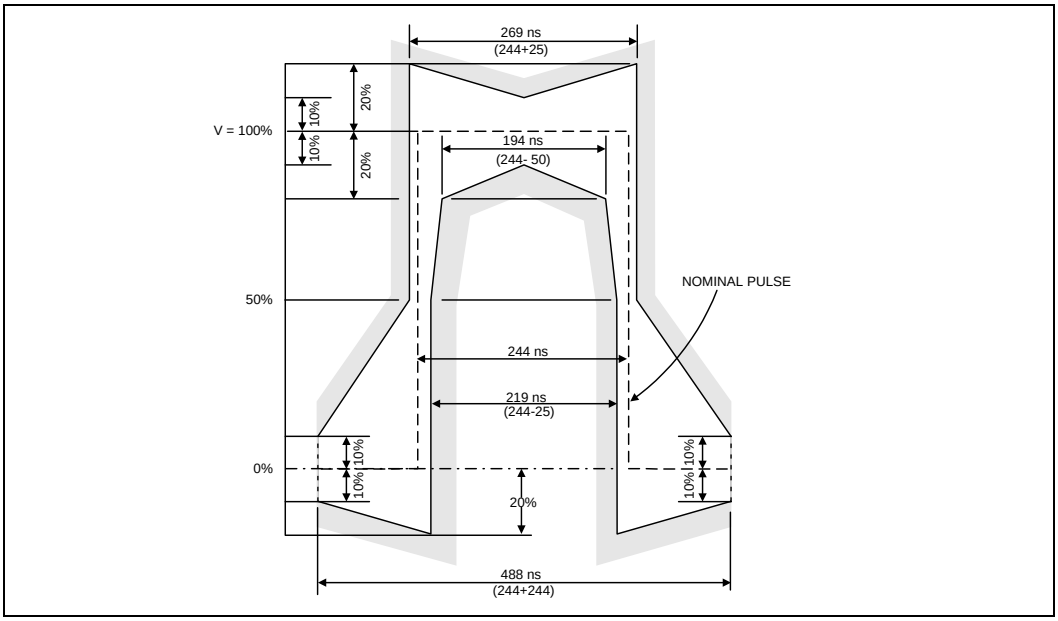
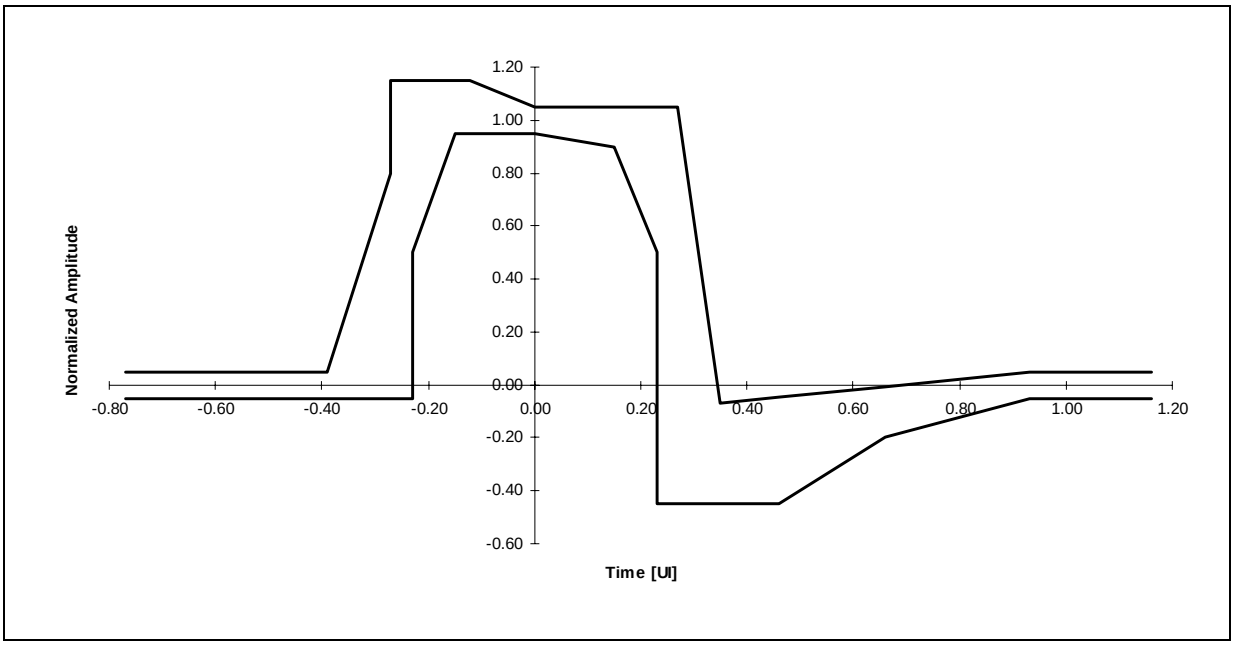


Table 45. T1.102 1.544 Mbps Pulse Mask Specifications

Parameter	Cable	Unit
	TWP	
Test load impedance	100	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ± 0.15	V
Nominal pulse width	324	ns
Ratio of positive and negative pulse amplitudes	95-105	%

Figure 21. T1, T1.102 Mask Templates

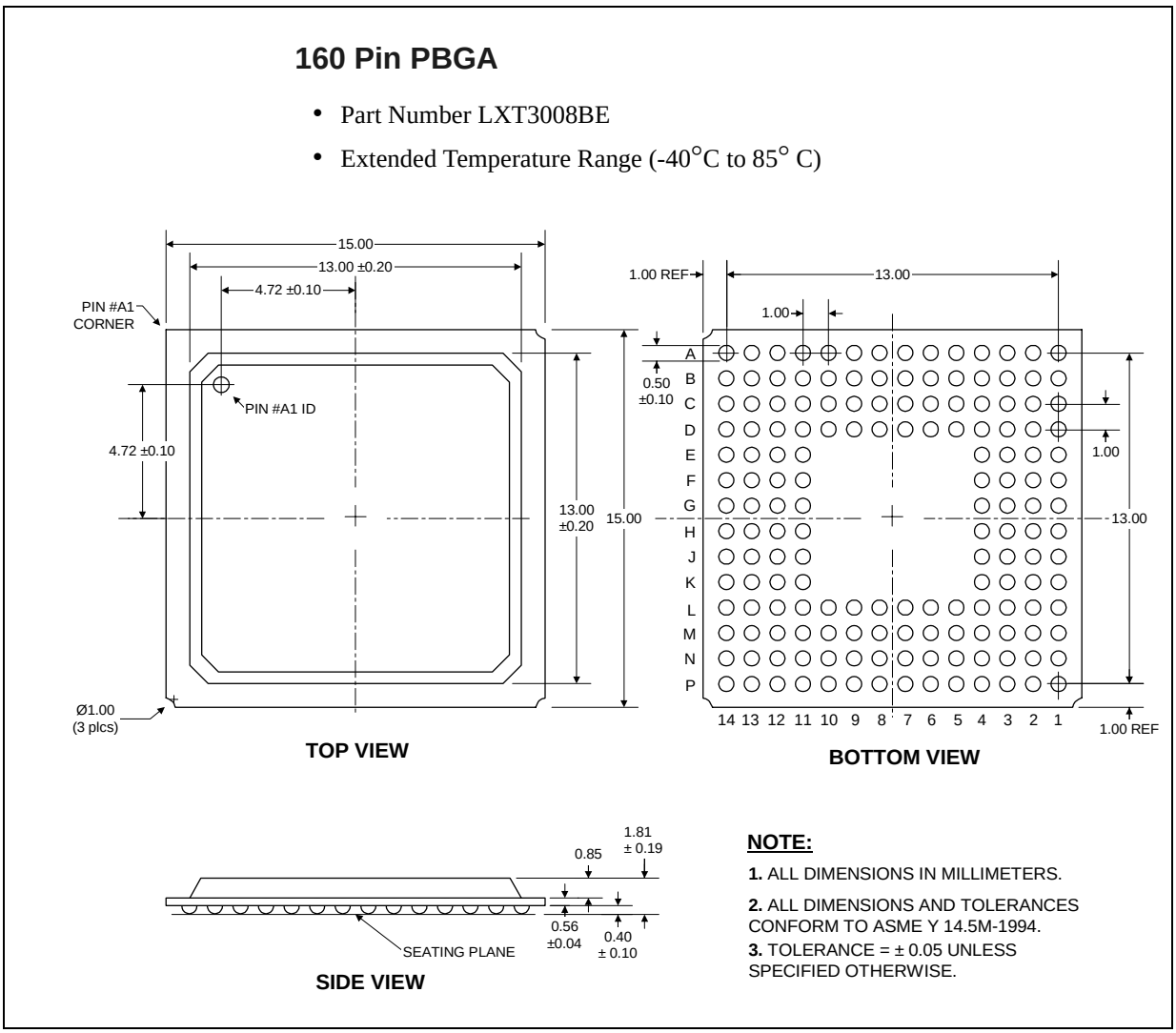


5.1 Recommendations and Specifications

- AT&T Pub 62411
- ANSI T1.102 - 199X Digital Hierarchy Electrical Interface
- ANSI T1.231 -1993 Digital Hierarchy Layer 1 In-Service Digital Transmission Performance Monitoring
- Bellcore TR-TSY-000009 Asynchronous Digital Multiplexes Requirements and Objectives
- Bellcore GR-253-CORE SONET Transport Systems Common Generic Criteria
- Bellcore GR-499-CORE Transport Systems Generic Requirements
- ETS 300166 Physical and Electrical Characteristics
- ETS 300386-1 Electromagnetic Compatibility Requirement
- G.703 Physical/electrical characteristics of hierarchical digital interfaces
- G.704 Functional characteristics of interfaces associated with network nodes
- G.735 Characteristics of Primary PCM multiplex equipment operating at 2048 Kbps and offering digital access at 384 Kbps and/or synchronous digital access at 64 Kbps
- G.736 Characteristics of a synchronous digital multiplex equipment operating at 2048 kbps
- G.772 Protected Monitoring Points provided on Digital Transmission Systems
- G.775 Loss Of Signal (LOS) and alarm indication (AIS) defect detection and clearance criteria
- G.783 Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks
- G.823 The control of jitter and wander within digital networks which are based on the 2048 Kbps hierarchy
- O.151 Specification of instruments to measure error performance in digital systems
- OFTEL OTR-001 Short Circuit Current Requirements

6.0 Mechanical Specifications

Figure 22. Plastic Ball Grid Array (PBGA) Package Dimensions



7.0 Glossary

Term Categories

Term	Term Definition
BYR	Bypass Register
FPF	Finish Process Order
IR	Instruction Register
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
LIU	Line Interface Unit
LOS	Loss of Signal
NRZ	Non Return to Zero
OER	Output Enable Register
PBGA	Plastic Ball Grid Array
PIU	Protection Interface Unit
PSDAT	Pulse Shaping Data Register
RES	RESet register
SH	Short Haul
SONET/SDH	Sychronous Optical NETwork/Sychronous Digital Hiearchy
TAP	Test Access Port