LXT307

Low-Power E1 Integrated Short-Haul Transceiver

Datasheet

The LXT307 is a fully integrated low-power transceiver optimized for G.703 2.048 Mbps (E1) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss. Transmit pulse amplitudes are selectable for various cable types. It is designed to exceed the latest international specifications, including G.775 and ETS 300 166.

The LXT307 is microprocessor controllable through a serial interface. It can also be controlled through individual pins in Hardware Mode.

The LXT307 offers a variety of diagnostic features, including transmit and receive monitoring. The device requires a single 2.048 MHz clock reference for the on chip high performance clock recovery system. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

Applications

- PCM G.703 Interfaces
- E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- G.703 Trunk line cards for Public Switching Systems and PABX
- High-speed data transmission lines

Product Features

- Low power dissipation 260 mW typical
- Constant low output impedance transmitter regardless of data pattern (3 Ω typical)
- Low speed reference clock to reduce PC board noise coupling
- Driver short circuit current limited to 50 mA per OFTEL/BABT recommendations
- 75/120 Ω operation without component changes
- Transmit and receive return loss exceeds ETSI ETS 300 166 and G.703
- Meets or exceeds all ITU specifications including G.703, G.823 (03/93) and G.775
- Compatible with most popular PCM framers
- Line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV
- Programmable transmit amplitude for 75 Ω and 120 Ω operation without component changes
- Local and remote loopback functions
- Transmit performance monitor with DPM detecting single line shorts for improved reliability
- Analog/digital LOS monitor per G.775
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Serial control interface
- Available in 28-pin DIP or PLCC

As of January 15, 2001, this document replaces the Level One document *LXT307 — Low-Power E1 Integrated Short-Haul Transceiver*.

Order Number: 249069-001
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Datasheet

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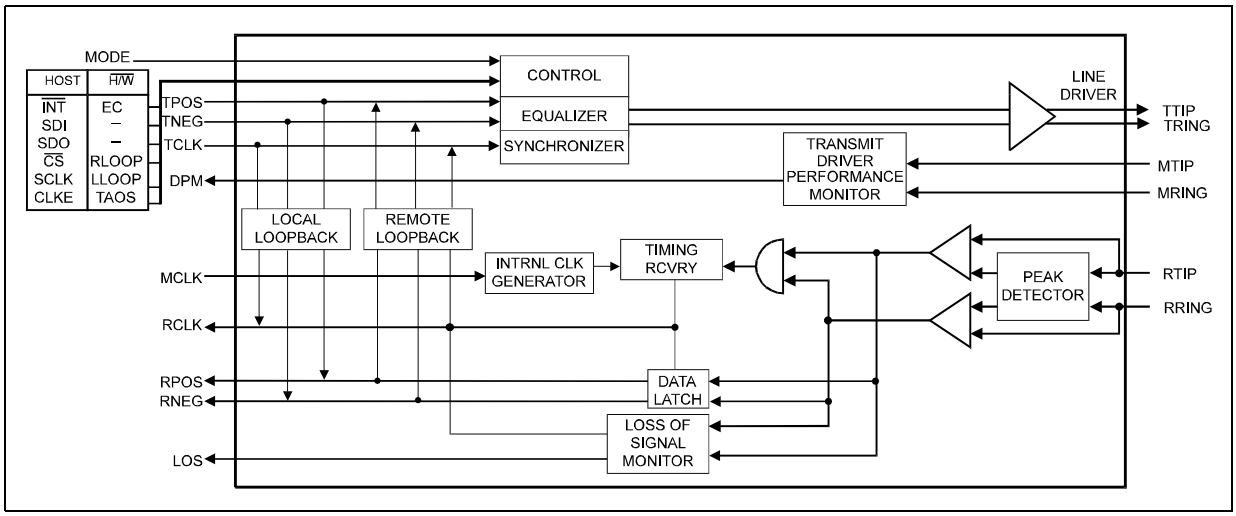
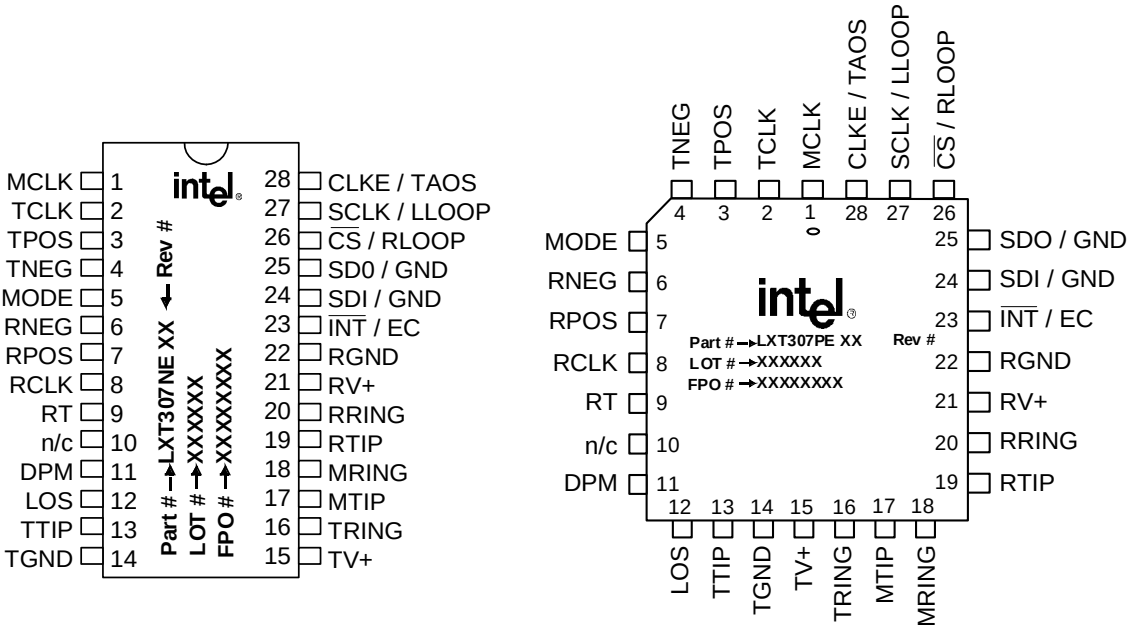
Figure 1. LXT307 Block Diagram



1.0 Pin Assignment and Signal Description

Figure 2. LXT384 Pin Assignments and Package Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Pin Assignments and Signal Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock.** A 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2	TCLK	DI	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down.
3	TPOS	DI	**Transmit Positive Data.** Input for the positive pulse to be transmitted on the line.
4	TNEG	DI	**Transmit Negative Data.** Input for the negative pulse to be transmitted on the line.
5	MODE	DI	**Mode Select.** Setting MODE High puts the LXT307 in the Host Mode. In the Host Mode, the serial interface is used to control the LXT307 and determine its status. Setting MODE Low puts the LXT307 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
6	RNEG	DO	**Receive Negative Data; Receive Positive Data.** Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode, both outputs are stable and valid on the rising edge of RCLK.
7	RPOS	DO	
8	RCLK	DO	**Recovered Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	RT	AI	**Resistor Termination.** Connect to RV+ through a 1k Ω resistor.
10	n/c	–	No connection.
11	DPM	DO	**Driver Performance Monitor.** DPM goes High when the transmit monitor (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains High until a signal is detected. It is reset to Low upon the first transition on MTIP and MRING.
12	LOS	DO	**Loss of Signal.** LOS goes High when the signal falls 20 dB below nominal for more than 175 consecutive bit periods. LOS returns Low when the received signal detects 4 transitions in any 32-bit window (12.5% 1s density) with no more than 15 consecutive 0s.
13	TTIP	AO	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These low-impedance outputs achieve high return loss when series resistors are used along with a transformer as specified in Table 9 and Table 10.
16	TRING	AO	
14	TGND	–	**Transmit Ground.** Ground return for the transmit driver power supply TV+.
15	TV+	S	**Transmit Power Supply.** +5 VDC power supply for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V during all operating conditions including start-up.
17	MTIP	AI	**Monitor Tip; Monitor Ring.** These pins are used to monitor the TTIP and TRING transmit outputs. The transceiver can be connected to monitor its own output or the output of another LXT307 on the board. To prevent false interrupts in the host mode, when the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to the clock's approximate midrange voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
18	MRING	AI	
19	RTIP	AI	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer for 75 Ω and 120 Ω is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS, RNEG and RCLK pins.
20	RRING	AI	
21	RV+	S	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	S	**Receive Ground.** Ground return for power supply RV+.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

Table 1. Pin Assignments and Signal Descriptions (Continued)

Pin #	Sym	I/O[1]	Description
23	$\overline{\text{INT}}$	DO	**Interrupt *(Host Mode)*.** This LXT307 Host mode output goes Low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM).
	EC	DI	**Equalizer Control *(H/W Mode)*.** In LXT307 Hardware mode, the signal applied at this pin is used to determine the amplitude of AMI transmit pulses.
24	SDI	DI	**Serial Data In *(Host Mode)*.** The serial data input stream is applied to this pin when the LXT307 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	GND	DI	**Ground *(H/W Mode)*.** Signal ground.
25	SDO	DO	**Serial Data Out *(Host Mode)*.** Serial data from the on-chip register is output on this pin in LXT307 Host mode. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{\text{CS}}$ is High.
	GND	DI	**Ground *(H/W Mode)*.** Signal ground.
26	$\overline{\text{CS}}$	DI	**Chip Select *(Host Mode)*.** This input is used to access the LXT307 serial interface in Host mode. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
	RLOOP	DI	**Remote Loopback *(H/W Mode)*.** This input controls loopback functions in LXT307 Hardware mode. Setting RLOOP to a logic High enables the Remote Loopback mode. Setting both RLOOP and LLOOP High causes a Reset.
27	SCLK	DI	**Serial Clock *(Host Mode)*.** This clock is used in LXT307 Host mode to write data to or read data from the serial interface registers.
	LLOOP	DI	**Local Loopback *(H/W Mode)*.** This input controls loopback functions in LXT307 Hardware mode. Setting LLOOP High enables the Local Loopback Mode.
28	CLKE	DI	**Clock Edge *(Host Mode)*.** In Host mode, setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	DI	**Transmit All Ones *(H/W Mode)*.** In Hardware mode, TAOS High causes the LXT307 to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes the TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

1. Entries in I/O column are: DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

2.0 Functional Description

The LXT307 is a fully integrated PCM transceiver for G.703 2.048 Mbps (E1) applications. A simplified block diagram of the transceiver is shown on page 1. The LXT307 allows full-duplex transmission of digital data over existing twisted-pair or coax installations. It interfaces with two lines, one for receive, one for transmit.

2.1 Power Requirements

The LXT307 is a low-power CMOS device. It operates from a single +5 V power supply that can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±0.3 V of each other, and decoupled separately to their respective grounds. Isolation between transmit and receive circuits is provided internally. During normal operation and local loopback (LLOOP), the transmitter powers down if TCLK is not supplied. The transmitter also powers down during transmit all ones (TAOS) operation when TCLK is not supplied.

2.2 Reset Operation

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and locks the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines The transmitter reference is provided by TCLK. MCLK is used as the receiver reference clock.

The transceiver can also be reset from either Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. The reset is then initiated on the falling edge of the reset command. In either mode, reset clears and sets all registers to 0 and then calibration begins.

2.3 Receiver

The LXT307 receives the signal input from one twisted-pair or one coax cable on each side of a center-grounded transformer. Positive pulses are detected at RTIP and negative pulses are detected at RRING.

The signal received at RTIP and RRING is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is 50% and is maintained over the entire input range.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The data and clock recovery circuits are highly tolerant with an input jitter tolerance significantly better than required by G.823 (see Figure 18). Recovered clock signals are supplied to the data latch. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 15 and Figure 14 for LXT307 receiver timing.

2.4 Loss of Signal Processor

2.4.1 Declaring the LOS Condition

Recommendation G.775 defines basic criteria for detection and clearance of Loss of Signal (LOS) defects. LOS detection is summarized in Table 2.

The LXT307 uses a digital-and-analog detection scheme to comply with G.775. If the signal level falls 20 dB below nominal, the LXT307 begins to count consecutive bit times and declares LOS after approximately 175 (160 to 190) consecutive zeros.

2.4.2 Clearing the LOS Condition

The LXT307 uses the following three-step process to determine when the LOS condition is clear:

1. The signal must first exceed the 20 dB signal level.
2. Then a 32-bit repeating window checks for 12.5% 1s density. (To meet this parameter, there must be at least four 1s out of the 32 bits in the window.)
3. Finally, there must be no more than 15 consecutive 0s to clear the LOS condition.

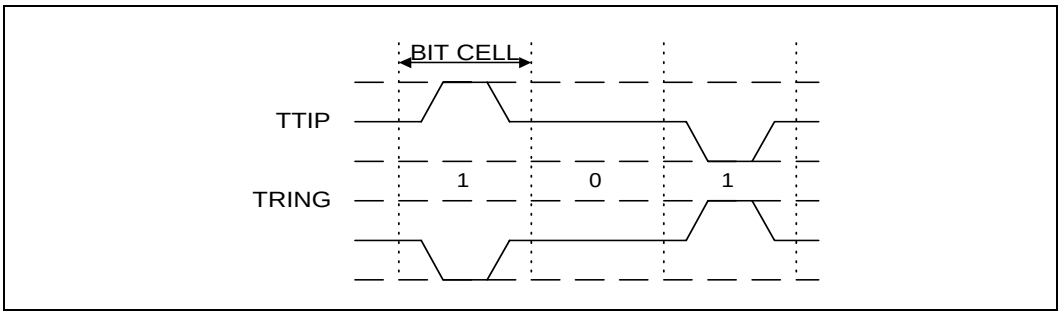
2.5 Transmitter

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). If TCLK is not supplied, the transmitter remains powered down, except during remote loopback and TAOS. Refer to Table 16 and Figure 15 for master and transmit clock timing characteristics.

2.5.1 Line Code

The LXT307 transmits data as a 50% AMI line code as shown in Figure 3. The output driver maintains a constant low output impedance under dynamic conditions regardless of whether it is driving marks or spaces.

Figure 3. 50% AMI Coding



The transmitted pulse amplitude is determined by the equalizer control signal (EC) as shown in Table 3.

The equalizer control signal may be hardwired (in Hardware mode) or input as part of the serial data stream (SDI) when in Host mode. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of 3 Ω (typical). This well-controlled output impedance provides excellent return loss when used with external precision resistors (±1% accuracy) in series with a transmit transformer. Series resistors also provide increased surge protection and reduce short circuit current flow.

Pulses can drive coaxial or shielded twisted-pair lines. A 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all ETSI 300 166 and European PTT specifications for transmit and receive return loss when series resistors are used.

Table 2. G.775 Requirements and LXT307 Implementation of LOS Detection

Condition	G.775 Recommendation	Intel Implementation
Detect LOS	Signal with no transitions[1] less than or equal to signal level of 35 dB below nominal for N consecutive intervals where 10 ≤N ≤255.	Signal level 20 dB below nominal and no consecutive transition for 160 to 190 (typical 175) pulse intervals.
Clear LOS	Signal has transitions[1] and level greater than or equal to 9 dB below nominal for N consecutive pulse intervals where 10 ≤N ≤255.	Signal level above 20 dB with ones density greater than 12.5% for 32-bit positions, and with fewer than 15 consecutive zeros.
1. A signal with “transitions” corresponds to a G.703 compliant signal.		

Table 3. Equalizer Control Inputs for Pulse Amplitude Selection

EC	Line Length & Cable Loss	Application
0	ITU Recommendation G.703	E1 - Coax (75 Ω)
1	ITU Recommendation G.703	E1 - Twisted-Pair (120 Ω)

2.6 Driver Performance Monitor

The transceiver incorporates an advanced Driver Performance Monitor (DPM). MTIP and MRING are the inputs to the DPM that are connected in parallel with TTIP and TRING at the output transformer. The DPM circuitry uses four comparators and a 150 ns pulse discriminator to filter glitches. The DPM output level goes High upon detection of 63 consecutive zeros, and is cleared when a transition is detected on the transmit line or when a reset command is received. The

DPM output also goes High to indicate a signal line short to ground on MTIP or MRING. A ground fault induced DPM flag is automatically cleared when the ground condition is corrected (chip reset is not required).

2.7 Operating Modes

The LXT307 transceiver can be controlled through hard-wired pins (Hardware Mode–default) or by a microprocessor through a serial interface (Host Mode). The mode of operation is set by the MODE pin logic level. The LXT307 can also be commanded to operate in one of several diagnostic modes.

2.7.1 Hardware Mode Operation

In Hardware mode transceiver operation is controlled by individual pins. With the exception of the $\overline{\text{INT}}$ and CLKE functions, Hardware mode provides all the functions available in Host mode. In Hardware mode, RPOS and RNEG outputs are valid on the rising edge of RCLK.

When the MODE pin is set Low, the LXT307 operates in Hardware Mode. In Hardware Mode the transceiver is controlled through individual pins; a microprocessor is not required. RPOS and RNEG are valid on the rising edge of RCLK.

The equalizer is controlled by pin 23 (EC). Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All 1s (TAOS) is provided through pins 26, 27, and 28.

2.7.2 Host Mode Control

The LXT307 operates in the Host mode when pin 5 (MODE) is High. In Host mode, a microprocessor controls the LXT307 through the serial I/O port (SIO). The SIO port provides access to a pair of transceiver data registers; one for command inputs and one for status outputs. An SIO transaction is initiated by a falling edge on the Chip Select pin. A High-to-Low transition on $\overline{\text{CS}}$ is required for each subsequent access to the Host mode registers.

The transceiver responds by writing the incoming serial word from the SDI pin into its command register. Figure 4 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the transceiver subsequently outputs the contents of its status register onto the SDO pin. Figure 5 shows an SIO read operation. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 4. Table 17 and Figure 16 and Figure 17 show SIO timing.

2.7.2.1 Serial Input Word

Figure 4 shows the Serial Input data structure. The LXT307 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/$\overline{\text{W}}$) control when the chip is accessed. The R/$\overline{\text{W}}$ bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second eight bits of a write operation, clear Loss of Signal (LOS) and Driver Performance Monitor (DPM) interrupts, reset the chip, and control diagnostic modes. The first 2 bits (D0 - D1) clear and/or mask LOS and DPM interrupts. The last three bits (D5 - D7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 5 for details on bits D5 - D7.

2.7.2.2 Serial Output Word

Figure 5 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a read command (R/$\overline{W}$ = 1), then SDO becomes active after the last Command/Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high-Z to a Low/High.

The first five bits (D0-D4) of the output data byte reports Loss of Signal (LOS) and Driver Performance Monitor (DPM) conditions and equalizer settings. The last three bits (D5 through D7) report operating modes (normal or diagnostic) and interrupt status as listed in Table 6.

If the $\overline{INT}$ line is High (no interrupt is pending), bits D5 through D7 report the status of the operating mode as listed in Table 6. If the $\overline{INT}$ line is Low, the interrupt status overrides all other reports and bits D5 - D7 reflect the interrupt status.

2.7.3 Interrupt Handling

The Host mode provides a latched Interrupt output pin, $\overline{INT}$. Any change in the LOS or DPM bits (D0 and D1 of the output data byte, respectively) triggers an interrupt. As shown in Figure 6, writing a one to the respective bit of the input data byte (D0 = LOS, D1 = DPM) masks either or both interrupt generators. When an interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of the $\overline{INT}$ pin consists of a pulldown device. Hence, an external pull-up resistor is required. Clear the interrupt as follows:

1. If one or both interrupt bits (LOS or DPM, D0 and D1 of the output data byte) = 1, writing a 1 to the input bit (D0 or D1, respectively), of the input data byte will clear the interrupt. Leaving a 1 in either of these bit positions will effectively mask the associated interrupt. To re-enable the interrupt capability, reset D0 and/or D1 to 0.
2. If neither LOS or DPM = 1, the interrupt will be cleared by resetting the chip. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

Table 4. CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS/RNEG SDO	RCLK SCLK	Rising Falling
HIGH	RPOS/RNEG SDO	RCLK SCLK	Falling Rising

Table 5. SIO Input Bit Settings (See Figure 4)

Mode	RLOOP Bit D5	LLOOP Bit D6	TAOS Bit D7
RLOOP	1	0	–
LLOOP	0	1	0
LLOOP + TAOS	0	1	1
TAOS	0	0	1
RESET	1	1	0

Table 6. Serial Data Output Bit Coding

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input. (*i.e.*, normal operation)
0	0	1	TAOS is active.
0	1	0	Local Loopback is active.
0	1	1	TAOS and Local Loopback are active.
1	0	0	Remote Loopback is active.
Bit D5	**Bit D6**	**Bit D7**	**Interrupt Status**
1	0	1	DPM has changed state since last clear DPM occurred.
1	1	0	LOS has changed state since last clear LOS occurred.
1	1	1	LOS and DPM have both changed state since last clear DPM and clear LOS occurred.

Figure 4. LXT307 SIO Write Operation

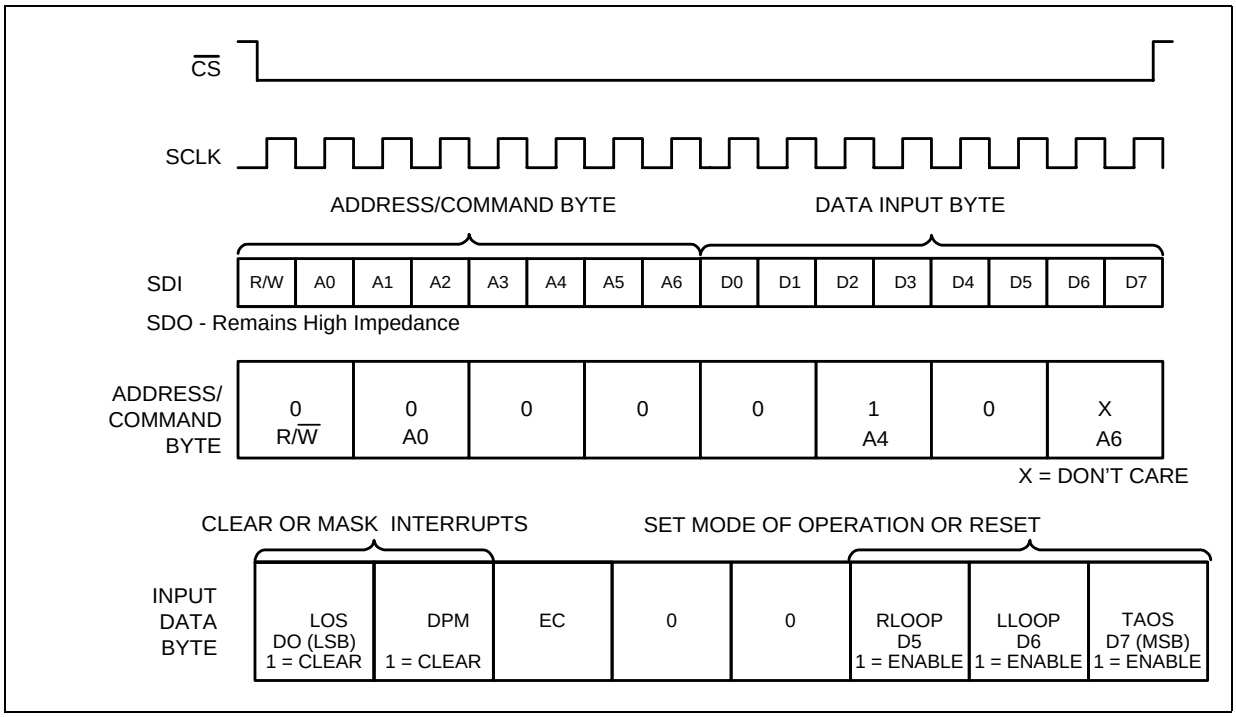


Figure 5. LXT307 SIO Read Operation

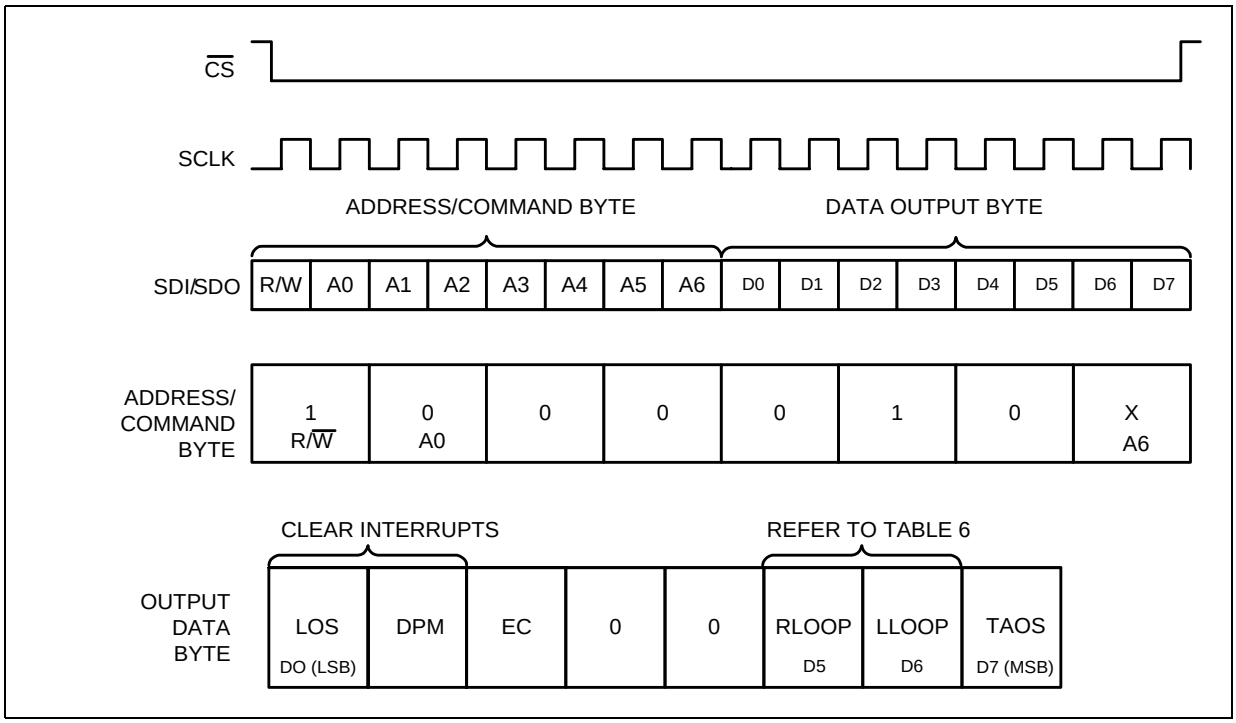
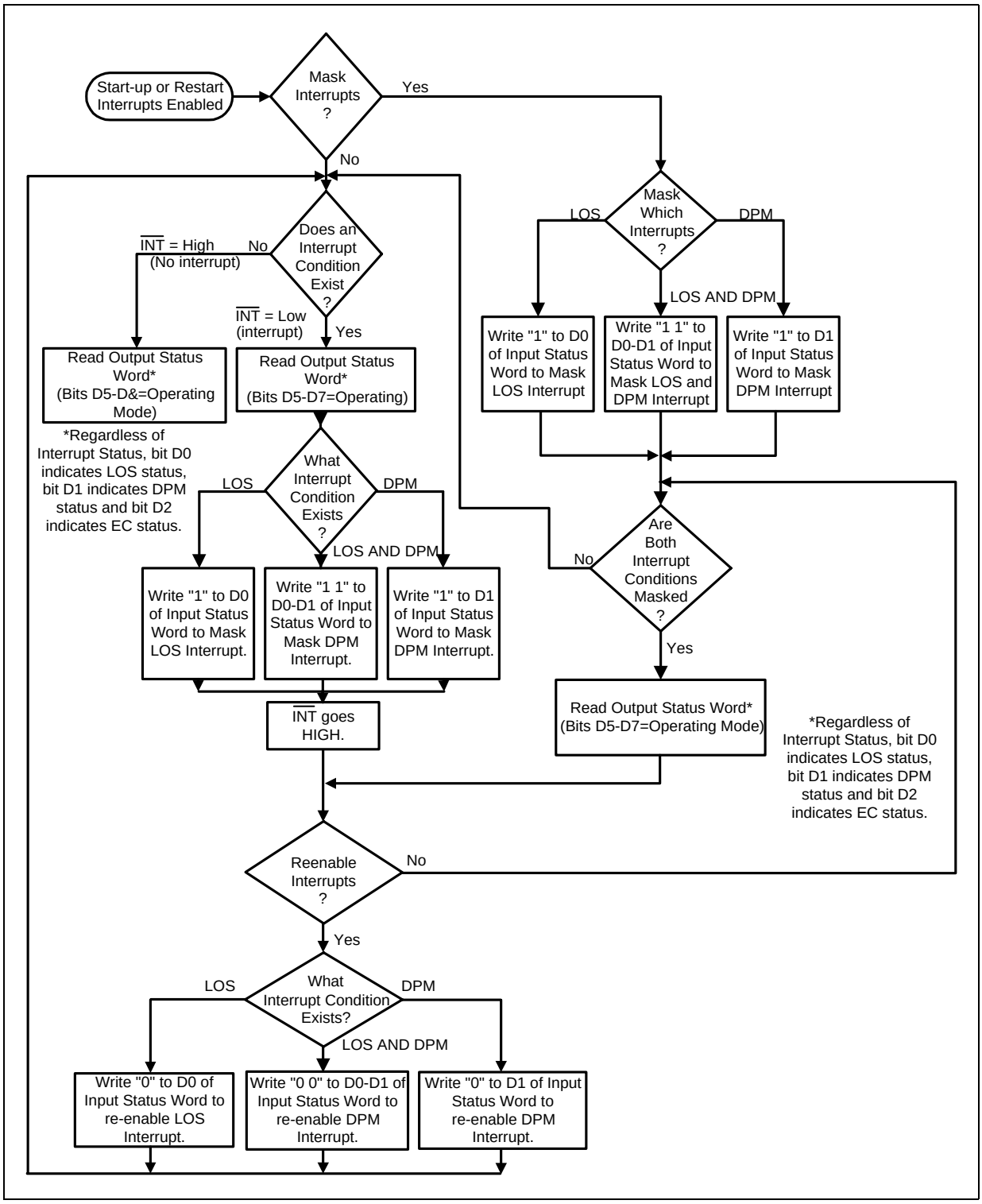


Figure 6. LXT307 Interrupt Handling



2.7.4 Diagnostic Mode Operation

2.7.4.1 Transmit All Ones

See Figure 7 and Figure 8. In Transmit All Ones (TAOS) mode, the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1s at the TCLK frequency when TAOS is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

Figure 7. TAOS

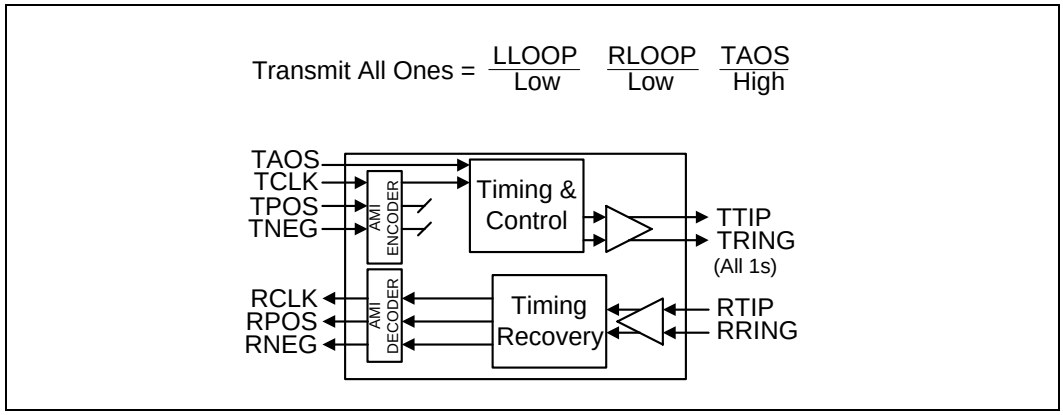
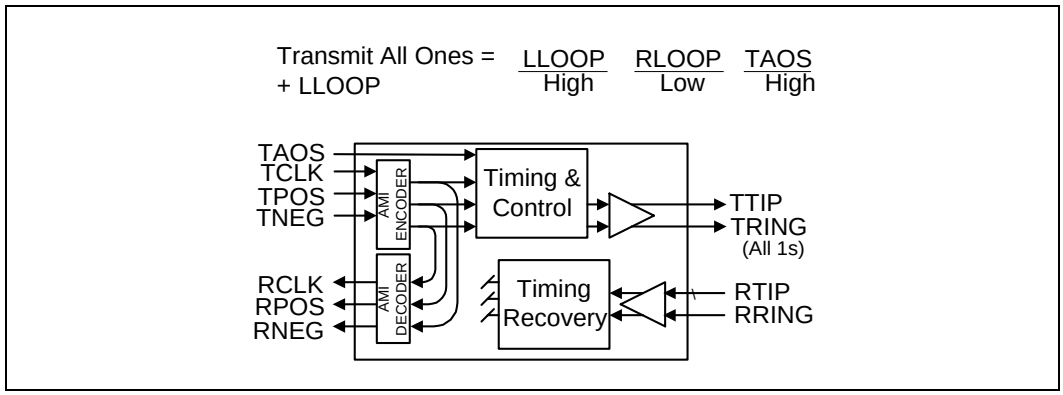


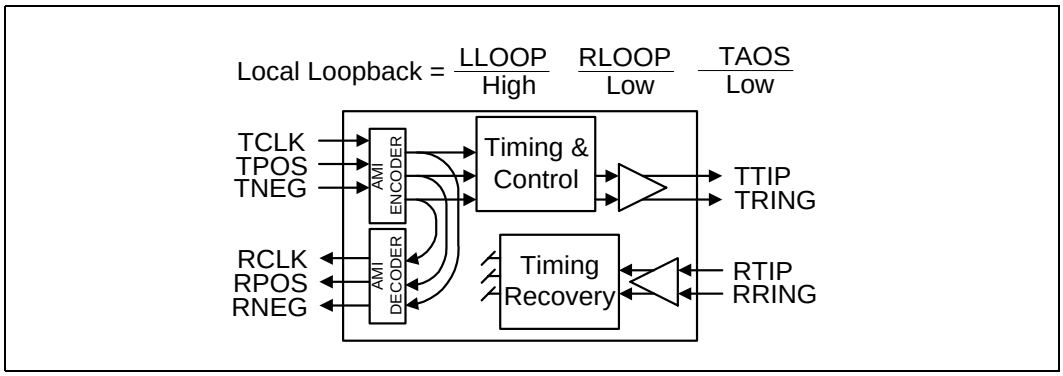
Figure 8. TAOS with LLOOP



2.7.4.2 Local Loopback

See Figure 9. In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK). The transmitter circuits are unaffected. The TPOS and TNEG inputs (or a stream of 1s if the TAOS command is active) will be transmitted normally.

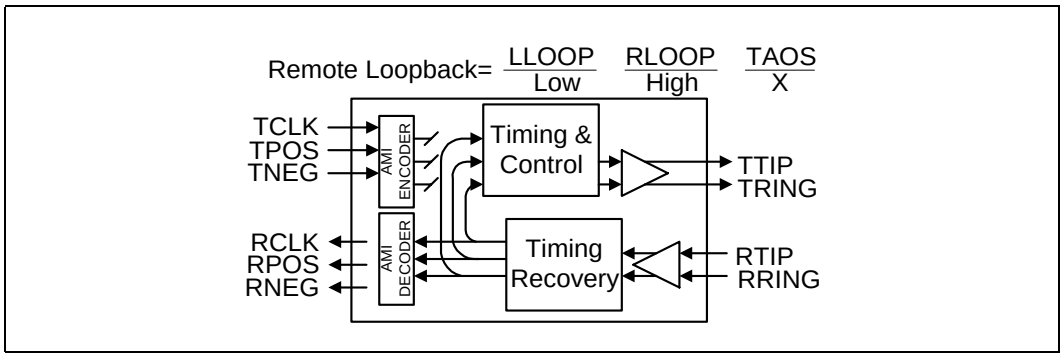
Figure 9. LLOOP



2.7.4.3 Remote Loopback

See Figure 10. In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

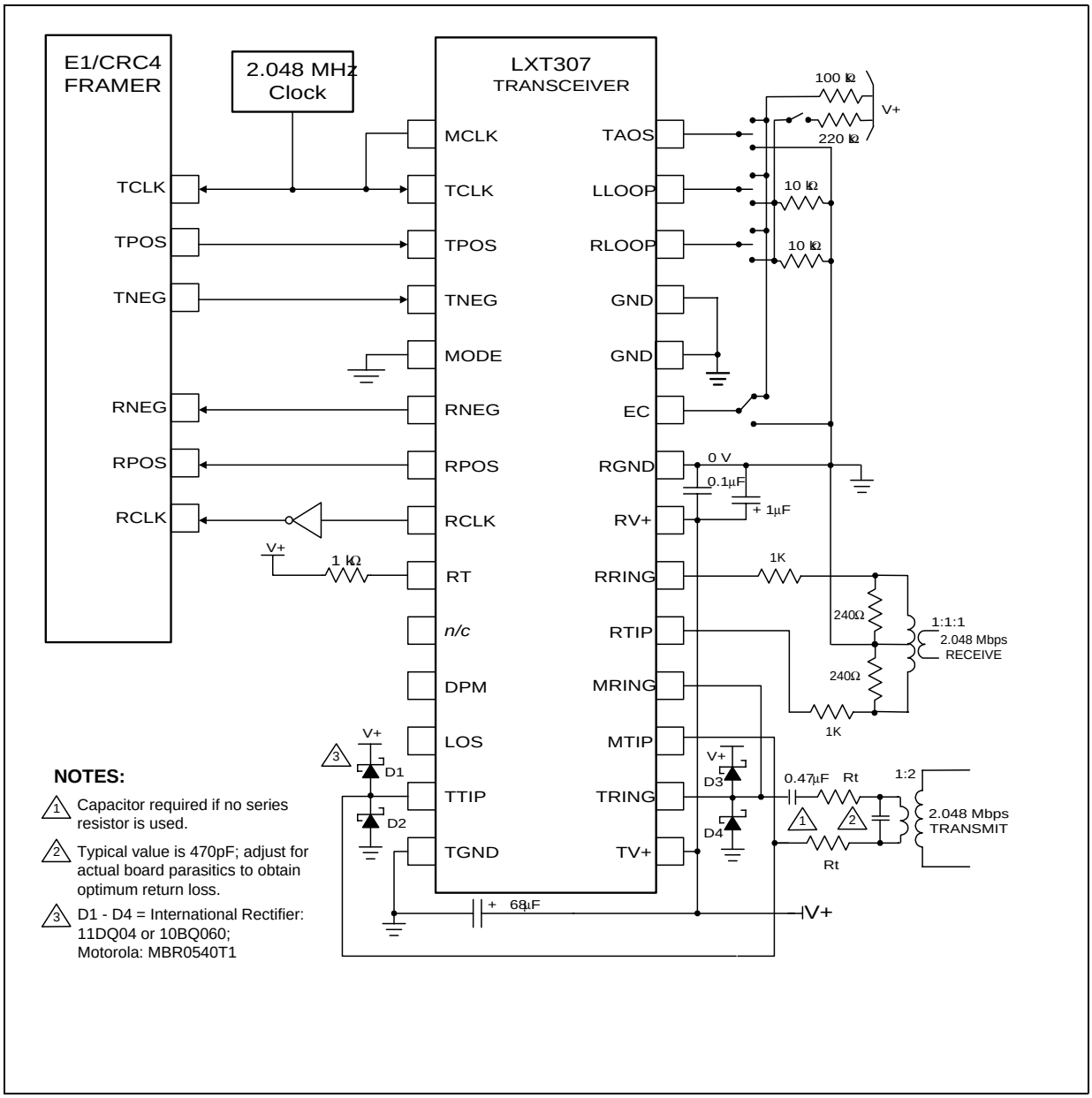
Figure 10. RLOOP



3.0 Application Information

Figure 11 is a 2.048 Mbps E1 120 Ω Twisted-Pair wire application using EC code 1 and 15 Ω Rt resistors in line with the transmit transformer to provide high return loss and surge protection. When high return loss is not a critical factor, a 1:1 transformer without in-line resistors provides maximum power savings. Table 9 and Table 10 list typical return loss figures for various transformer ratios, Rt values and the associated EC code for 75 Ω coax and 120 Ω twisted-pair applications, respectively. The LXT307 is shown in Hardware mode with a general G.704 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 11. LXT307 120 Ω Application (Hardware Mode)



3.1 E1 Coaxial Applications

Figure 12 shows the line interface for a typical E1 coaxial (75 Ω) application. The EC code should be set to 0 for coax. With 9.1 Ω Rt resistors in line with the 1:2 output transformer, the LXT307 produces 2.37 V peak pulses as required for coax applications. A 1:1:1 transformer is used on the receive side.

3.2 Line Protection

On the receive side, the 1 kΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (40 kΩ typical) the resistors do not affect the receiver sensitivity. On the transmit side, the Schottky diodes D1-D4 protect the output driver. While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

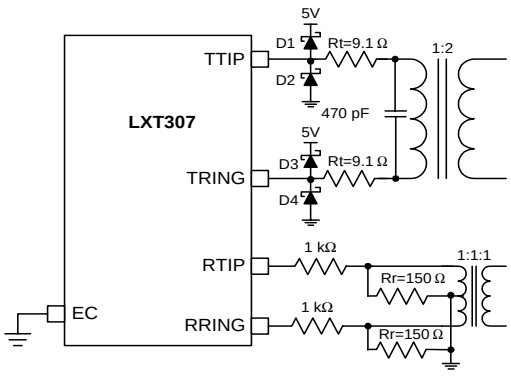
Table 7. Transformer Specifications

Parameter	Value
Turns ratio Tx	1:2 (±2%)
Primary inductance	1.2 mH min
Leakage inductance	0.5 µH max
Interwinding capacitance	25 pF max
Series resistance	1.0 Ω PRI

Table 8. Transformer Selection Guide

Transformer Manufacturer	Part Number	Turns Ratio	Description
Pulse Engineering	PE65861	1:2	Dual SMD
	PE 65351	1:2	Single through hole
Bel Fuse	0553-5006	1:2	Dual
Schott	67127370	1:2	Single through hole
Midcom	671-5832	1:2	Single through hole

Figure 12. Line Interface for E1 Coax Applications



D1 - D4 = International Rectifier: 11DQ04 or 10BQ060;
Motorola: MBR0540T1

Table 9. 75 Ω Output Combinations

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
1	1: 1	Rt = 10 Ω	5 dB
1	1: 2	Rt = 14.3 Ω	10 dB
0	1: 1	Rt = 0 Ω[4]	0.5 dB
0	1: 2	Rt = 9.1 Ω	18 dB

1. Transformer turns ratio accuracy is ±2%.
2. Rt values are ±1%.
3. Typical return loss, 51 kHz - 3.0728 kHz.
4. A capacitor is required if no series resistor is used.

Table 10. 120 Ω Output Combinations

EC	Xfmr Ratio[1]	Rt Value[2]	Rtn Loss[3]
1	1: 1	Rt = 0 Ω[4]	0.5 dB
1	1: 2	Rt = 15 Ω	18 dB
0	1: 2	Rt = 9.1 Ω	10 dB

1. Transformer turns ratio accuracy is ±2%.
2. Rt values are ±1%.
3. Typical return loss, 51 kHz - 3.0728 kHz.
4. A capacitor is required if no series resistor is used.

4.0 Test Specifications

Note: The minimum and maximum values in Table 11 through Table 17 and Figure 13 through Figure 18 represent the performance specifications of the LXT307 and are guaranteed by test, except where noted by design.

Table 11. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin[1]	VIN	RGND - 0.3	RV+ + 0.3	V
Input current, any pin[2]	Iin	-10	10	mA
Storage temperature	TSTG	-65	150	°C

Caution: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

1. Excluding RTIP and RRING which must stay between -6V and (RV+ + 0.3) V.
2. Transient currents of up to 100 mA will not cause SCR latch up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Table 12. Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Unit
DC supply[1]	RV+, TV+	4.75	5.0	5.25	V
Ambient operating temperature	TA	-40	25	85	°C

1. TV+ must not exceed RV+ by more than 0.3 V.

Table 13. Electrical Characteristics (Over Recommended Operating Conditions)

Parameter		Sym	Min	Typ	Max	Unit	Test Conditions
Total power dissipation[1, 2]	75 Ω (EC = 0)	PD	–	260	320	mW	50% 1s density
	120 Ω (EC = 1)	PD	–	270	320	mW	
Total power consumption[3]	120 Ω (EC = 1)	PD	–	400	T.B.D	mW	100% 1s density
High level input voltage[4] (pins 1-5, 23)		VIH	2.0	–	–	V	
Low level input voltage[4] (pins 1-5, 23)		Vil	–	–	0.8	V	
High level output voltage[4, 5] (pins 6-8, 11, 12, 23, 25)		VOH	2.4	–	–	V	IOUT = -400 µA
Low level output voltage[4, 5] (pins 6-8, 11, 12, 23, 25)		VOL	–	–	0.4	V	IOUT = 1.6 mA
Input leakage current[6]		ILL	0	–	±10	µA	
Three-state leakage current (pin 25)		I3L	0	–	±10	µA	

1. Device power dissipation while driving a 75 or 120 Ω load over operating temperature range. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load. Rt = 0 Ω; transformer ratio = 1:1.
2. Guaranteed by design and other correlation methods.
3. Power consumption while driving a 60 Ω effective load. Includes device and load. Rt = 15 Ω; transformer ratio = 1:2; EC = 1.
4. Functionality of pin 23 depends on mode. See Host/Hardware Mode Descriptions.
5. Output drivers will output CMOS logic levels into CMOS loads.
6. Except MTIP and MRING ILL = ±50 µA.

Table 14. Analog Characteristics (Over Recommended Operating Conditions)

Parameter		Min	Typical[1]	Max	Unit	Test Conditions
AMI output pulse Amplitudes	75 Ω	2.14	2.37	2.6	V	G.703
	120 Ω	2.7	3.0	3.3	V	G.703
Peak voltage of a space	75 Ω	-0.237	0	+0.237	V	
	120 Ω	-0.3	0	+0.3	V	
Ratio of the widths of positive and negative pulses at the nominal half amplitude		95	–	105	%	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval		95	–	105	%	
Recommended output load at TTIP and TRING		–	75	–	Ω	
Driver output impedance[4]			3	10	Ω	
Driver short circuit current[2]				50	mA	
Jitter added by the transmitter	10 Hz - 8 kHz[4]	–	–	0.02	UI	G.823
	18 kHz - 100 kHz[4]	–	–	0.025	UI	G.823
	20 Hz - 100 kHz[4]	–	–	0.025	UI	G.823
	Broad Band[3]	–	0.025	0.050	UI	
Receiver sensitivity	(0 dB = 2.4 V)	13.6	–	–	dB	
		500	–	–	mV	
Receiver input impedance		–	40	–	kΩ	
Signal to interference ratio (FEXT)[4]		15	–	–	dB	G.703, O.151
Input jitter tolerance 18 kHz - 100 kHz		0.4	–	–	UI	G.823
Loss of Signal threshold		–	20	–	dB	below nominal
Data decision threshold[4]		43	50	57	% peak	
Allowable consecutive zeros before LOS[4]		160	175	190	–	G.775
LOS reset transition window[4]		–	32	–	bit	four transitions
		Transmit		Receive		
		Min	Typ[1]	Min	Typ[1]	
Minimum Return Loss[4]	51 Hz – 102 kHz	18	20	20	–	dB	Dynamic conditions per ETS 300 166 and ITU G.703. See Figure 11 & Figure 12.
	102 kHz –2.048 MHz	18	20	20	–	dB	
	2.048 MHz – 3.072 MHz	18	20	20	–	dB	

1. Typical values are measured at 25° C and are for design aid only. Not guaranteed or subject to production testing.
2. Per OFTEL OTR-001/BABT BS4650 with 15 Ω termination resistors and a 1:2 transmit transformer on a 0.5 Ω test load.
3. Input signal to TCLK is jitter-free.
4. Guaranteed by design or other correlation methods.

Figure 13. 2.048 Mbps Pulse Mask Template

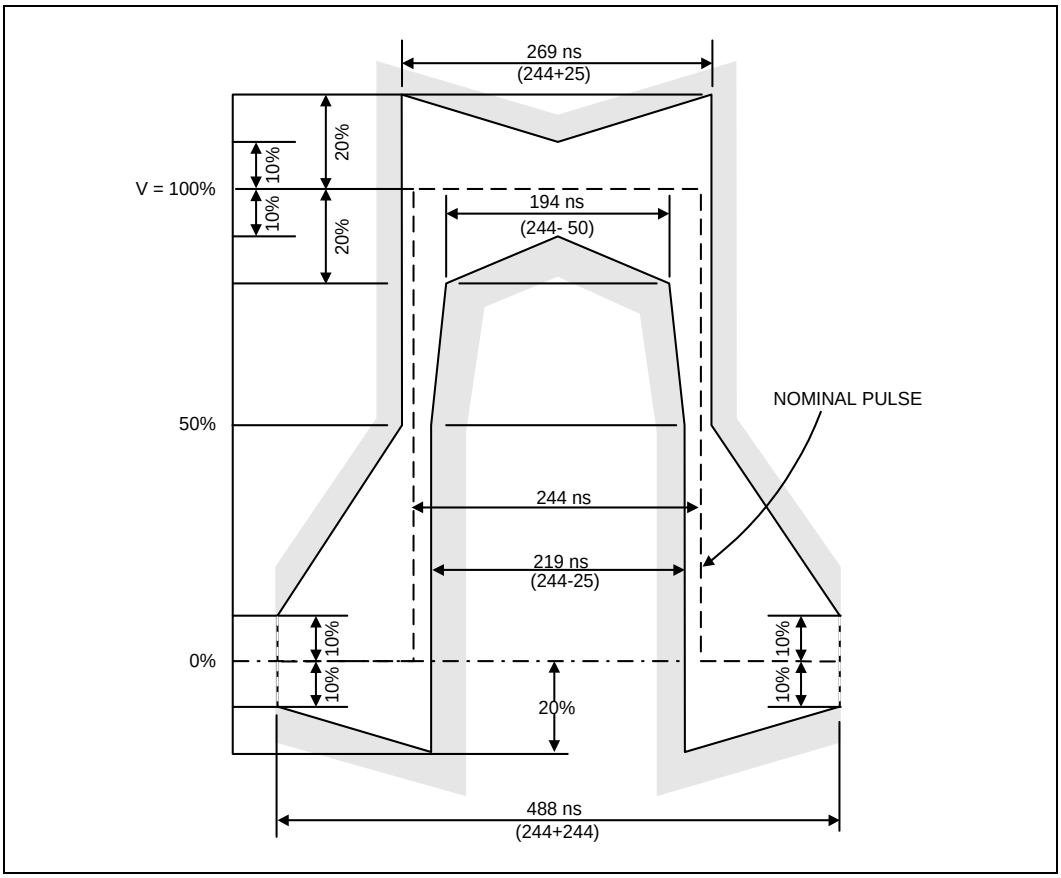


Table 15. Receive Timing Characteristics (Over Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Receive clock duty cycle	RCLKd	40	–	60	%	
Receive clock pulse width	t_{PW}	–	244	–	ns	
RPOS/RNEG to RCLK rising setup time	t_{SUR}	–	194	–	ns	
RCLK rising to RPOS/RNEG hold time	t_{HR}	–	194	–	ns	
1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.						

Figure 14. LXT307 Receive Clock Timing

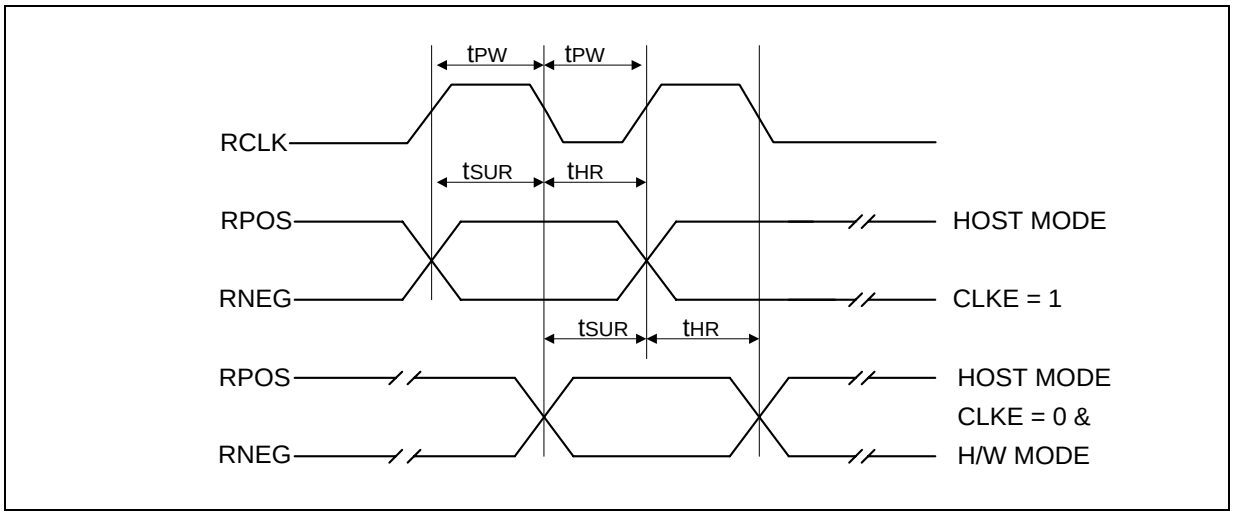


Figure 15. LXT307 Transmit Clock Timing

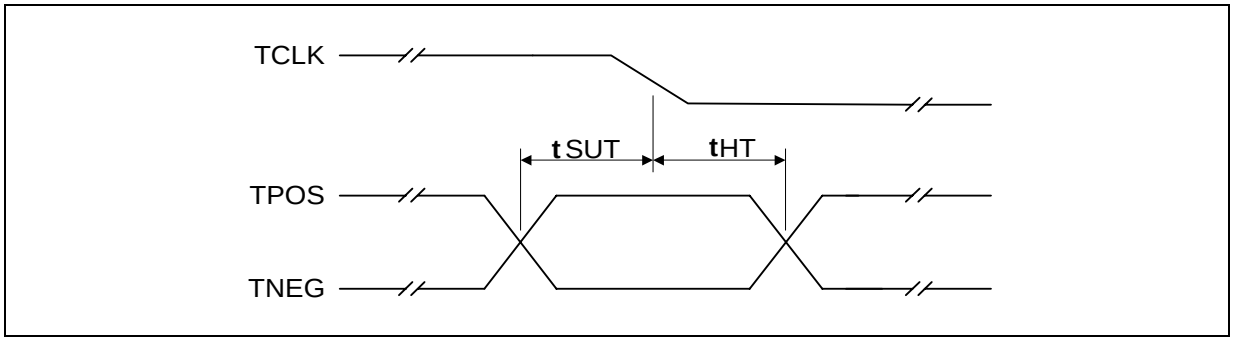


Table 16. Transmit Timing Characteristics (Over Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Unit
Master clock frequency	MCLK	–	2.048	–	MHz
Master clock tolerance	MCLKt	–	±100	–	ppm
Master clock duty cycle	MCLKd	40	–	60	%
Transmit clock frequency	TCLK	–	2.048	–	MHz
Transmit clock tolerance	TCLKt	–	±50	–	ppm
Transmit clock duty cycle	TCLKd	10	–	90	%
TPOS/TNEG to TCLK setup time	tSUT	25	–	–	ns
TCLK to TPOS/TNEG Hold time	tHT	25	–	–	ns

1. Typical values are at 25 °C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 17. Serial I/O Timing Characteristics (Over Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Rise time - any digital output	t_R	–	–	100	ns	Load 1.6 mA, 50 pF
Fall time - any digital output	t_F	–	–	100	ns	Load -400 µA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–		50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	–	–	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	–	100	–	ns	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 16. LXT307 Serial Data Input Timing Diagram

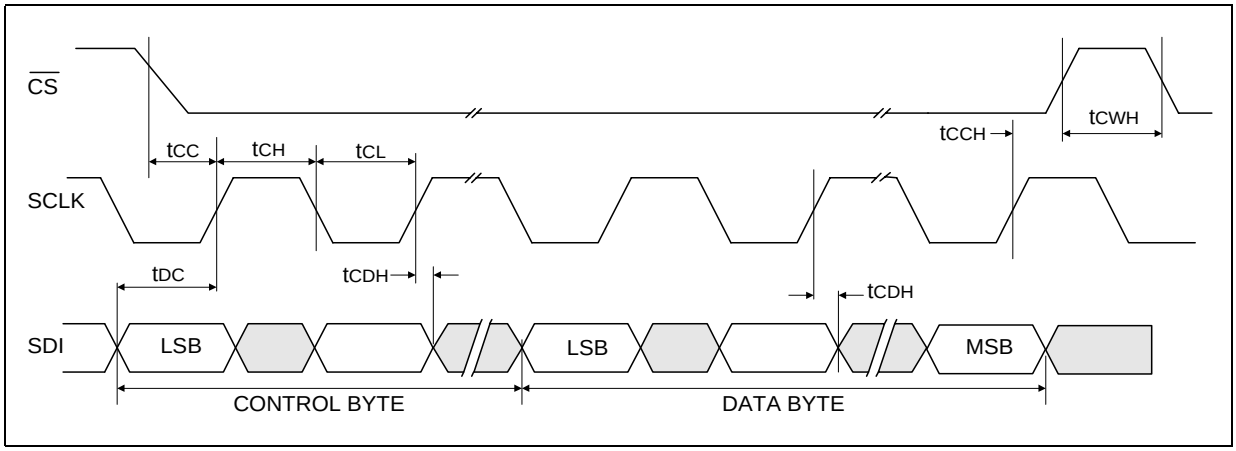


Figure 17. LXT307 Serial Data Output Timing Diagram

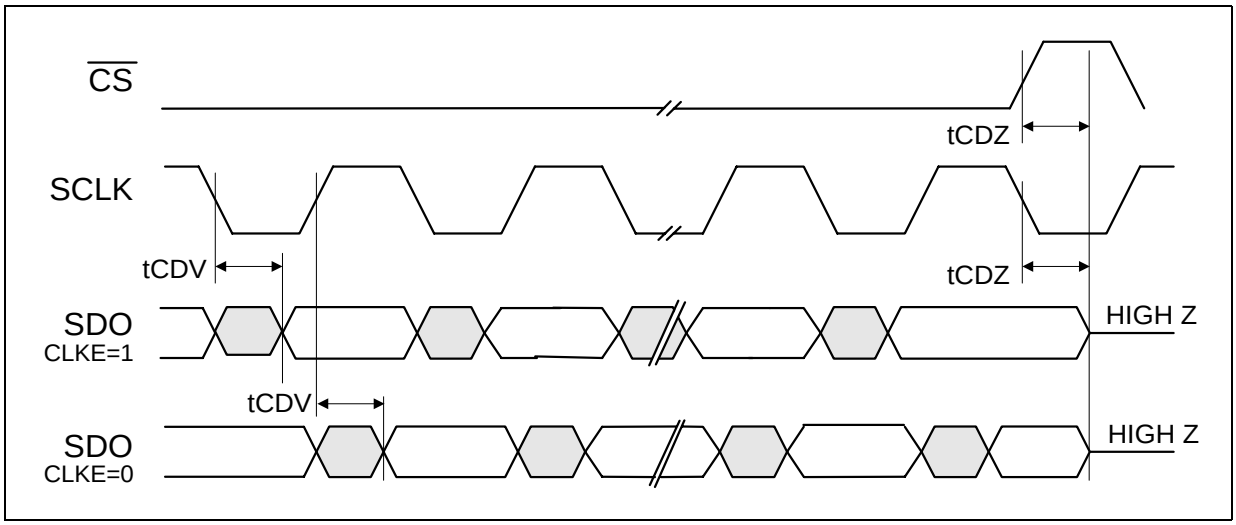
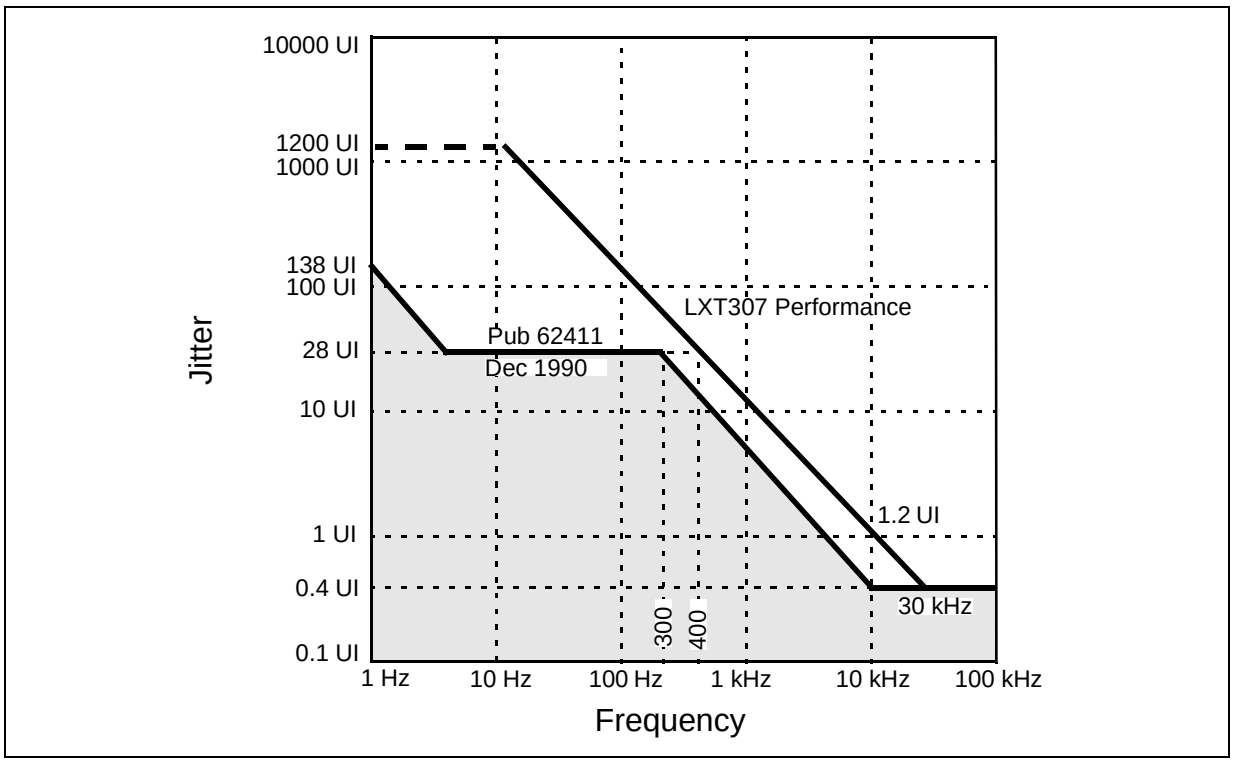


Figure 18. Typical Receiver Input Jitter Tolerance (Loop Mode)

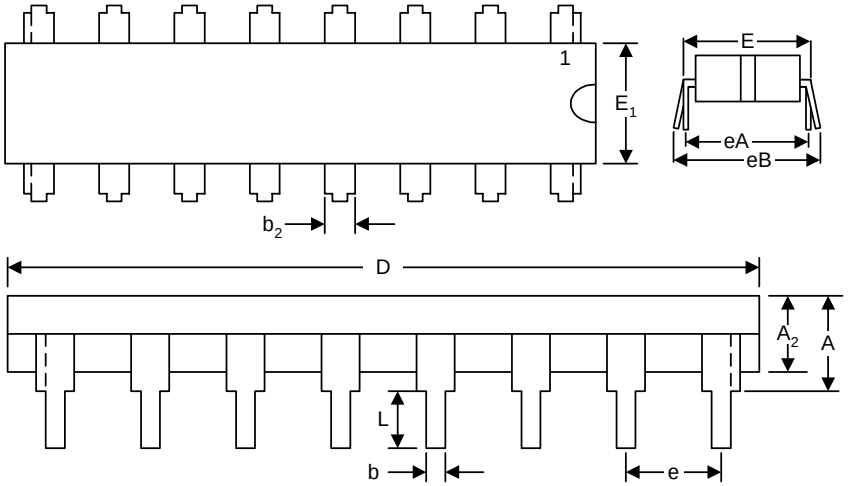


5.0 Mechanical Specifications

Figure 19. Plastic DIP Specifications

28-pin Dual In-Line Package

- P/N LXT307NE
- Temperature range -45 °C to +85 °C



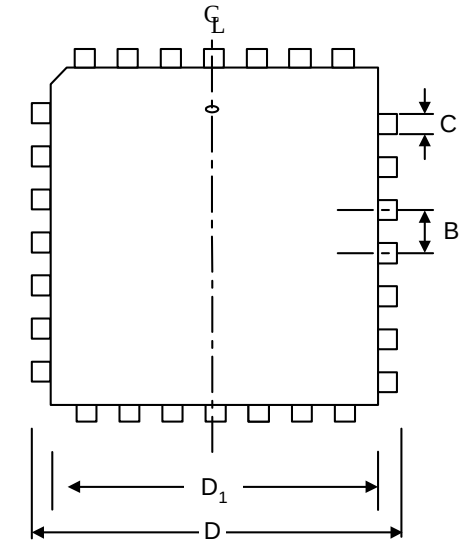
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.250	–	6.350
A2	0.125	0.195	3.175	4.953
b	0.014	0.022	0.356	0.559
b2	0.030	0.070	0.762	1.778
D	1.380	1.565	35.052	39.751
E	0.600	0.625	15.240	15.875
E1	0.485	0.580	12.319	14.732
e	0.100 BSC[1] (nominal)		2.540 BSC[1] (nominal)	
eA	0.600 BSC[1] (nominal)		15.240 BSC[1] (nominal)	
eB	–	0.700	–	17.780
L	0.115	0.200	2.921	5.080

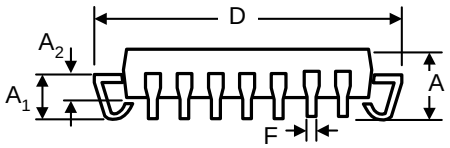
1. BSC—Basic Spacing between Centers

Figure 20. PLCC Package Specifications

28-Pin Plastic Leaded Chip Carrier

- P/N LXT307PE
- Temperature range -45 °C to +85 °C





Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers