LXT318

E1 NTU/ISDN PRI Transceiver

Datasheet

The LXT318 is the first fully integrated transceiver for E1 Network Termination Unit (NTU) and ISDN Primary Rate Interface (ISDN PRI) applications at 2.048 Mbps. The transceiver operates from 0.0 km to 2.6 km of 0.6 mm (22 AWG) twisted-pair cable with no external components.

The LXT318 offers selectable HDB3 encoding/decoding, and unipolar or bipolar data I/O. The LXT318 also provides jitter attenuation in either the transmit or receive direction starting at 3 Hz, and incorporates a serial interface (SIO) for microprocessor control.

The LXT318 offers a variety of diagnostic features including loopbacks and loss of signal monitoring. It is built using an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

Applications

- PCM 30/ISDN PRI Interface (ITU G.703, I.431)
- NTU (interface to E1 Service)
- E1 Mux or LAN bridge - Campus Networking
- Wireless Base Stations/Networking
- CPU to CPU Channel Extenders
- Digital Loop Carrier — Subscriber Carrier Systems
- Channel Banks
- HDSL - E1 Extension

Product Features

- Fully integrated transceiver comprising: on-chip equalizer; timing recovery/control; data processor; receiver; transmitter and digital control
- Pin compatible with the LXT310 T1 CSU/ ISDN PRI (1.544 Mbps) transceiver
- Meets or exceeds latest ITU specifications including G.703, G.736, G.823, and I.431
- Meets ETSI 300011 and 300233 standards
- Jitter attenuation starting at 3 Hz, switchable to transmit or receive path
- Exceeds ETSI TBR12/13 jitter transfer performance specifications
- Fully restores the received signal after transmission via a cable with attenuation of 43 dB @ 1024 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable HDB3 encoding/decoding
- Output short circuit current limit protection
- Meets 50 mA RMS short-circuit current limit (per OFTEL OTR-001)
- On-line idle mode for testing or for redundant systems
- Local and remote loopback functions
- Receive monitor with Loss of Signal (LOS) output
- Microprocessor controllable
- Available in 28-pin DIP and PLCC
- Extended Temperature Range (-40° C to +85° C)

As of January 15, 2001, this document replaces the Level One document *LXT318 — E1 NTU/ISDN PRI Transceiver*.

Order Number: 249073-001
January 2001

Datasheet

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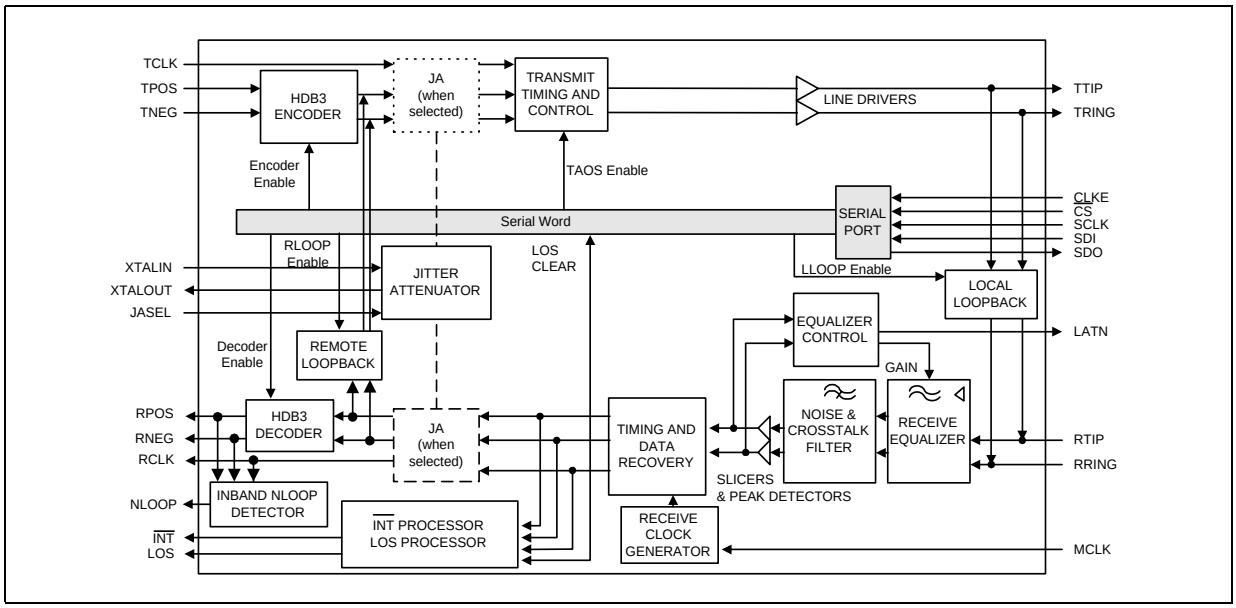
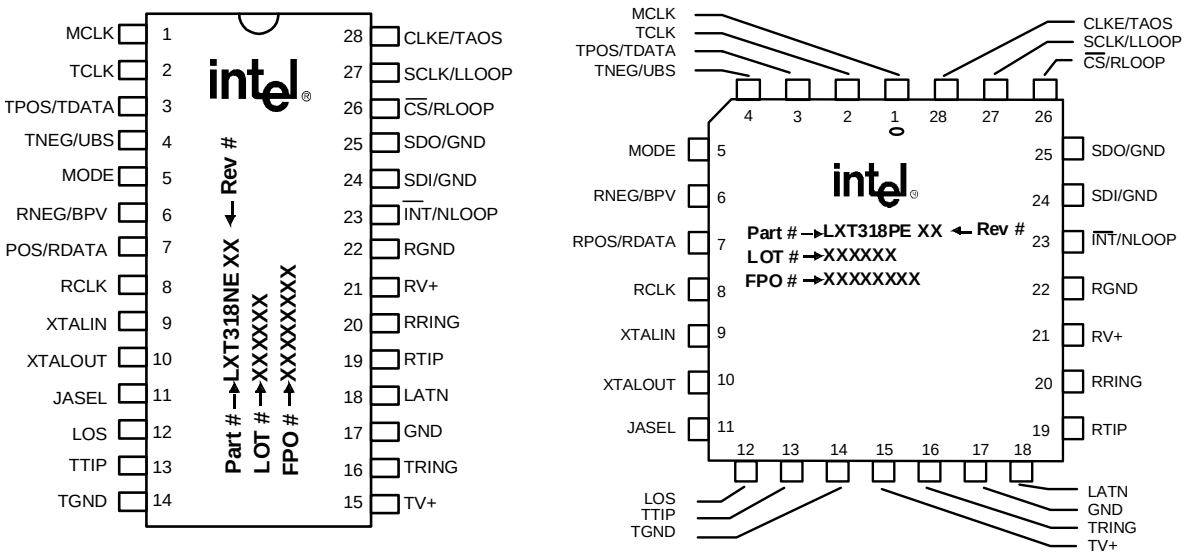


1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT318 Pin Assignments and Package Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. Pin Descriptions

Pin #	Symbol	I/O	Description
1	MCLK	I	**Master Clock.** 2.048 MHz clock used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
2	TCLK	I	**Transmit Clock.** TPOS and TNEG are sampled on the falling edge of TCLK. Ground this pin if TCLK is not supplied.
3 4	TPOS/ TDATA TNEG/UBS	I I	**Transmit Data Input/Polarity Select.** Input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. When pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT318 switches to a unipolar I/O mode and transmit data is input on pin 3. Unipolar mode pin functions are listed in Table 2.
5	MODE	I	**Mode Select.** Setting MODE High selects Host mode. In Host mode, the serial interface is used to control the LXT318 and determine its status. Setting MODE Low puts the LXT318 in the Hardware (H/W) mode. In Hardware mode, the serial interface is disabled and hard-wired pins are used to control configuration and report status. Tying MODE to RCLK activates the Hardware mode and enables the HDB3 encoder/decoder.
6	RNEG/BPV	O	**Receive Negative Data; Receive Positive Data.** In Bipolar I/O mode, a signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In Hardware mode both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 is a Bipolar Violation output, and pin 7 is the Unipolar data output. See Table 2 for Unipolar mode functions.
7	RPOS/ RDATA	O	
8	RCLK	O	**Receive Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	XTALIN	I	**Crystal Input; Crystal Output.** An external crystal (18.7 pF load capacitance, pullable) operating at four times the bit rate (8.192 MHz) is required to enable the jitter attenuation function of the LXT318. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and leaving the XTALOUT pin unconnected or tied to ground.
10	XTALOUT	O	
11	JASEL	I	**Jitter Attenuation Select.** Selects jitter attenuation location. When JASEL is High, the jitter attenuator is active in the receive path. When JASEL is Low, the jitter attenuator is active in the transmit path.
12	LOS	O	**Loss Of Signal.** LOS goes High after 175 consecutive spaces and returns Low when the received signal reaches 12.5% mark density (minimum of four marks within 32 bit periods, with no more than 15 consecutive 0s). Received marks are output on RPOS and RNEG even when LOS is High.
13 16	TTIP TRING	O	**Transmit Tip.** Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
14	TGND	–	**TV+ Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	I	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
17	GND	I	**Ground.** This pin must be tied to ground.
18	LATN	O	**Line Attenuation Indication.** Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 1024 kHz) in 9.5 dB steps. When LATN is High for one RCLK pulse, the equalizer is set at 9.5 dB gain; 2 pulses = 19 dB; 3 pulses = 28.5 dB and 4 pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	**Receive Tip; Receive Ring.** The HDB3 signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	
21	RV+	I	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	–	**RV+ Ground.** Ground return for power supply RV+.

Table 1. Pin Descriptions (Continued)

Pin #	Symbol	I/O	Description
23	INT	O	**Interrupt *(Host Mode)*.** In Host mode, this pin goes Low to flag the host processor when LOS changes state. $\overline{\text{INT}}$ is an open drain output and should be tied to power supply RV+ through a resistor. Reset $\overline{\text{INT}}$ by clearing the LOS register bit.
	NLOOP	O	**Network Loopback Detection *(H/W Mode)*.** In Hardware mode, this pin indicates that inband network loopback is active by going High. To set this signal High, the device must receive the NLOOP activation pattern (00001) for five seconds. To reset it Low, either the device must receive the deactivation pattern (001) for five seconds or either RLOOP or LLOOP must be activated.
24	SDI	I	**Serial Data In *(Host Mode)*.** The serial data input stream is applied to this pin when the LXT318 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
	GND	I	**Ground *(H/W Mode)*.** This pin is inactive in the Hardware mode and must be tied to ground.
25	SDO	O	**Serial Data Out *(Host Mode)*.** In Host mode, serial data from the on-chip register is output on this pin. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. SDO goes to the high-impedance state when the serial port is being written to.
	GND	I	**Ground *(H/W Mode)*.** This pin is inactive in Hardware mode and should be tied to ground.
26	$\overline{\text{CS}}$	I	**Chip Select *(Host Mode)*.** In Host mode, this pin selects the serial interface. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
	RLOOP	I	**Remote Loopback *(H/W Mode)*.** In Hardware mode, this pin controls the Remote Loopback function. Setting RLOOP High enables Remote Loopback. During Remote Loopback, inline encoders and decoders are bypassed. Setting both RLOOP and LLOOP while holding TAOS Low causes a Reset.
27	SCLK	I	**Serial Clock *(Host Mode)*.** In Host mode, this clock is used to write data to, or read data from the serial interface register.
	LLOOP	I	**Local Loopback *(H/W Mode)*.** In Hardware mode, setting this pin High selects the Local Loopback function. Setting both RLOOP and LLOOP while holding TAOS Low causes a Reset.
28	CLKE	I	**Clock Edge *(Host Mode)*.** In Host mode, this pin controls selects when the data outputs are valid. Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is Low, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
	TAOS	I	**Transmit All Ones *(H/W Mode)*.** In Hardware mode, setting this pin High selects the TAOS function causing the LXT318 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

Table 2. Unipolar Data I/O Pin Descriptions[1]

Pin #	Symbol	I/O	Description
3	TDATA	I	**Transmit Data.** Unipolar input for data to be transmitted on the twisted-pair line.
4	UBS	I	**Unipolar/Bipolar Select.** When pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT318 switches to Unipolar data I/O. The device immediately returns to bipolar data I/O when pin 4 goes Low.
6	BPV	O	**Bipolar Violation.** Pin 6 goes High to indicate a bipolar violation was detected.
7	RDATA	O	**Receive Data.** RDATA is a Non Return-to-Zero (NRZ) Unipolar data output. In Host mode, CLKE determines the clock edge when RDATA is stable and valid. In Hardware mode RDATA is stable and valid on the rising edge of RCLK.

1. Table 2 lists only those pins which are affected by the switch to unipolar data I/O.

2.0 Functional Description

The LXT318 is a fully integrated PCM transceiver for 2.048 Mbps (E1) applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

The LXT318 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

The transceiver may be controlled by a microprocessor via the serial port (Host Mode), or by individual pin settings (Hardware Mode). The jitter attenuator may be positioned in either the transmit or receive path, as determined by JASEL.

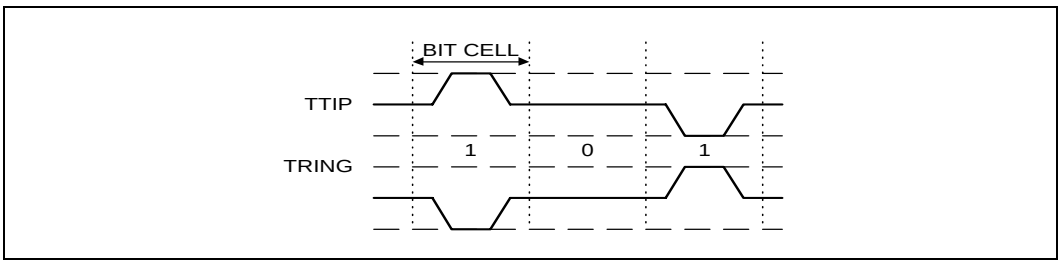
2.1 Transmitter

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the LXT318. Bipolar data is input at TPOS and TNEG. Unipolar data is input at TDATA only (Unipolar mode is enabled by holding TNEG High for 16 RCLK cycles). Input data may be passed through the Jitter Attenuator and/or HDB3 encoder, if selected. In Host mode, HDB3 is selected by setting bit D2 of the input data byte. In Hardware mode, HDB3 is selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Timing requirements for TCLK and the Master Clock (MCLK) are defined in the Test Specifications section. When TCLK is not supplied, the TCLK pin must be grounded.

2.1.1 Line Code

The LXT318 transmits data as a 50% HDB3 line code as shown in Figure 3. Biasing of the transmit DC level is on-chip. Shaped pulses meeting the various ITU requirements are applied to the HDB3 line driver for transmission onto the line at TTIP and TRING. Refer to Figure 23 and Table 15 for 2.048 Mbps pulse mask specifications.

Figure 3. 50% Duty Cycle Coding Diagram



2.1.2 Idle Mode

The LXT318 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications or for testing purposes. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). The high impedance state can be temporarily disabled by enabling Remote Loopback.

2.1.3 Short Circuit Limit

The LXT318 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 100 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

The LXT318 will meet or exceed the OFTEL OTR-001 short circuit limit (50 mARMS) when the design includes a 1:2 transmit transformer and 15 Ω resistors on TTIP and TRING. The device also meets or exceeds ITU specifications for NTU applications, as well as requirements for ISDN PRI.

2.2 Receiver

The receiver input from the twisted-pair is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to the Test Specifications section.

The signal received at RTIP and RRING is processed through the receive equalizer which may apply up to 43 dB of gain. Insertion loss of the line, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 4.

The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. The threshold is set to 50% of the peak value. The receiver is capable of accurately recovering signals with up to 43 dB of cable attenuation (from 2.7 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the HDB3 decoder (if selected) and to the LOS processor. The data and timing recovery sections provide an input jitter tolerance significantly better than required by ITU G.823, as shown in the Test Specifications section.

The LOS Processor loads a digital counter at the RCLK frequency. The count is incremented each time a 0 (space) is received, and reset to 0 each time a one (mark) is received. Upon receipt of 175 consecutive 0s the LOS pin goes High, and a smooth transition replaces the RCLK output with the MCLK. (During LOS, if MCLK is not supplied and JASEL is High, the RCLK output is replaced with the centered quartz crystal frequency.)

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the ones density reaches 12.5%. This level is based on receipt of at least four 1s in any 32 bit periods, with no more than 15 consecutive 0s.

2.2.1 Jitter Attenuation

Jitter attenuation is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). The Test Specifications show the LXT318 jitter attenuation performance compared with the jitter template specified by ITU G.736. The 3 dB corner frequency for the LXT318 is at 3 Hz. The performance complies with ETSI TBR-12 and TBR-13. An external crystal oscillating at four times the bit rate provides clock stabilization. The ES is a 32 x 2-bit register. When JASEL is High, the JAL is positioned in the receive path. When JASEL Low, the JAL is positioned in the transmit path.

Data (TPOS/TNEG or TDATA; or RPOS/RNEG or RDATA) is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits in the associated path.

2.3 Control Modes

The LXT318 transceiver can be controlled by a microprocessor through a serial interface (Host mode), or through individual hard-wired pins (Hardware mode). The mode of operation is determined by the input to MODE. With MODE set High, the LXT318 operates in the Host mode. With MODE set Low, the LXT318 operates in the Hardware mode. With MODE tied to RCLK, the LXT318 operates in the Hardware mode with the HDB3 encoder/decoder enabled. The LXT318 can also be commanded to operate in one of several diagnostic modes.

2.4 Host Mode Control

The LXT318 operates in the Host mode when MODE is set High. In Host mode the LXT318 is controlled through the serial I/O port (SIO) by a microprocessor. The LXT318 provides a pair of data registers, one for command inputs and one for status outputs, and an interrupt output.

An SIO transaction is initiated by a High-to-Low transition on $\overline{CS}$. The LXT318 responds by writing the incoming serial word from the SDI pin into its command register. If the command word contains a read request, the LXT318 subsequently outputs the contents of its status register onto the SDO pin. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as in Table 3.

The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte as shown in Figure 5 and Figure 6. SIO timing characteristics are shown in Table 14.

Table 3. CLKE Settings

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

Table 4. SIO Input Bits (See Figure 5)

Mode	RLOOP bit D5	LLOOP bit D6	TAOS bit D7
RLOOP	1	0	N/A

Table 4. SIO Input Bits (See Figure 5)

LLOOP	0	1	N/A
TAOS	0	N/A	1
RESET	1	1	0

2.4.1 Serial Input Word

Figure 5 shows the Serial Input data structure. The LXT318 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/$\overline{W}$) control when $\overline{CS}$ is Low. The R/$\overline{W}$ bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The Data Input byte is the second eight bits of a write operation. The first bit (D0) clears and/or masks LOS interrupts. The second bit (D1) clears and/or masks NLOOP detection interrupts. The third bit (D2) enables or disables HDB3 coding/decoding, and the last 3 bits (D5 - D7) control operating modes (normal and diagnostic) and chip reset. Refer to Table 4 for details on bits D5 - D7.

2.4.2 Serial Output Word

Figure 6 shows the Serial Output data structure. When the Serial Input word has bit A0 = 1, the LXT318 drives the output data byte onto the SDO pin. The output data byte reports Loss of Signal (LOS) conditions, NLOOP detection status, HDB3 code setting, and operating modes (normal or diagnostic as shown in Table 5. The first bit (D0) reports LOS status. The second bit (D1) reports network loopback detection status. The third bit (D2) reports the HDB3 setting. The last 3 bits (D5 - D7) report operating modes and interrupt status.

The Host mode provides a latched Interrupt output pin, $\overline{INT}$. An interrupt is triggered by a change in the LOS bit (D0 of the output data byte). If the $\overline{INT}$ line is High (no interrupt is pending), bits D5 - D7 report the operating modes listed in Table 5. If the $\overline{INT}$ line is Low, the interrupt status overrides all other reports and bits D5 - D7 reflect the interrupt status as listed in Table 5.

2.4.3 Hardware Mode Operation

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. The LXT318 operates in Hardware mode only when MODE is Low or connected to RCLK.

2.5 Initialization and Reset

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the crystal oscillator is grounded, MCLK is used as the receiver reference clock. All PLLs are continuously calibrated.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, command reset by simultaneously writing 1s to RLOOP and LLOOP, and a 0 to TAOS. In Hardware mode, reset by holding RLOOP and LLOOP High simultaneously for 200 ns while holding TAOS Low. In either mode, reset sets all registers to 0.

Figure 4. LXT318 Line Attenuation (LATN) Pulse Width Encoding

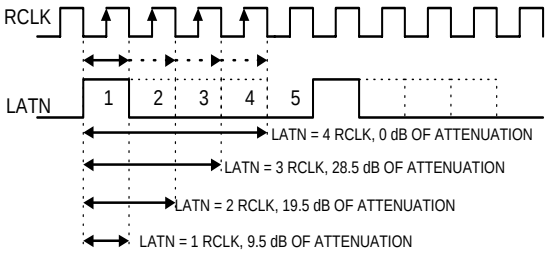


Table 5. LXT318 Serial Data Output Bit Coding (See **Figure 6**)

Bit			Status
D5	D6	D7	
Operating Modes			
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	LLOOP active
0	1	1	TAOS and LLOOP active
1	0	0	RLOOP active
Interrupt Status			
1	0	1	NLOOP has changed state since last Clear NLOOP occurred.
1	1	0	LOS has changed state since last Clear LOS occurred.
1	1	1	LOS and NLOOP have both changed state since last Clear NLOOP and Clear LOS occurred.

Figure 5. LXT318 Serial I/O Input Data Structure

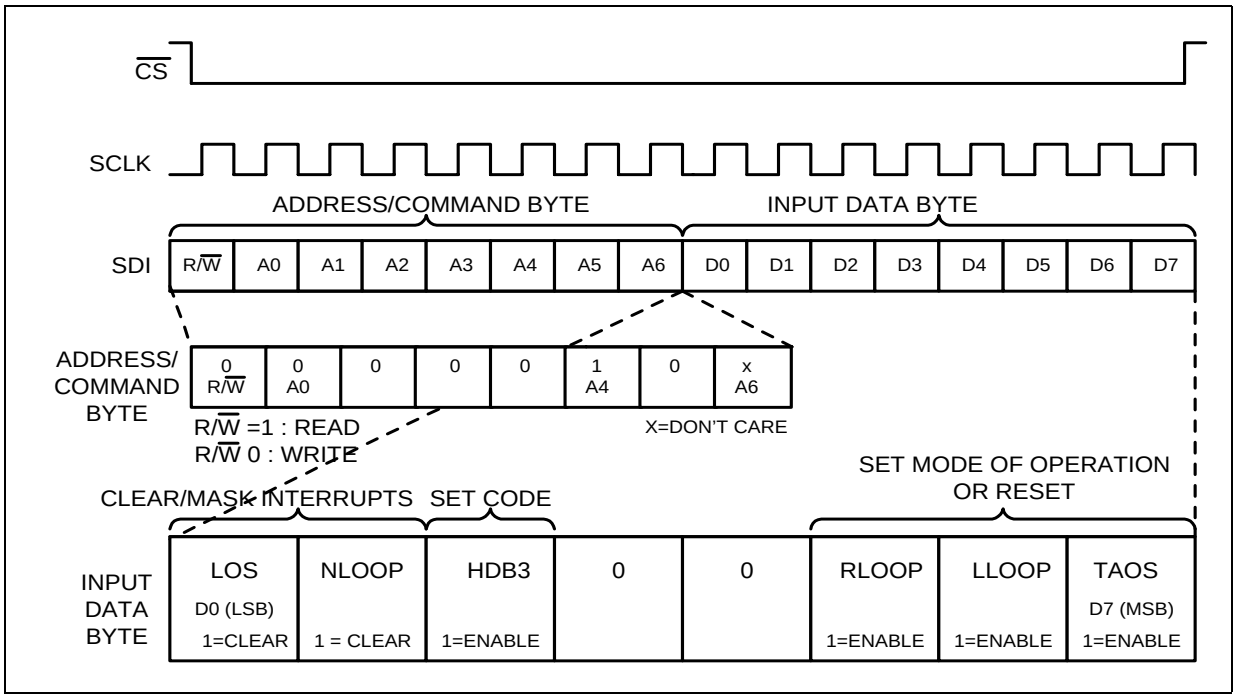
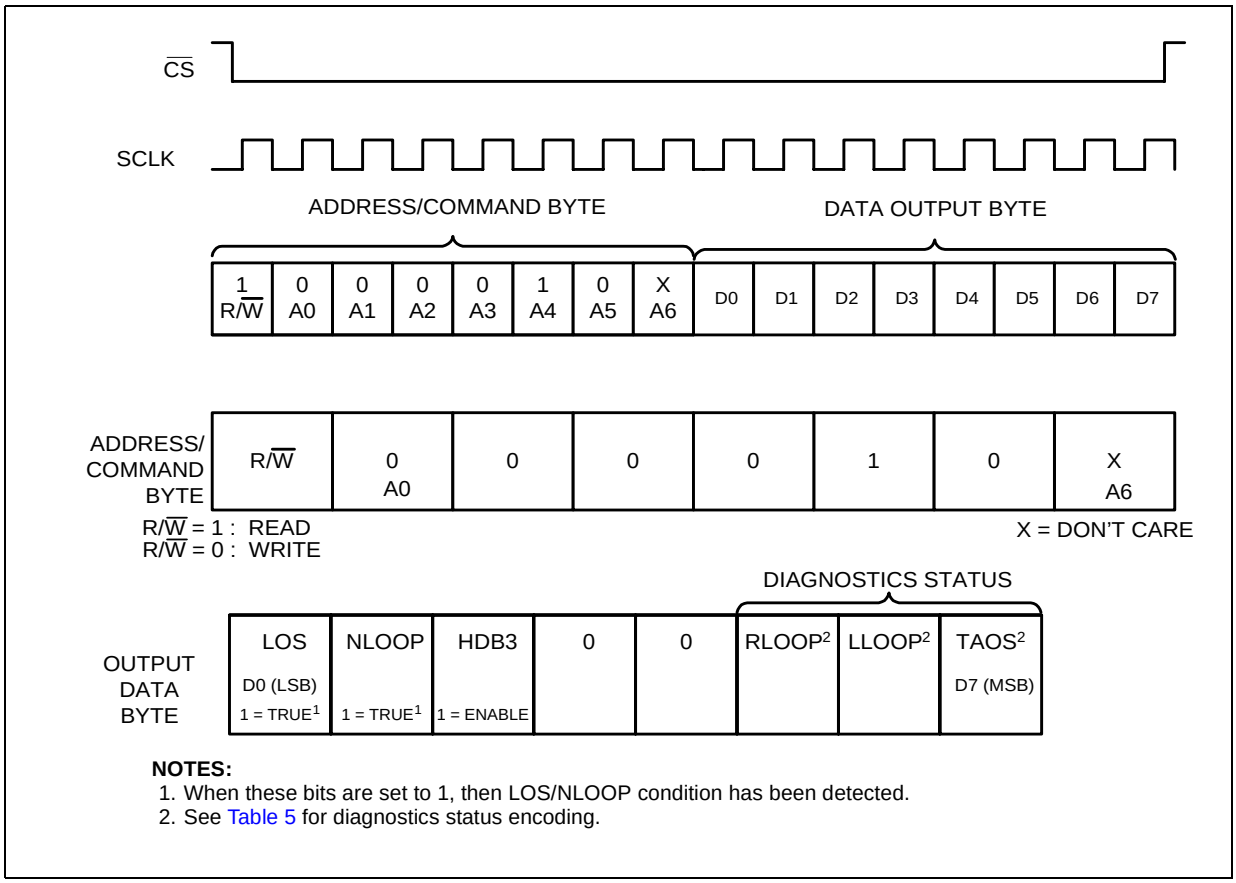


Figure 6. LXT318 Serial I/O Output Data Structure



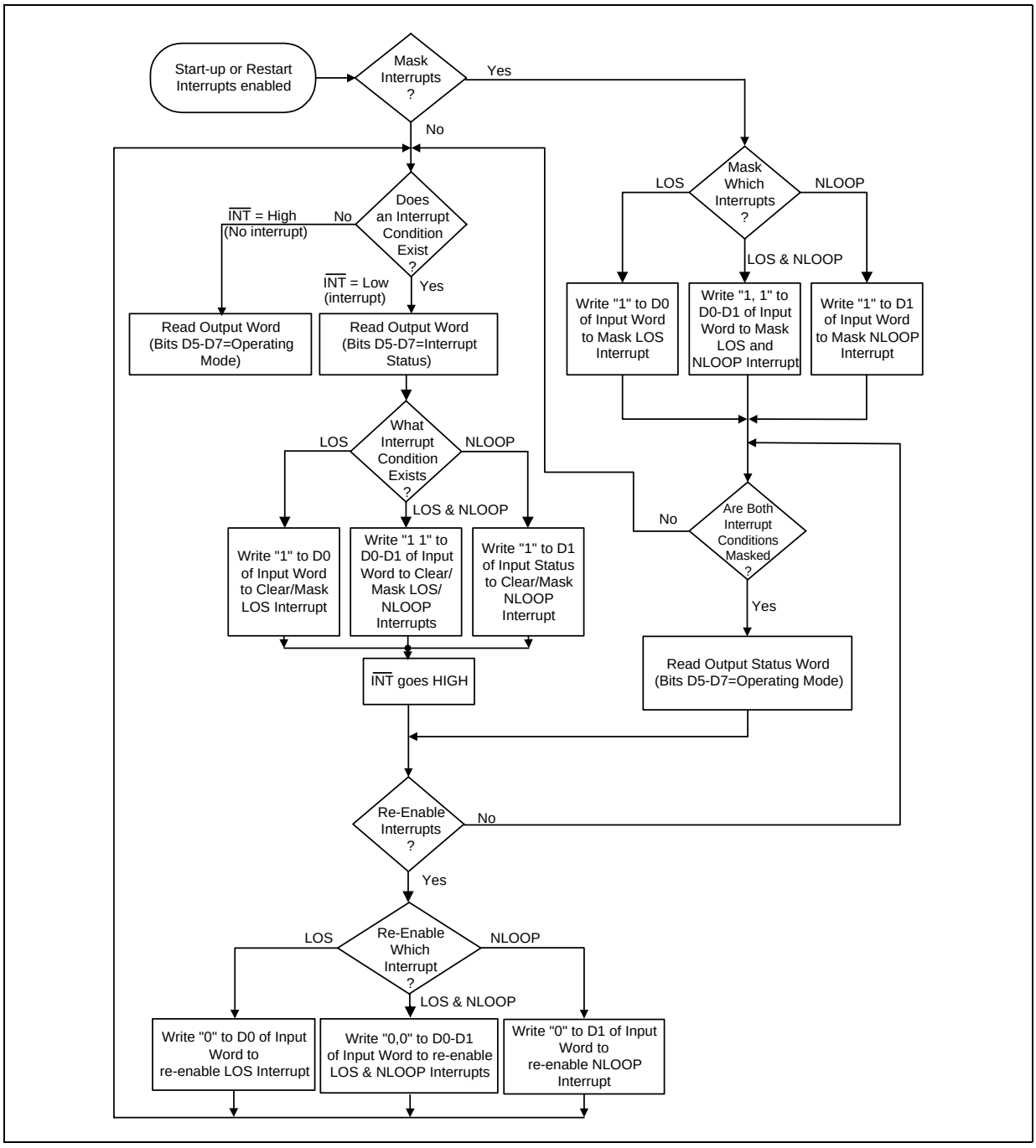
NOTES:
1. When these bits are set to 1, then LOS/NLOOP condition has been detected.
2. See Table 5 for diagnostics status encoding.

2.6 Interrupt Handling

Figure 7 shows how to mask the interrupt generator by writing a one to the respective bit of the input data byte LOS (D0) or NLOOP (D1). Either interrupt pulls the $\overline{INT}$ output pin Low. The output stage of the $\overline{INT}$ pin consists only of a pull-down device which requires an external pull-up resistor for it to function. To clear either interrupt:

1. If either of the interrupt bits LOS (D0) and NLOOP (D1) of the output data byte) is High, writing a one to the respective input bit (D0 or D1, of the input data byte) will clear the interrupt. Leaving a one in this bit position will effectively mask the interrupt. To re-enable the interrupt capability, reset D0 and/or D1 to 0.
2. If either the LOS or the NLOOP bit is Low, resetting the device will clear both interrupts. To reset the chip, set input bits D5 and D6 to one, and D7 to 0.

Figure 7. LXT318 Interrupt Handling



2.7 Diagnostic Mode Operation

2.7.1 Transmit All Ones.

See Figure 8A. In Transmit All Ones (TAOS) mode, the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1s at the TCLK frequency. When JASEL is set Low and TCLK is not provided, TAOS is locked to the MCLK. This can be used as the Blue Alarm Indicator (AIS). In Host mode, TAOS is commanded by writing a one to bit D7 of the input data byte. In Hardware mode, TAOS is commanded by setting TAOS High. TAOS can be commanded simultaneously with Local Loopback as shown in Figure 8B, but is inhibited during Remote Loopback.

Figure 8. Transmit All Ones

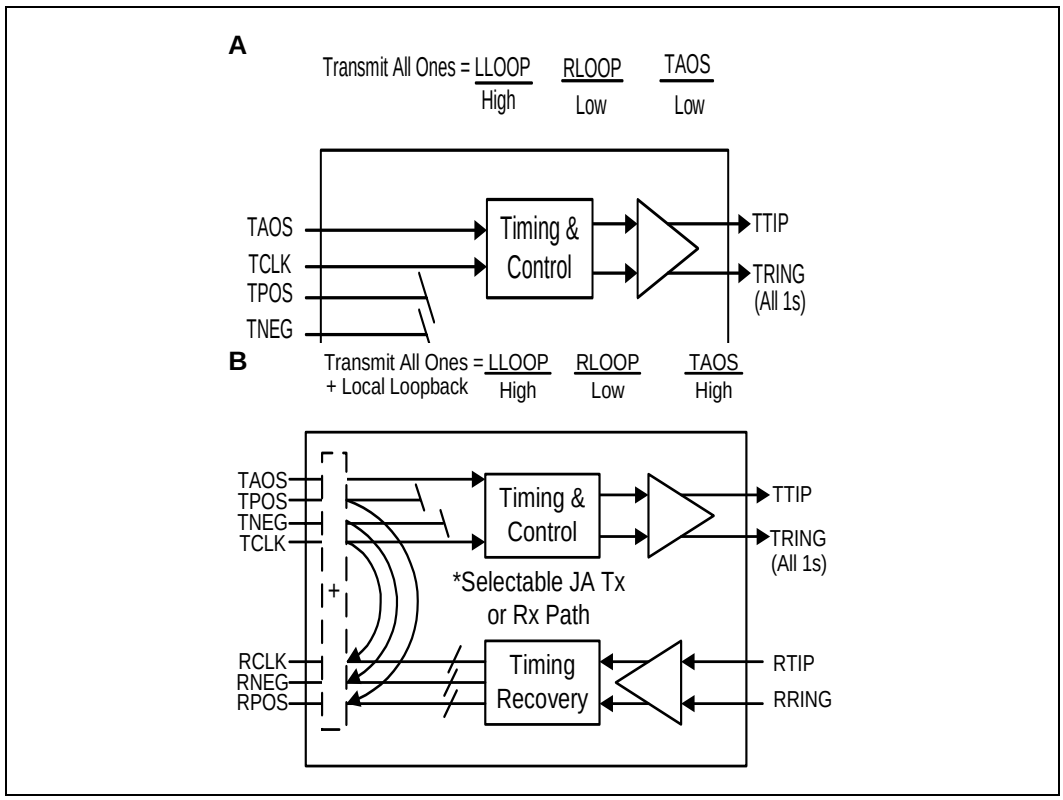
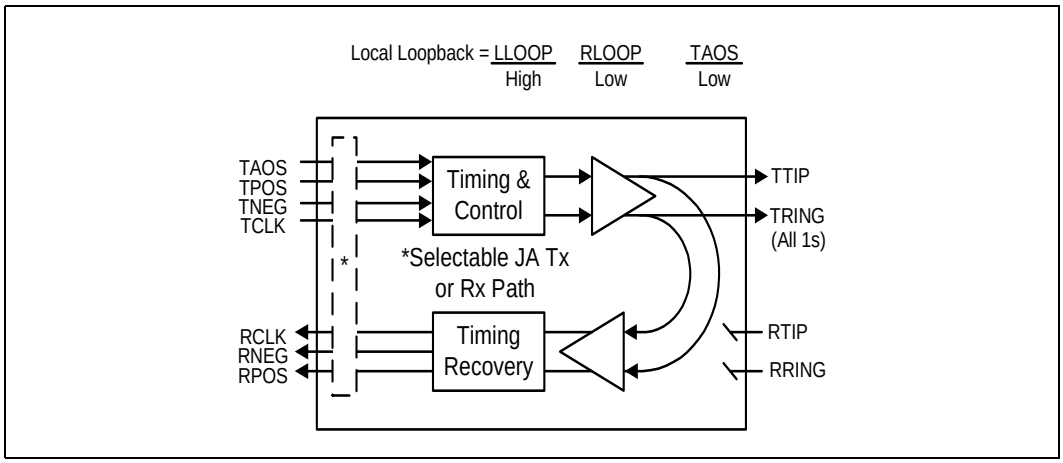


Figure 9. Local Loopback



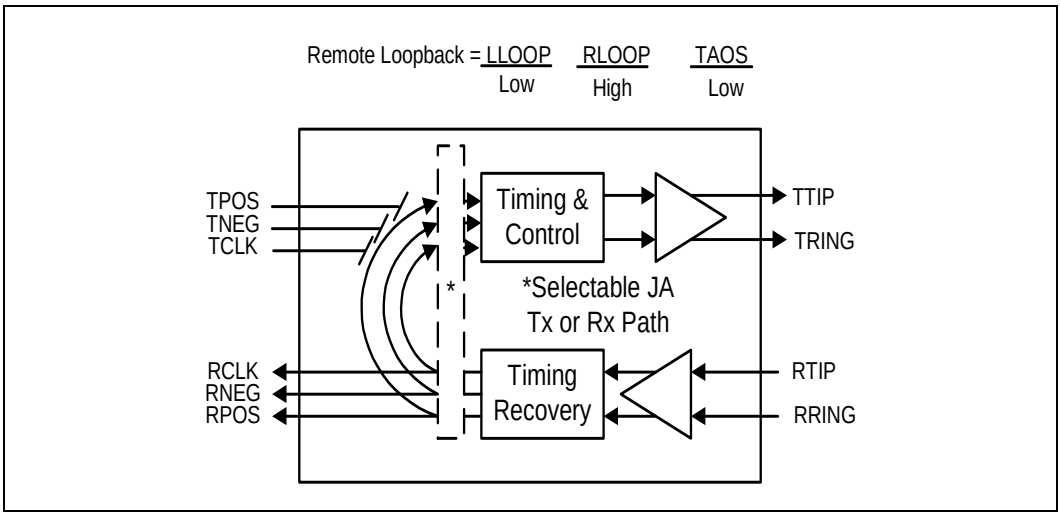
2.7.2 Local Loopback.

See Figure 9. Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks. During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Host mode, writing a one to bit D6 of the input data byte commands Local Loopback. In Hardware mode, Local Loopback is commanded by setting LLOOP High. If TAOS and LLOOP are both active, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data loops back to the RPOS/RNEG outputs through the jitter attenuator.

2.7.3 Remote Loopback.

See Figure 10. In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host mode, writing a one to bit D5 of the input data byte commands Remote Loopback. In Hardware mode, Remote Loopback is commanded by setting RLOOP High.

Figure 10. Remote Loopback



2.7.4 Network Loopback Detection.

In Host mode, to start the Network Loopback detection mode, write a one to each of RLOOP, LLOOP, and TAOS simultaneously and write all 0s in the next cycle. In Hardware mode, hold RLOOP, LLOOP and TAOS High simultaneously for 200 ns, then pull them all Low. Alternatively, tying RLOOP to RCLK will enable NLOOP.

With NLOOP detection enabled, the receiver monitors the input data for the NLOOP enable data pattern (00001). When either pattern repeats for five seconds, the device begins remote loopback operation. The LXT318 responds to either framed or unframed NLOOP patterns. Once the device begins NLOOP operation, the function is identical to remote loopback. When it detects the disable pattern (001) for five seconds or if RLOOP is enabled, the chip resets NLOOP. Activating LLOOP interrupts NLOOP temporarily, but it does not reset NLOOP.

3.0 Application Information

3.1 LATN Decoder

As shown in Figure 4, the line attenuation (LATN) output is encoded as a simple serial bit stream for use in line monitoring applications. Figure 11 shows a typical decoding circuit for the LATN signal. This circuit uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 6 lists the decoded output (L1 and L2) for each equalizer setting.

Figure 11. Typical LATN Decoding Circuit

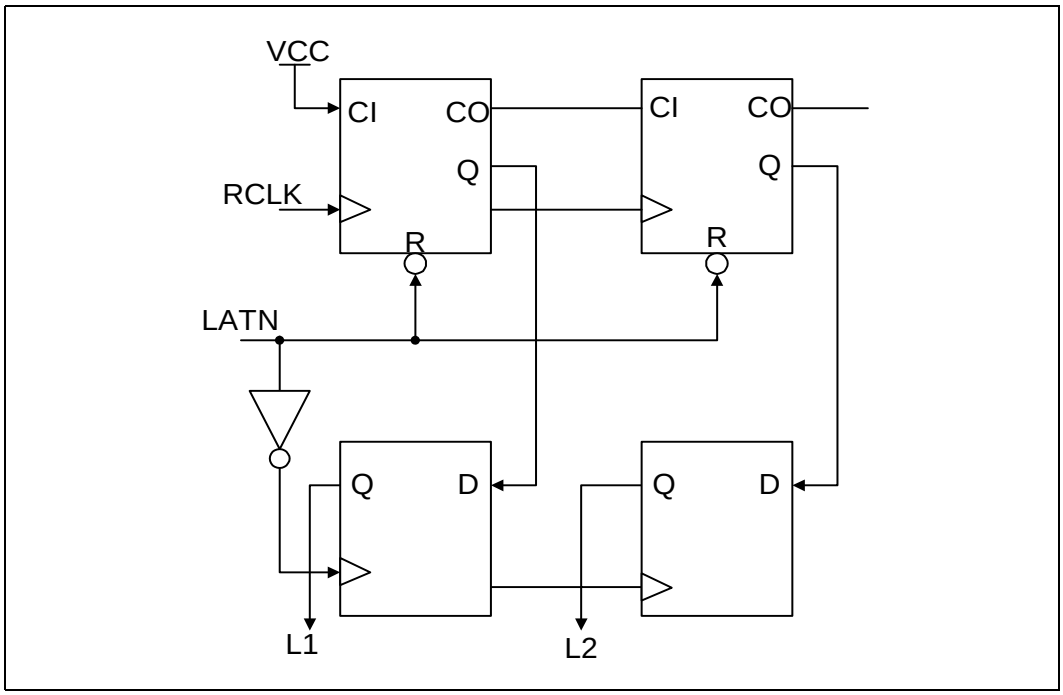


Table 6. Line Attenuation Decoding

L2	L1	Line Attenuation
0	0	0.0 dB
0	1	-9.5 dB
1	0	-19.5 dB
1	1	-28.5 dB

3.2 Power Requirements

The LXT318 is a low-power CMOS devices. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3V of each other, and decoupled to their respective grounds separately, as shown in Figure 12. Isolation between the transmit and receive circuits is provided internally.

3.3 Crystal Specifications

Table 7 shows the minimum specifications for the external crystal used by the LXT318 jitter attenuation loop.

Table 7. Jitter Attenuator Crystal Specifications

Parameter	Specification
Frequency	8.192 MHz
Frequency stability	±20 ppm @ 25° C ±25 ppm @ -40° to +85° C (ref 25° C reading)
Pullability (Pull range may be slightly asymmetrical)	C_L = 19 pF to 37 pF, crystal should pull -95 ppm to -115 ppm from nominal frequency C_L = 19 pF to 11.6 pF, crystal should pull +95 ppm to +130 ppm from nominal frequency
Effective series resistance	30 Ω maximum
Crystal cut	AT
Resonance	Parallel
Drive level	2.0 mW maximum
Mode of operation	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 fF typical;

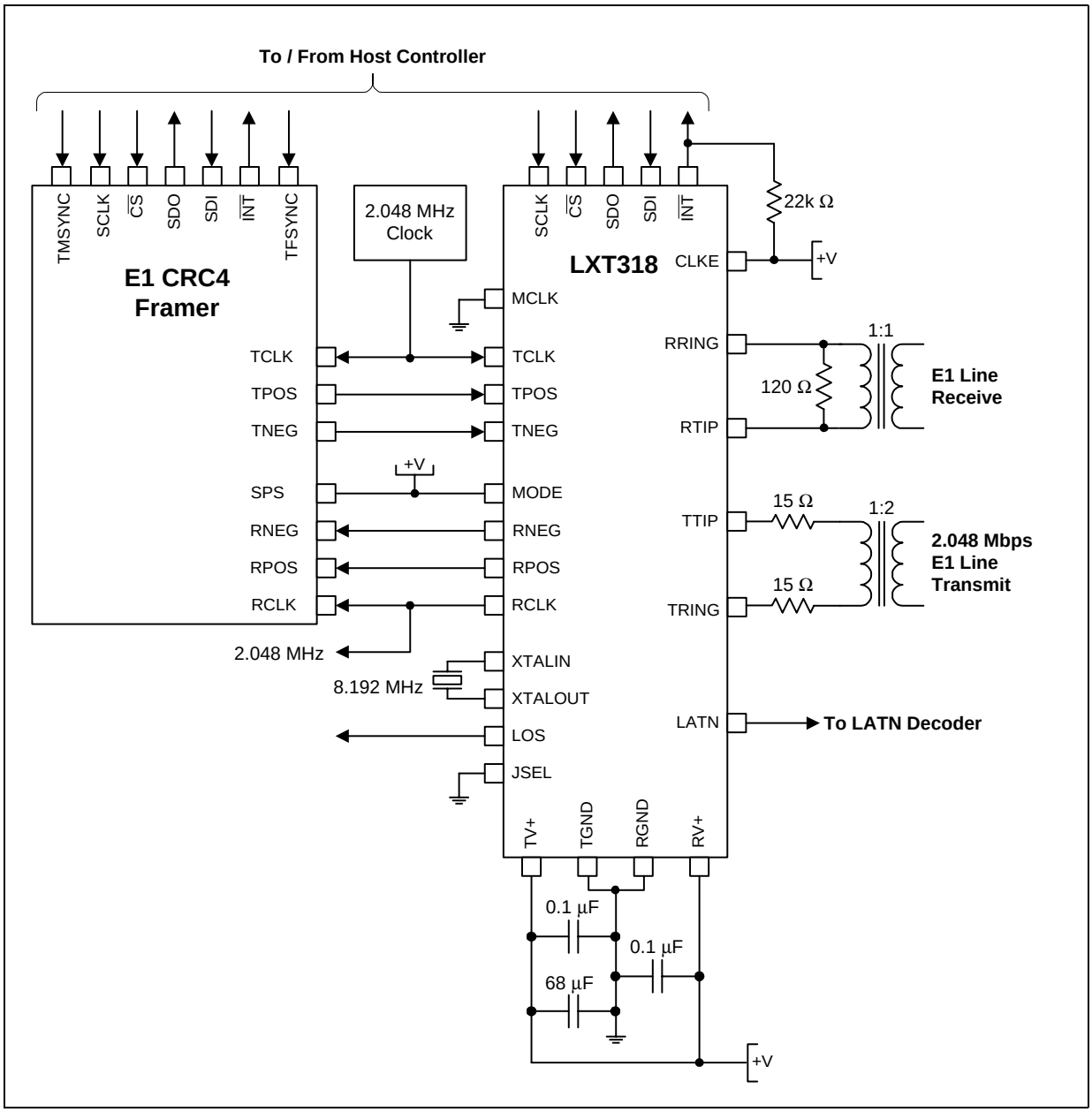
3.3.1 LXT318 Host Mode Applications

Figure 12 shows a typical E1 NTU application with the LXT318 operating in the Host mode (MODE pin tied High). The E1/CRC Framer provides the digital interface with the host controller. Both devices are controlled through the serial interface.

The 8.192 MHz crystal across XTALIN and XTALOUT enables the JAL that is switched to the transmit side by the Low on JASEL. The power supply pins are tied to a common bus with appropriate decoupling capacitors (68 µF and 0.1 µF) installed on each side.

A 120 Ω resistor (for TWP applications) across the input of a 1:1 transformer is used on the receive side, and a pair of 15 Ω resistors are installed in series with the 1:2 transmit transformer.

Figure 12. Typical LXT318 Host Mode E1/NTU, 120 Ω Twisted Pair Application



3.3.2 LXT318 Hardware Mode Applications

Figure 13 shows a typical 2.048 Mbps application with the LXT318 operating in the Hardware mode. This configuration is illustrated with a single power supply bus. CMOS control logic is used to set the TAOS, LLOOP and RLOOP diagnostic modes individually. The RCLK output is tapped to clock the MODE pin, enabling HDB3 encoding. The receive and transmit line interfaces are identical to the Host mode application shown in Figure 12.

Figure 13. Typical LXT318 Hardware Mode, 120 Ω Twisted Pair Application

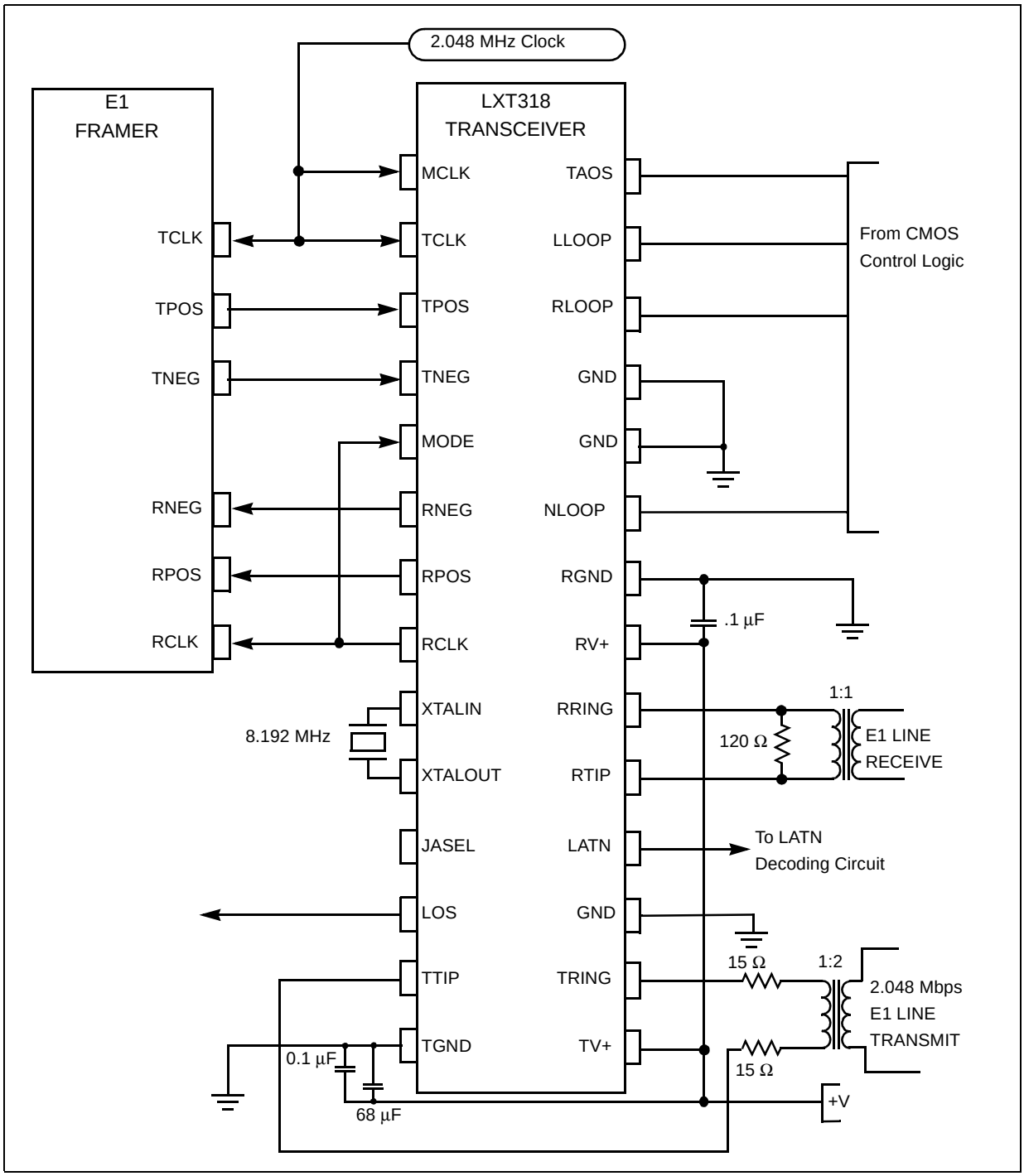
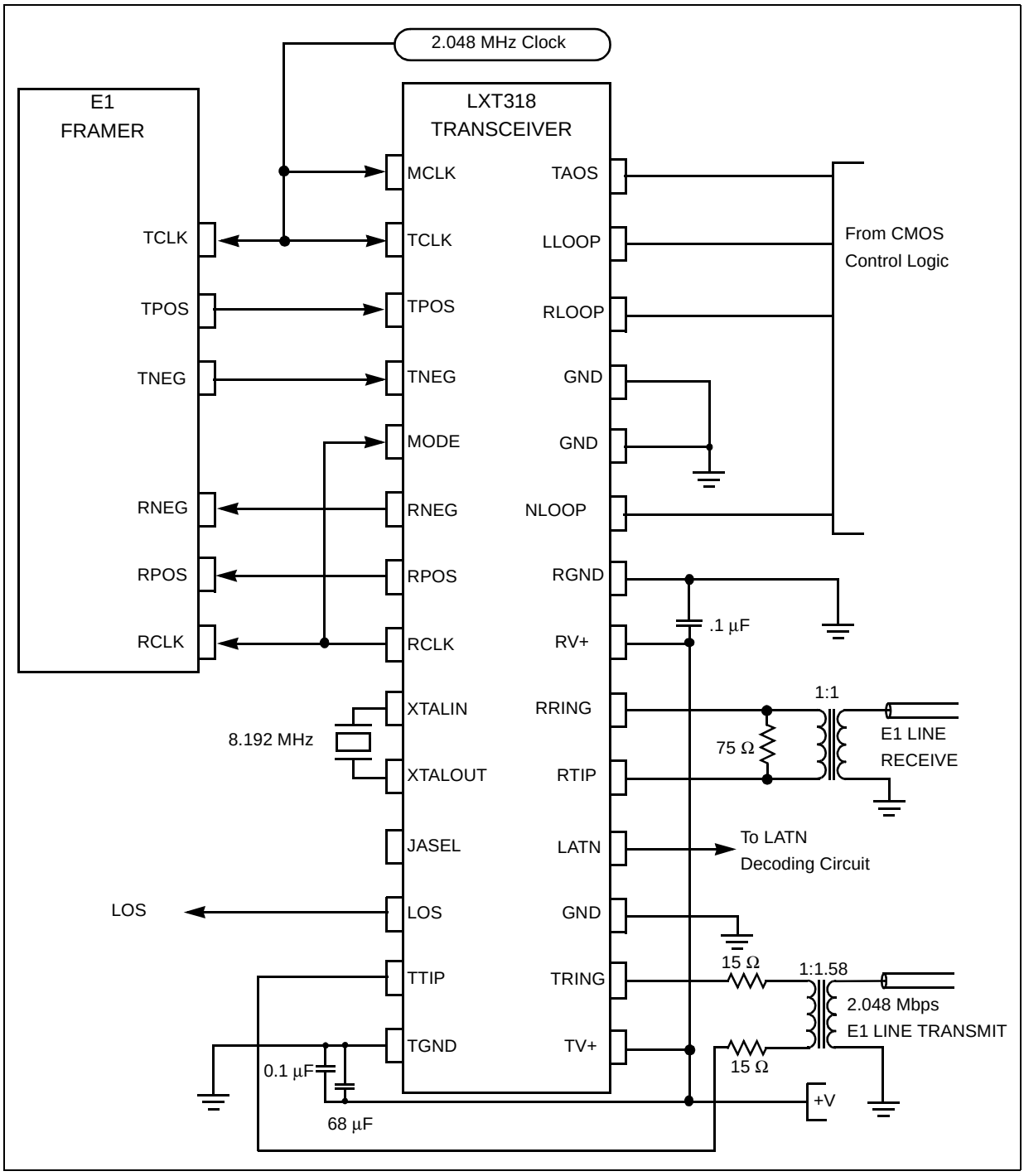


Figure 14. Typical LXT318 Hardware Mode, 75 Ω Coax Application



4.0 Test Specifications

Note: The minimum and maximum values in Table 8 through Table 14 and Figure 19 through Figure 24 represent the performance specifications of the LXT318 and are guaranteed by test, except where noted by design.

Table 8. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin	V_{IN}	RGND, -0.3	RV+, +0.3	V
Input current, any pin [1]	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	° C

Caution: Operation at or beyond these limits may permanently damage the device. Normal operation not guaranteed at these extremes.

1. Transient Currents of up to 100 mA will not cause SCR latch-up. TTIP TRING, TV+, TGND can withstand continuous current of 100 mA.

Table 9. Recommended Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
DC supply[2]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	-	+85	°C	
Power dissipation[3]	P_D	-	300	400	mW	100% ones density & maximum line length @ 5.25 V

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TV+ must not differ from RV+ by more than 0.3 V.
3. Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 10. Digital Characteristics (Over Recommended Operating Conditions)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
High level input voltage[1,2] (pins 1-5, 10, 23-28)	V_{IH}	2.0	–	–	V	
Low level input voltage[1,2] (pins 1-5, 10, 23-28)	V_{IL}	–	–	0.8	V	
High level input voltage[1,2] (pins 6-8, 12, 23, 25)	V_{OH}	2.4	–	–	V	I_{OUT} = -400 µA
Low level input voltage[1,2] (pins 6-8, 12, 23, 25)	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current	I_{LL}	0	–	±10	µA	
Three-state leakage current[1] (pin 25)	$I3_L$	0	–	±10	µA	
Driver power down current[3]	I_{PD}	–	–	±1.2	mA	Direct connection to VCC or GND

1. Functionality of pins 23 and 25 depends on mode. See Host/Hardware Mode descriptions.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. TTIP, TRING only in Idle or Power Down Mode.

Table 11. Analog Characteristics (Over Recommended Operating Conditions)

Parameter		Min	Typ[1]	Max	Unit	Test Conditions
Recommended output load at TTIP and TRING		50	120	200	Ω	
AMI output pulse amplitudes		2.7	3.0	3.3	V	Measured at the output
Jitter added by the transmitter[2]	20 Hz - 100kHz[3]	–	–	0.05	UI	
Input jitter tolerance	20 Hz - 100kHz	0.2	0.3	–	UI	0 - 43 dB line
	10 Hz	100	500	–	UI	
Jitter attenuation curve corner frequency[4]		–	3	–	Hz	
Receive signal attenuation range		0	43	–	dB	
Allowable consecutive zeros before LOS		160	175	190	–	
Transmitter return loss[3]	51 kHz - 102 kHz	–	18	–	dB	
	102 kHz - 2.048 MHz	–	24	–	dB	
	2.048 MHz - 3.072 MHz	–	22	–	dB	
Receiver return loss[3, 5]	51 kHz - 102 kHz	–	20	–	dB	
	102 kHz - 2.048 MHz	–	24	–	dB	
	2.048 MHz - 3.072 MHz	–	22	–	dB	

1. Typical figures are at 25 °C and are for design aid only, not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter free.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
5. Measured with 1:1 transformer terminated with 120 Ω resistance.

Table 12. LXT318 Master Clock and Transmit Timing Characteristics (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Master clock frequency	MCLK	–	2.048	–	MHz	
Master clock tolerance	MCLKt	–	±100	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Crystal frequency	fc	–	8.192	–	MHz	
Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 15. LXT318 Transmit Clock Timing

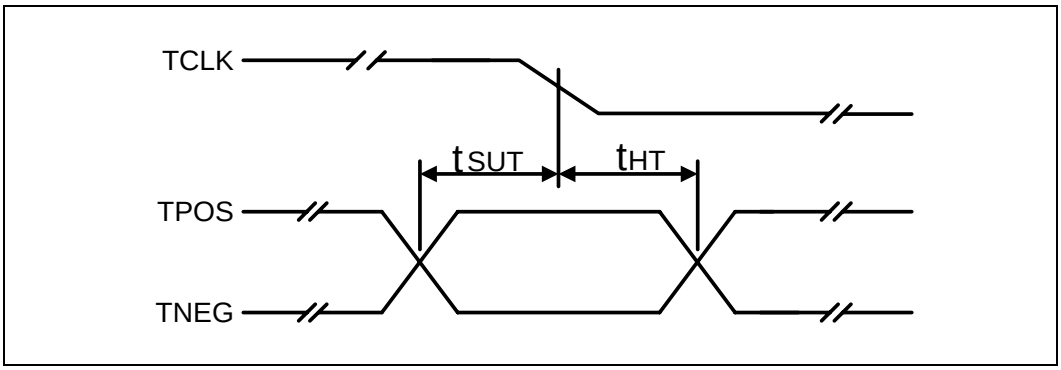


Figure 16. LXT318 Receive Clock Timing

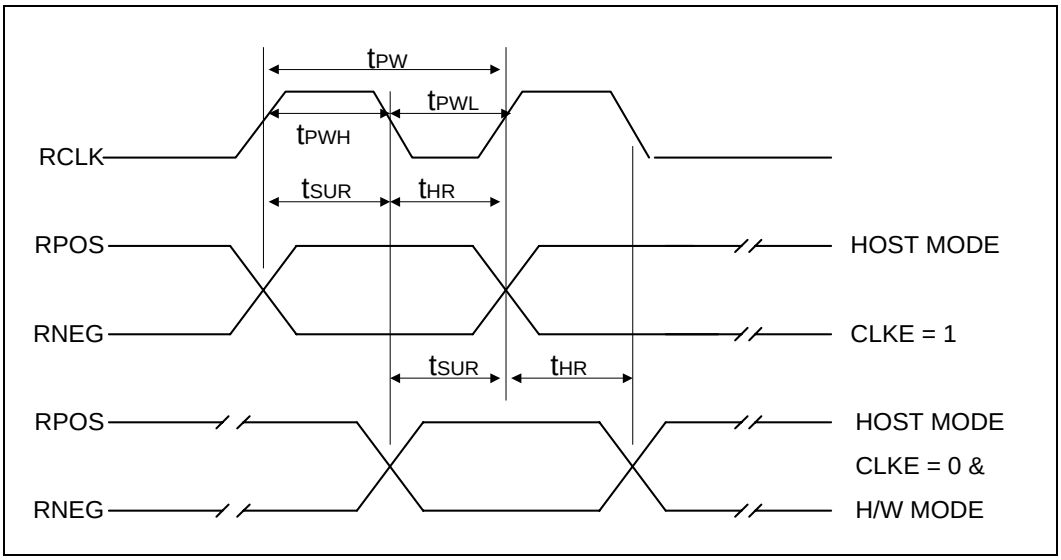


Table 13. LXT318 Receive Timing Characteristics (See **Figure 16**)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Receive clock duty cycle[2]	RCLKd	40	50	60	%	
Receive clock pulse width[2]	t_{PW}	-	488	-	ns	
Receive clock pulse width High	t_{PWH}	-	244	-	ns	
Receive clock pulse width Low	t_{PWL}	220	244	268	ns	
RPOS/RNEG to RCLK rising setup time	t_{SUR}	-	194	-	ns	
RCLK rising to RPOS/RNEG hold time	t_{HR}	-	194	-	ns	

1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and min. RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 2.048 Mbps).

Table 14. LXT318 Serial I/O Timing Characteristics (See Figure 17 and Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Unit	Parameter
Rise/fall time—any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	t_{CC}	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	t_{CCH}	150	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid time	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	t_{CDZ}	–	100	–	ns	
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 17. LXT318 Serial Data Input Timing Diagram

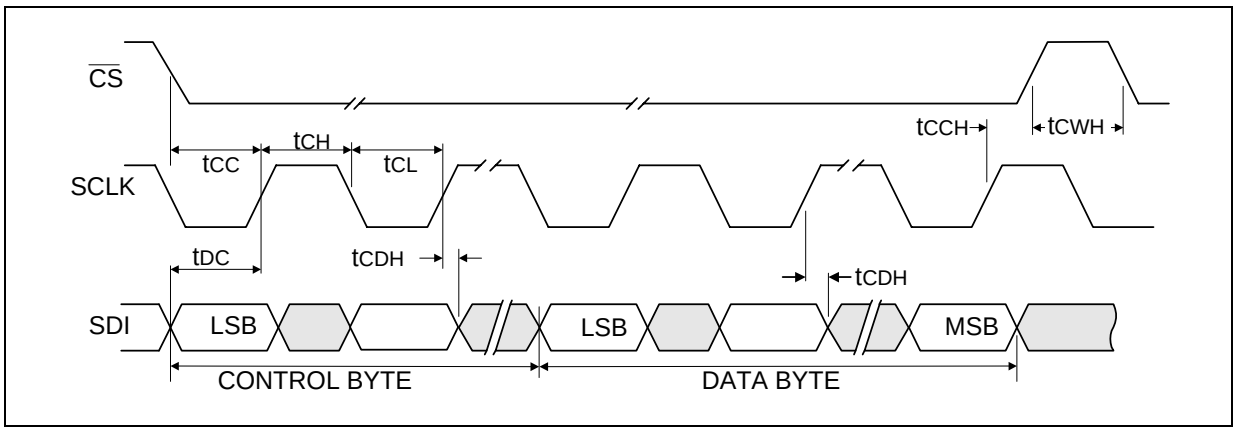


Figure 18. LXT318 Serial Data Output Timing Diagram

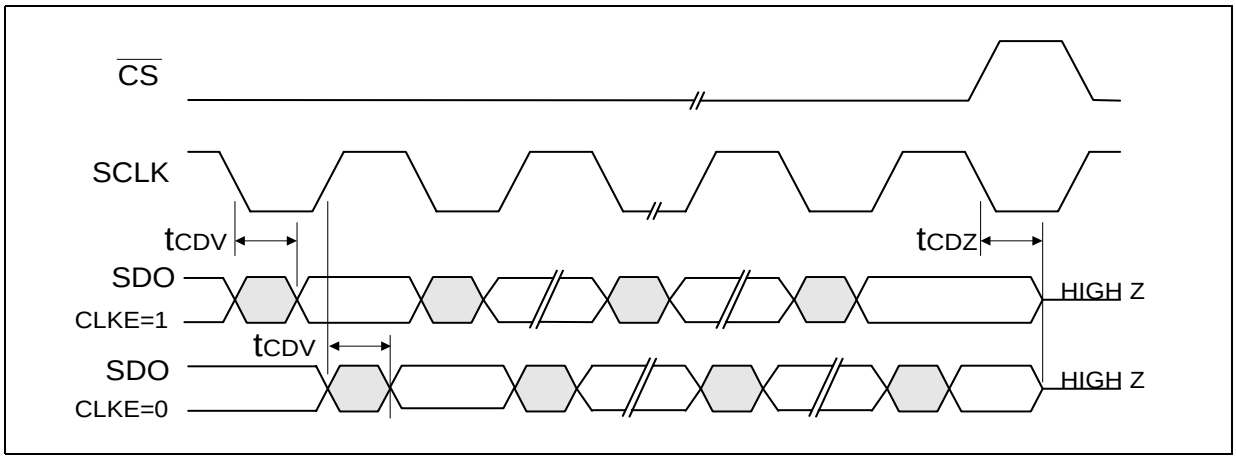


Figure 19. LXT318 Jitter Tolerance @ 43 dB (Typical)

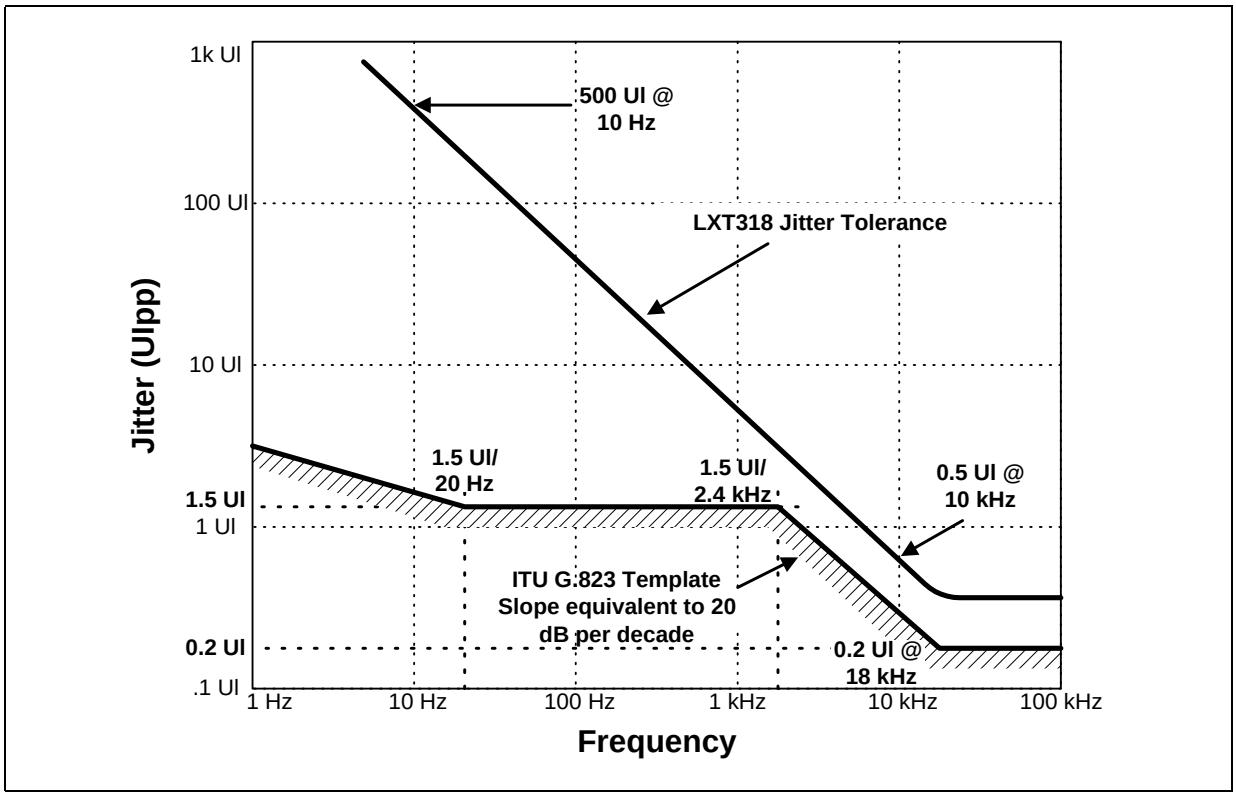


Figure 20. LXT318 Jitter Attenuation (Typical)

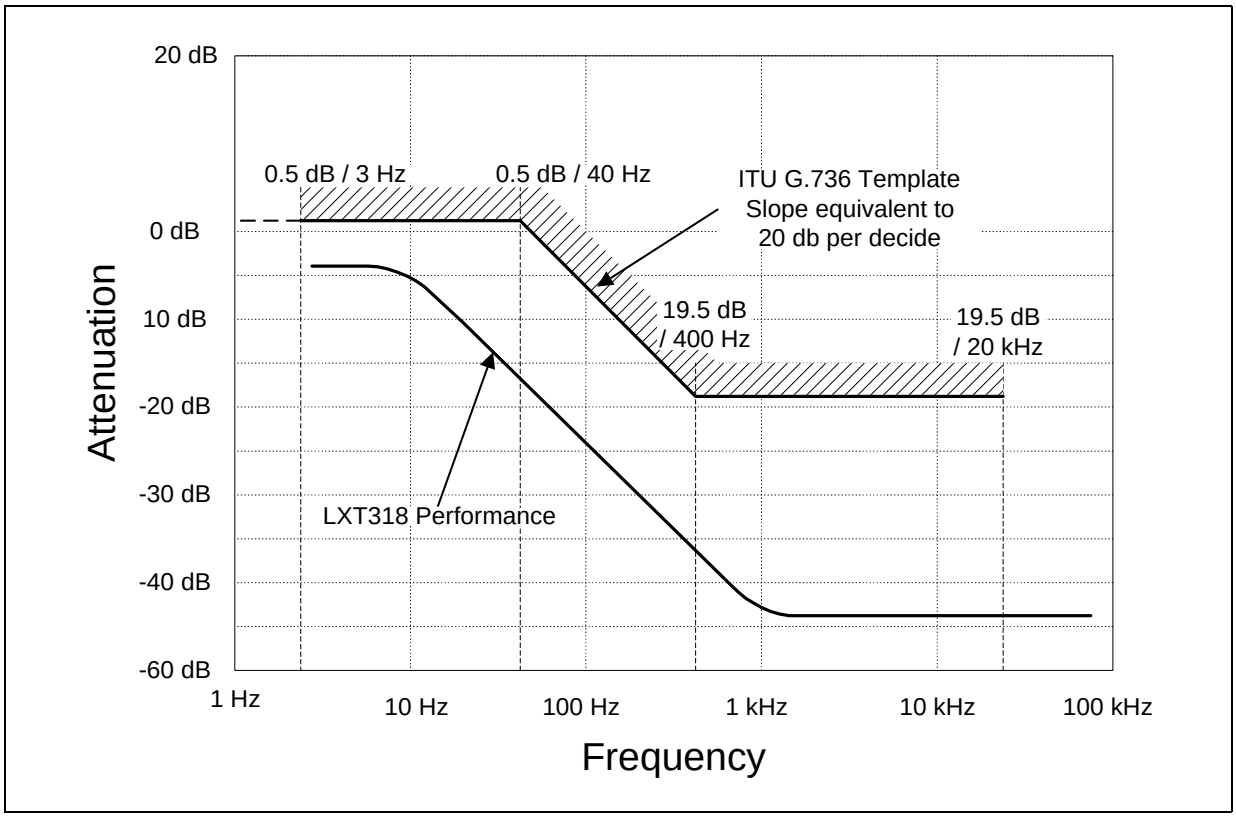


Figure 21. Input and Maximum Output Jitter Specified by TBR12/13

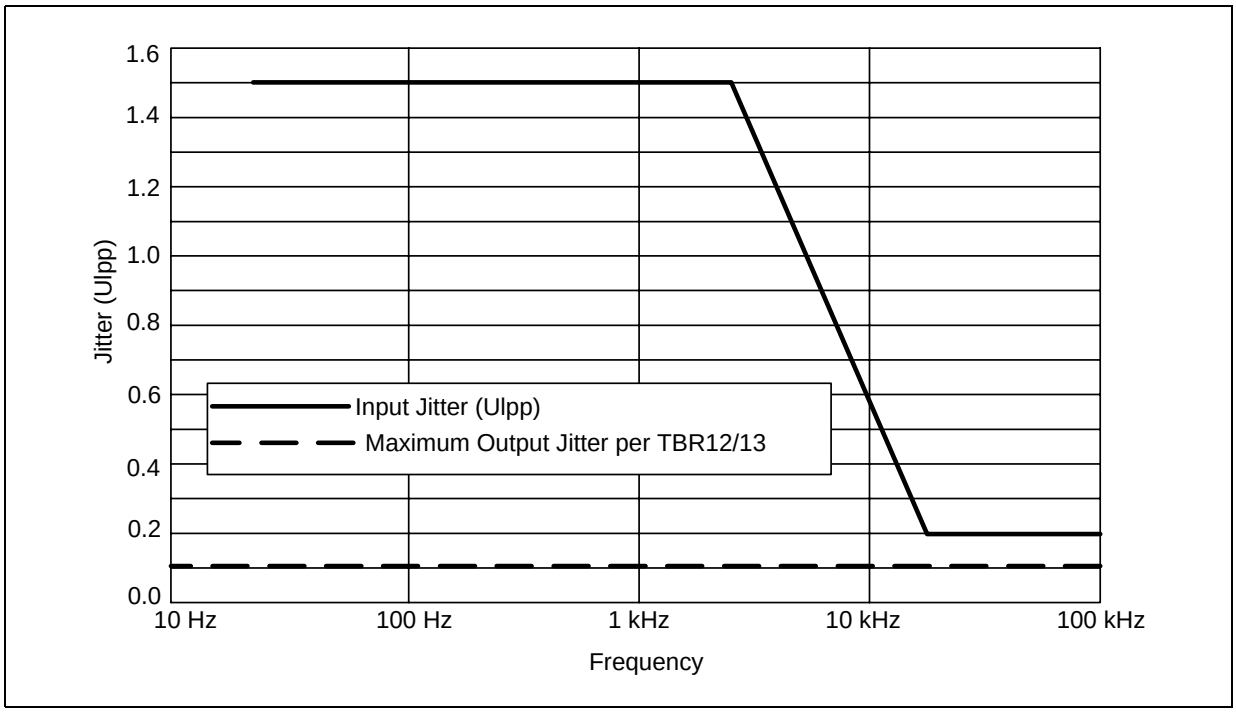


Figure 22. LXT318 Jitter Attenuation Performance (Typical–Measured Against TBR12/13)

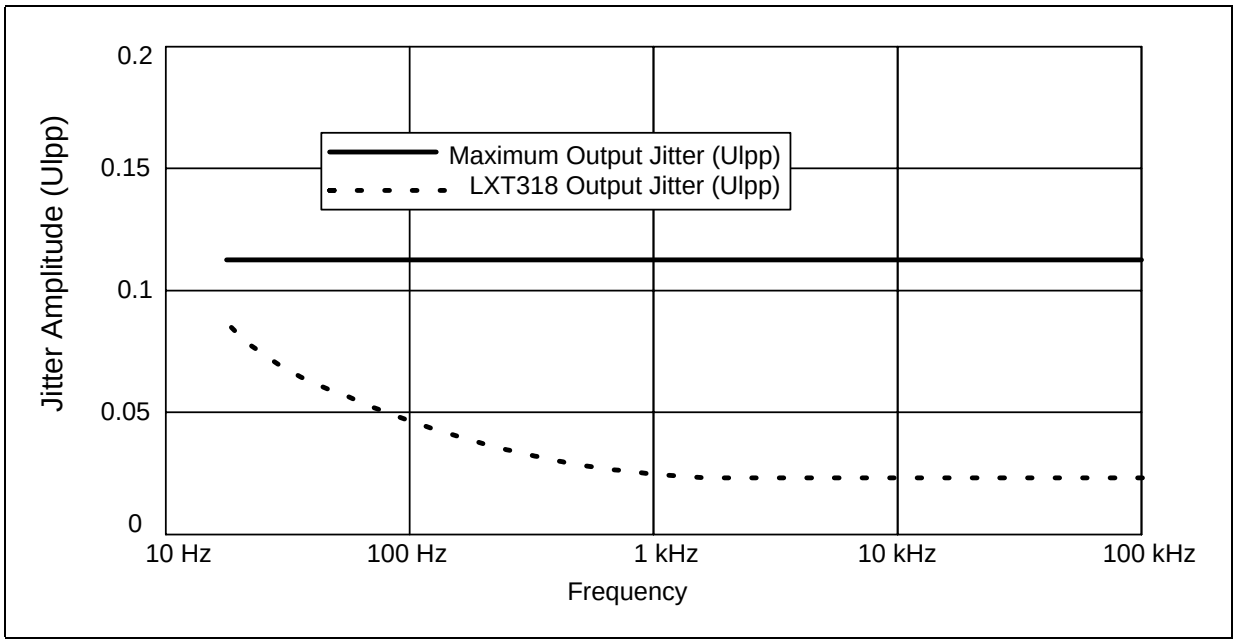


Figure 23. 2.048 Mbps Pulse Mask

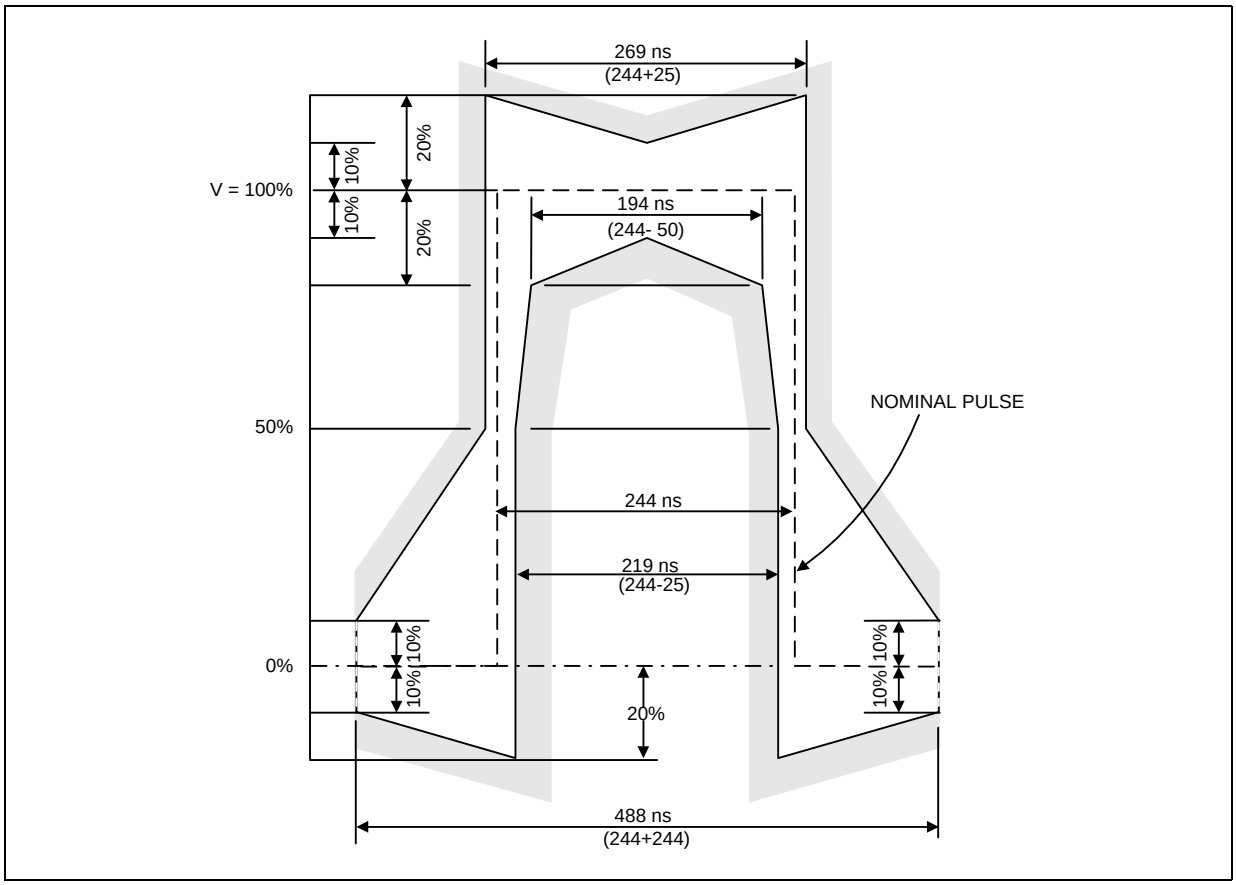
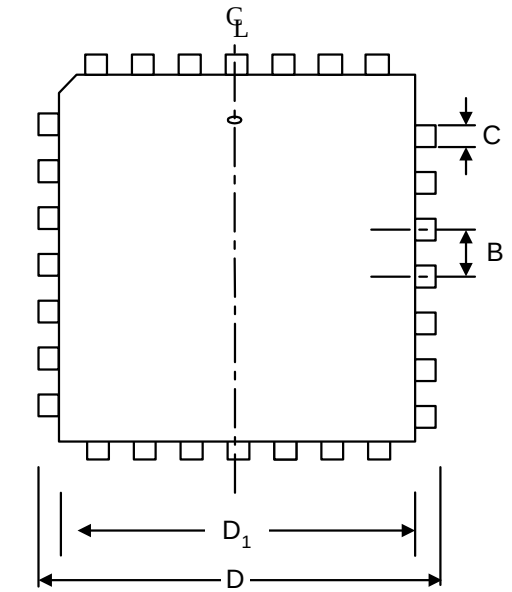


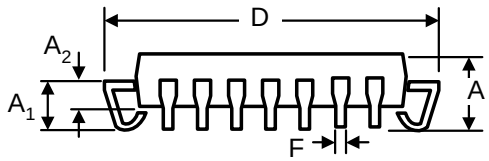
Table 15. 2.048 Mbps Pulse Mask Parameters

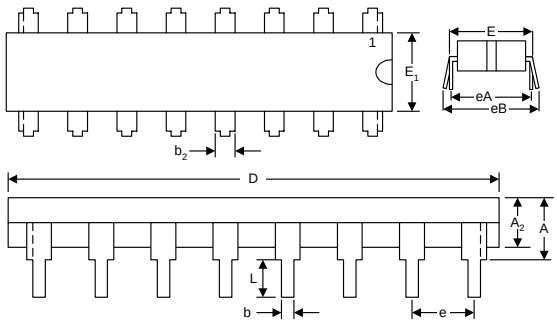
Parameter	TPW	Unit
Test load impedance	120	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ± 0.30	V
Nominal pulse width	244	ns
Ratio of positive and negative pulse amplitude at center of pulse	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	%

5.0 Mechanical Specifications

Figure 24. Package Specifications







28-Pin Plastic Leaded Chip Carrier

- Extended Temperature Range (-40°C to + 85°C)
- P/N LXT318PE

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers

28-Pin Plastic Dual In-Line Package

- Extended Temperature Range (-40°C to + 85°C)
- P/N LXT318NE

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.250	–	6.350
A2	0.125	0.195	3.175	4.953
b	0.014	0.022	0.356	0.559
b2	0.030	0.070	0.762	1.778
D	1.380	1.565	35.052	39.751
E	0.600	0.625	15.240	15.875
E1	0.485	0.580	12.319	14.732
e	0.100 BSC[1] (nominal)		2.540 BSC[1] (nominal)	
eA	0.600 BSC[1] (nominal)		15.240 BSC[1] (nominal)	
eB	–	0.700	–	17.780
L	0.115	0.200	2.921	5.080

1. BSC—Basic Spacing between Centers