LXT381

Octal E1 Line Interface Unit

Datasheet

General Description

The LXT381 is an octal short haul analog Line Interface Unit for ITU G.703 2.048 Mbit/sec. transmission systems. It incorporates eight independent receivers and eight independent transmitters in a single LQFP-144 or PBGA-160 package.

The transmit output drivers provide low impedance, constant during marks and spaces and constant pulse amplitudes independent of supply voltage variations.

The LXT381 may be configured for unbalanced 75Ω or for balanced 120Ω systems without external component changes in the transmit section. The transmit return loss performance exceeds latest ETSI return loss recommendations such as ETS 300166.

The LXT381 features a differential data receiver architecture with high noise interference margin. The receivers use peak detection and a variable threshold for reliable data recovery down to 500 mV or up to 12 dB of cable attenuation.

Each receiver incorporates an analog Loss Of Signal (LOS) processor that meets latest ITU G.775 standard.

The fast power down mode of all transmitters allows the implementation of Hitless Protection Switching (HPS) application without the use of relays.

Applications

- Synchronous Digital Hierarchy (SDH) E1 tributary interfaces
- Public switching trunk line interfaces
- Digital Access Cross Connects (DACS)
- Microwave transmission systems

Product Features

- Octal E1 short haul line interface per ITU G.703
- Single rail supply voltage of 3.3V with 5V I/O capability
- Low power consumption of <100 mW per channel (typ.)
- 75Ω/120Ω TX operation without component changes
- Transmit return loss complies with ETSI ETS 300 166
- Hitless Protection Switching (HPS)
- Driver short circuit current limiter (<50 mA RMS)
- Differential receiver with 15dB of signal to noise interference margin
- Data recovery with no need for external reference clock
- Analog LOS detection per ITU G.775
- Simple hardware control mode
- JTAG Boundary Scan test port per IEEE 1149.4
- Small footprint 144 pin LQFP or 160 pin PBGA package

As of January 15, 2001, this document replaces the Level One document known as *Octal E1 Line Interface*.

Order Number: 249005-001
January 2001

Datasheet

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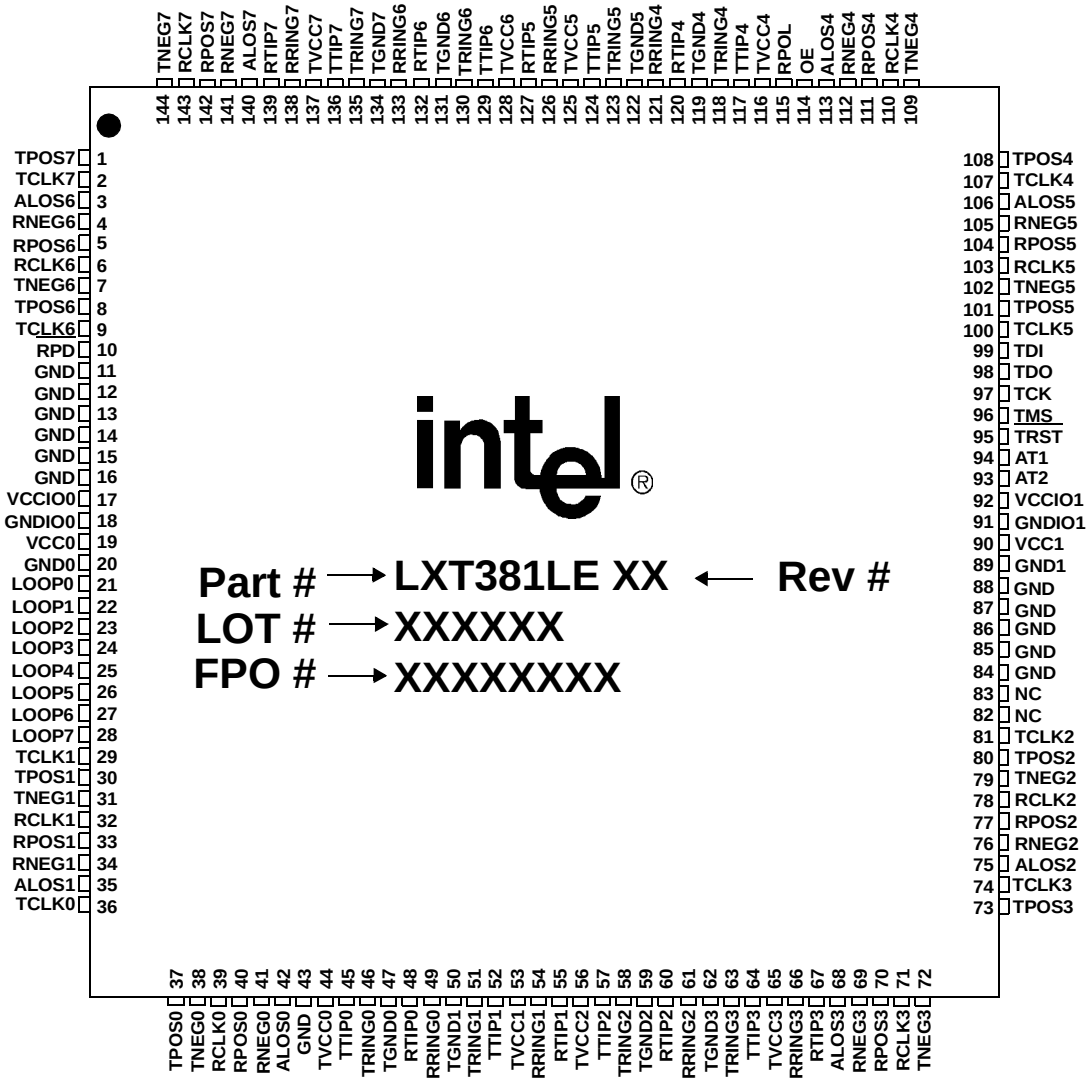


Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Figure 2. LXT381 160-Pin Plastic Ball Grid Array (PBGA) Pin Assignments

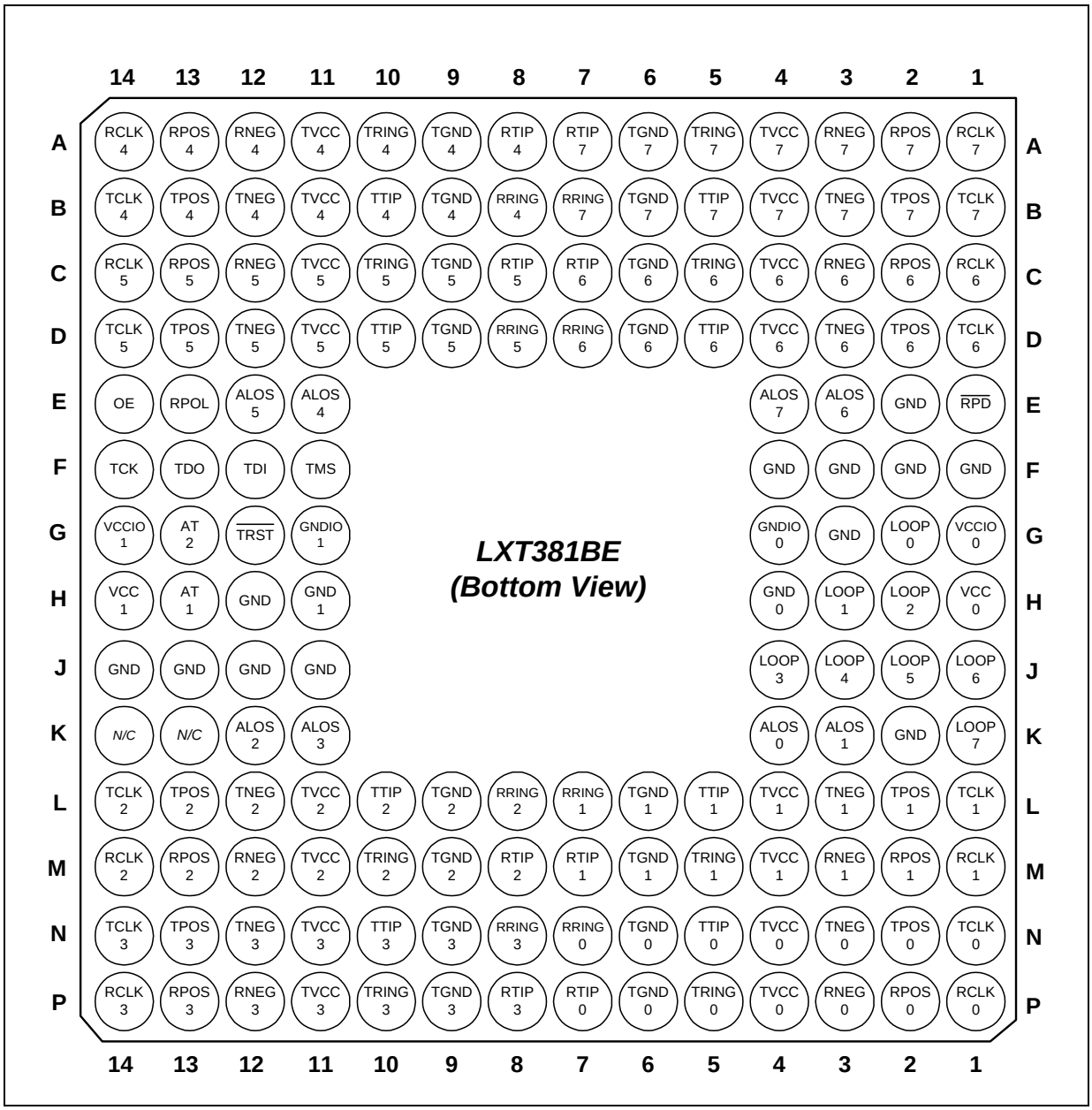


Table 1. LXT381 Pin Description

Pin # LQFP	Pin # PBGA	Symbol	I/O[1]	Description
1	B2	TPOS7	DI	**Transmit Positive Data Input.**
2	B1	TCLK7	DI	**Transmit Clock Input.** When TCLK is active, TPOS and TNEG work as NRZ inputs. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is held High, TPOS and TNEG work as RZ inputs. In this mode, pulse widths are determined by TPOS and TNEG duty cycles. An analog timer is used to determine if TCLK is high for at least 12 µ seconds in order to enable the above function. If TCLK is held Low, the output drivers enter a low power high Z mode. **TCLK** **Operating Mode** Clocked NRZ H RZ L Driver Tri-State
3	E3	ALOS6	DO	**Analog Loss of Signal Output.** Please refer to the ALOS functional description.
4 5	C3 C2	RNEG6 RPOS6	DO DO	Receive Negative Data Output. Receive Positive Data Output. These pins act as RZ data receiver outputs. The output polarity is selectable with RPOL The pins will be active High polarity when RPOL is High and Active Low Polarity when RPOL is Low. RPOS and RNEG will be active when the corresponding transceiver is in LOS. RPOS and RNEG will be in high impedance state if the $\overline{\text{RPD}}$ pin is Low.
6	C1	RCLK6	DO	**Receive Clock Output.** RPOS and RNEG are internally connected to an EXOR that is fed to the RCLK output for external clock recovery applications. RCLK will be in high impedance state if the $\overline{\text{RPD}}$ pin is Low.
7 8	D3 D2	TNEG6 TPOS6	DI DI	**Transmit Negative Data Input.** **Transmit Positive Data Input.** When TCLK is active, TPOS/TNEG are active high NRZ inputs. TPOS indicates the transmission of a positive pulse whereas TNEG indicates the transmission of a negative pulse. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is held High, TPOS and TNEG work as RZ inputs. In this mode, pulse widths are determined by TPOS and TNEG duty cycles. An analog timer is used to determine if TCLK is high for at least 12 µ seconds in order to enable the above function. **TCLK** **TPOS/TNEG Operating Mode** Clocked NRZ H RZ
9	D1	TCLK6	DI	**Transmit Clock Input.**
10	E1	$\overline{\text{RPD}}$	DI	**Receiver Power Down Input.** If $\overline{\text{RPD}}$ is Low, the complete receive path is powered down and the output pins RCLK, RPOS and RNEG are switched to Tri-state mode.
11	E2	GND	S	**Ground.** This pin must be connected to Ground.
12	F1	GND	S	**Ground.** This pin must be connected to Ground.
13	F2	GND	S	**Ground.** This pin must be connected to Ground.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT381 Pin Description (Continued)

Pin # LQFP	Pin # PBGA	Symbol	I/O[1]	Description
14	F3	GND	S	**Ground.** This pin must be connected to Ground.
15	F4	GND	S	**Ground.** This pin must be connected to Ground.
16	G3	GND	S	**Ground.** This pin must be connected to Ground.
17	G1	VCCIO0	S	**Power (I/O).**
18	G4	GNDIO0	S	**Ground (I/O).**
19	H1	VCC0	S	**Power (Core).**
20	H4	GND0	S	**Ground (Core).**
21 22 23 24 25 26 27 28	G2 H3 H2 J4 J3 J2 J1 K1	LOOP0 LOOP1 LOOP2 LOOP3 LOOP4 LOOP5 LOOP6 LOOP7	DI DI DI DI DI DI DI DI	**Loopback Mode Select/Parallel Databus Input & Output.** These pins are inputs that select the loopback mode for transceiver ports 0-7 respectively as follows: Normal operation (no loopback) is selected when pin is left open (unconnected). Remote loopback mode is selected when pin is Low. In this mode, data on TPOS and TNEG is ignored and data received on RTIP and RRING is looped around and retransmitted on TTIP and TRING. Analog local loopback mode is selected when pin is High. In this mode, data received on RTIP and RRING is ignored and data transmitted on TTIP and TRING is internally looped around and routed back to the receive inputs. ***Note:*** When these inputs are left open, they stay in a high impedance state. Therefore, the layout design should not route signals with fast transitions near the LOOP pins. This practice will minimize capacitive coupling.
29	L1	TCLK1	DI	**Transmit Clock Input.**
30 31	L2 L3	TPOS1 TNEG1	DI DI	**Transmit Positive Data Input.** **Transmit Negative Data Input.**
32	M1	RCLK1	DO	**Receive Clock Output.**
33 34	M2 M3	RPOS1 RNEG1	DO DO	**Receive Positive Data Output.** **Receive Negative Data Output.**
35	K3	ALOS1	DO	**Analog Loss of Signal Output.**
36	N1	TCLK0	DI	**Transmit Clock Input.**
37 38	N2 N3	TPOS0 TNEG0	DI DI	**Transmit Positive Data Input.** **Transmit Negative Data Input.**
39	P1	RCLK0	DO	**Receive Clock Output.**
40 41	P2 P3	RPOS0 RNEG0	DO DO	**Receive Positive Data.** **Receive Negative Data.**
42	K4	ALOS0	DO	**Analog Loss of Signal Output.**
43	K2	GND	S	**Ground.** This pin must be connected to Ground.
44	N4, P4	TVCC0	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT381 Pin Description (Continued)

Pin # LQFP	Pin # PBGA	Symbol	I/O[1]	Description
45 46	N5 P5	TTIP0 TRING0	AO AO	**Transmit Tip Output.** **Transmit Ring Output.** These pins are differential line driver outputs designed to drive 75 Ω unbalanced or 120 Ω balanced cables with a 1:2 transformer and two 11 Ω series resistors. TRING and TTIP will be in high impedance state if the TCLK pin is Low.
47	N6, P6	TGND0	S	**Transmit Driver Ground.** Ground pin for the output driver.
48 49	P7 N7	RTIP0 RRING0	AI AI	**Receive TIP Input.** **Receive Ring Input.** These pins are the inputs to the differential line receiver. Data is recovered and output on the RPOS/RNEG pins.
50	L6, M6	TGND1	S	**Transmit Driver Ground.**
51 52	M5 L5	TRING1 TTIP1	AO AO	**Transmit Ring Output.** **Transmit Tip Output.**
53	L4, M4	TVCC1	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
54 55	L7 M7	RRING1 RTIP1	AI AI	**Receive Ring Input.** **Receive Tip Input.**
56	L11, M11	TVCC2	S	**Transmit Driver Power Supply.**
57 58	L10 M10	TTIP2 TRING2	AO AO	**Transmit Tip Output.** **Transmit Ring Output.**
59	L9, M9	TGND2	S	**Transmit Driver Ground.**
60 61	M8 L8	RTIP2 RRING2	AI AI	**Receive TIP Input.** **Receive Ring Input.**
62	N9, P9	TGND3	S	**Transmit Driver Ground.** Ground pin for the output driver.
63 64	P10 N10	TRING3 TTIP3	AO AO	**Transmit Ring.** **Transmit Tip Output.**
65	N11, P11	TVCC3	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
66 67	N8 P8	RRING3 RTIP3	AI AI	**Receive Ring Input.** **Receive Tip Input.**
68	K11	ALOS3	DO	**Analog Loss of Signal Output.**
69 70	P12 P13	RNEG3 RPOS3	DO DO	**Receive Negative Data Output.** **Receive Positive Data Output.**
71	P14	RCLK3	DO	**Receive Clock Output.**
72 73	N12 N13	TNEG3 TPOS3	DI DI	**Transmit Negative Data Input.** **Transmit Positive Data Input.**
74	N14	TCLK3	DI	**Transmit Clock Input.**
75	K12	ALOS2	DO	**Analog Loss of Signal Output.**
76 77	M12 M13	RNEG2 RPOS2	DO DO	**Receive Negative Data Output.** **Receive Positive Data Output.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT381 Pin Description (Continued)

Pin # LQFP	Pin # PBGA	Symbol	I/O[1]	Description
78	M14	RCLK2	DO	**Receive Clock Output.**
79	L12	TNEG2	DI	**Transmit Negative Data Input.**
80	L13	TPOS2	DI	**Transmit Positive Data Input.**
81	L14	TCLK2	DI	**Transmit Clock Input.**
82	K13	NC	NC	**Not Connected.** This pin must be left open for normal operation.
83	K14	NC	NC	**Not Connected.** This pin must be left open for normal operation.
84	J11	GND	S	**Ground.** This pin must be connected to Ground.
85	J12	GND	S	**Ground.** This pin must be connected to Ground.
86	J13	GND	S	**Ground.** This pin must be connected to Ground.
87	J14	GND	S	**Ground.** This pin must be connected to Ground.
88	H12	GND	S	**Ground.** This pin must be connected to Ground.
89	H11	GND1	S	**Ground (Core).**
90	H14	VCC1	S	**Power (Core).**
91	G11	GNDIO1	S	**Ground (I/O).**
92	G14	VCCIO1	S	**Power (I/O).**
93	G13	AT2	AO	**JTAG Analog Output Test Port 2.**
94	H13	AT1	AI	**JTAG Analog Input Test Port 1.**
95	G12	$\overline{\text{TRST}}$	DI	**JTAG Controller Reset Input.** Input is used to reset JTAG controller. $\overline{\text{TRST}}$ is pulled up internally and may be left disconnected.
96	F11	TMS	DI	**JTAG Test Mode Select Input.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.
97	F14	TCK	DI	**JTAG Clock Input.** Clock input for JTAG. Connect to GND when not used.
98	F13	TDO	DO	**JTAG Data Output.** Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. Updated on falling edge of TCK.
99	F12	TDI	DI	**JTAG Data Input.** Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.
100	D14	TCLK5	DI	**Transmit Clock Input.**
101	D13	TPOS5	DI	**Transmit Positive Data Input.**
102	D12	TNEG5	DI	**Transmit Negative Data Input.**
103	C14	RCLK5	DO	**Receive Clock Output.**
104	C13	RPOS5	DO	**Receive Positive Data Output.**
105	C12	RNEG5	DO	**Receive Negative Data Output.**
106	E12	ALOS5	DO	**Analog Loss of Signal Output.**
107	B14	TCLK4	DI	**Transmit Clock Input.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT381 Pin Description (Continued)

Pin # LQFP	Pin # PBGA	Symbol	I/O[1]	Description
108	B13	TPOS4	DI	**Transmit Positive Data Input.**
109	B12	TNEG4	DI	**Transmit Negative Data Input.**
110	A14	RCLK4	DO	**Receive Clock Output.**
111	A13	RPOS4	DO	**Receive Positive Data Output.**
112	A12	RNEG4	DO	**Receive Negative Data Output.**
113	E11	ALOS4	DO	**Analog Loss of Signal Output.**
114	E14	OE	DI	**Output Driver Enable Input.** If this pin is asserted Low all analog driver outputs immediately enter a high impedance mode to support redundancy applications without external mechanical relays. All other internal circuitry stays active.
115	E13	RPOL	DI	**Receive Polarity Select Input.** Determines RPOS/RNEG polarity. RPOS/RNEG are active High output polarity when RPOL is High and active Low polarity when RPOL is Low.
116	A11, B11	TVCC4	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
117	B10	TTIP4	AO	**Transmit Tip Output.**
118	A10	TRING4	AO	**Transmit Ring Output.**
119	A9, B9	TGND4	S	**Transmit Driver Ground.** Ground pin for the output driver.
120	A8	RTIP4	AI	**Receive Tip Input.**
121	B8	RRING4	AI	**Receive Ring Input.**
122	C9, D9	TGND5	S	**Transmit Driver Ground.** Ground pin for the output driver.
123	C10	TRING5	AO	**Transmit Ring Output.**
124	D10	TTIP5	AO	**Transmit Tip Output.**
125	C11, D11	TVCC5	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
126	D8	RRING5	AI	**Receive Ring Input.**
127	C8	RTIP5	AI	**Receive Tip Input.**
128	C4, D4	TVCC6	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
129	D5	TTIP6	AO	**Transmit Tip Output.**
130	C5	TRING6	AO	**Transmit Ring Output.**
131	C6, D6	TGND6	S	**Transmit Driver Ground.** Ground pin for the output driver.
132	D7	RRING6	AI	**Receive Ring Input.**
133	C7	RTIP6	AI	**Receive Tip Input.**
134	A6, B6	TGND7	S	**Transmit Driver Ground.** Ground pins for the output driver.
135	B5	TTIP7	AO	**Transmit Tip Output.**
136	A5	TRING7	AO	**Transmit Ring Output.**
137	A4, B4	TVCC7	S	**Transmit Driver Power Supply.** Power supply pin for the output driver.
138	B7	RRING7	AI	**Receive Ring Input.**
139	A7	RTIP7	AI	**Receive Tip Input.**
140	E4	ALOS7	DO	**Analog Loss of Signal Output.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

Table 1. LXT381 Pin Description (Continued)

Pin # LQFP	Pin # PBGA	Symbol	I/O[1]	Description
141	A3	RNEG7	DO	**Receive Negative Data Output.**
142	A2	RPOS7	DO	**Receive Positive Data Output.**
143	A1	RCLK7	DO	**Receive Clock Output.**
144	B3	TNEG7	DI	**Transmit Negative Data Input.**

1. DI: Digital Input; DO: Digital Output; DI/O: Digital Bidirectional Port; AI: Analog Input; AO: Analog Output S: Power Supply; N.C.: Not Connected.

2.0 Functional Description

The LXT381 is a fully integrated octal line interface unit designed for G.703 2.048 Mbps applications. Each transceiver front end interfaces with four lines, one pair for transmit, one pair for receive. These two lines comprise a digital data loop for full duplex transmission. The LXT381 is designed to operate as an analog front-end (line driver and data recovery) without any reference clock.

2.1 Receiver

The eight receivers in the LXT381 are identical. The following paragraphs describe the operation of a single receiver.

The receive signal is input to the LIU via a 1:1 transformer. See Figure 5. A peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers to ensure optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 12dB of attenuation (from 2.37 V nominal), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, the peak detectors are held above a minimum level of 150 mV to provide immunity from impulsive noise. After processing through the data slicers, the received signal is routed to the data ports and to the receive monitor.

Recovered data is output at RPOS and RNEG. RPOS/RNEG polarity is determined by the RPOL pin. In addition, RPOS and RNEG are internally connected to an EXOR that is fed to the RCLK output for external clock recovery applications.

The receivers in the LXT381 can be powered down using the $\overline{\text{RPD}}$ pin. In this case, the receiver outputs RCLK/RPOS/RNEG will be in a high impedance state.

2.1.1 Loss Of Signal Detector

The LXT381 includes an analog LOS detector (ALOS pins) compliant with ITU-G.775 recommendation. The LXT381 monitors the incoming signal amplitude. Any signal below 200mV for more than 30µs (typ) will assert the corresponding ALOS pin. The LOS condition is cleared when the signal amplitude rises above 250mV. The LXT381 requires more than 10 and less than 255 bit periods to declare a LOS condition in accordance to ITU G.775.

During the LOS condition, the receiver outputs (RPOS and RNEG) will be held high.

2.2 Transmitter

The eight low power transmitters of the LXT381 are identical.

The LXT381 transmitters can work either with NRZ or RZ formatted signals, depending on the TCLK state. See Table 2. When TCLK is active, NRZ data applied to TPOS/TNEG is clocked serially into the device. The TPOS/TNEG inputs are sampled on the falling edge of TCLK.

When TCLK is held high for at least 12 µs, TPOS and TNEG become RZ formatted inputs. In this mode, TPOS and TNEG control the pulse width and polarity on TTIP and TRING.

If TCLK is held Low, the output drivers enter a low power, high impedance mode. The OE pin can also be used to set all the output drivers to an high impedance mode. This feature is useful for redundancy/protection applications.

Each output driver is supplied by a separate power supply (TVCC and TGND).

2.2.1 Transmit Pulse Shaping

In NRZ mode, the transmitted pulse shape is internally generated using a high speed D/A converter. Shaped pulses are further applied to the line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance regardless of whether it is driving marks, spaces or if it is in transition. This well controlled dynamic impedance provides excellent return loss when used with external precision resistors (± 1% accuracy) in series with the transformer. See Figure 5.

The LXT381 produces 2.048 MHz pulses for both 75 Ω coaxial (2.37 V) or 120 Ω shielded twisted-pair (3.0 V) lines through an output transformer with a 1:2 step up pulse transformer and 11 Ω series resistors. No transmit component changes are required in 75 or 120 Ω operation as the output driver dynamically adjusts its output pulse amplitude.

2.3 Interfacing with 5V logic

The LXT381 can interface with 5V logic. In this case, the VCCIO pins should be connected to a 5V power supply. The VCCIO pins feed the digital I/O pads making the input/output voltage levels consistent with 5V logic. See Table 10. The internal logic will still operate from the 3.3V supply (VCC0 and VCC1) to minimize the power consumption.

2.4 Line Protection

In the receive side, the 1 kΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (70 kΩ typ.) the resistors do not affect the receiver sensitivity. In the transmit side, the Schottky diodes D1-D4 protect the output driver.While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

2.5 Loopbacks

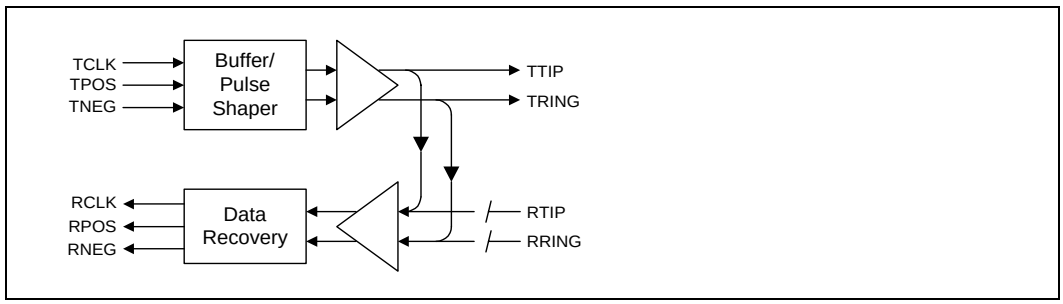
The LXT381 offers two loopback modes for diagnostic purposes. The loopback mode is selected with the LOOPn pins.

2.5.1 Analog Loopback

When selected, the transmitter outputs (TTIP & TRING) are connected internally to the receiver inputs (RTIP & RRING) as shown in Figure 3. Data and clock are output at RCLK, RPOS & RNEG pins for the corresponding transceiver. Note: Signals on the RTIP & RRING pins are ignored during analog loopback.

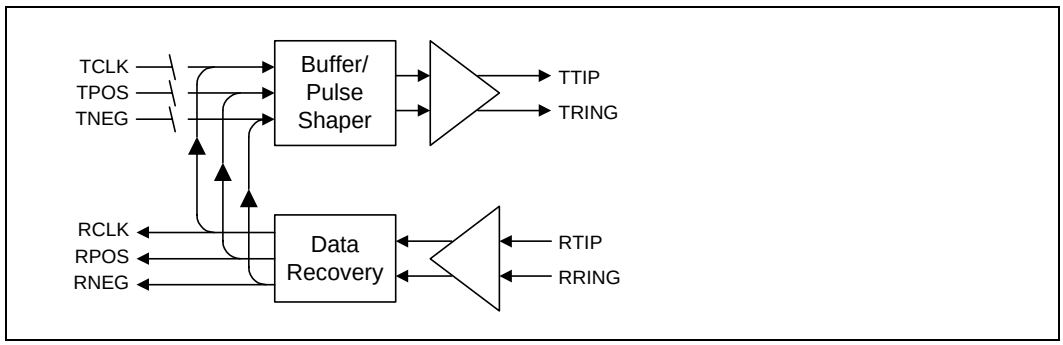
2.5.2 Remote Loopback

Figure 3. Analog Loopback



During remote loopback, the RCLK, RPOS & RNEG outputs routed to the transmit circuits and output on the TTIP & TRING pins. Signals on the TCLK, TPOS & TNEG pins are ignored during remote loopback. See Figure 4. Note: because in a remote loopback, the RPOS/RNEG outputs determine the transmitter pulse width, the G.703 pulse template may not be met in this test mode.

Figure 4. Remote Looback



2.6 Hitless Protection Switching (HPS)

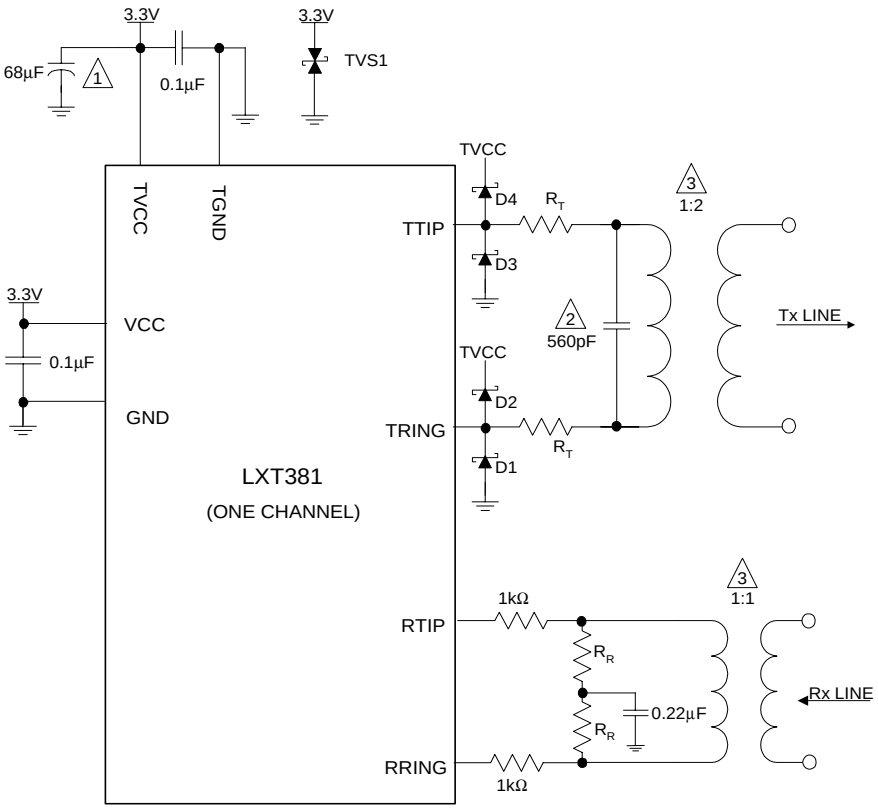
The LXT386 transceivers include an output driver tristatability feature for T1/E1 redundancy applications. This feature greatly reduces the cost of implementing redundancy protection by eliminating external relays. Please refer to Application Note 119 for guidelines for implementing redundancy systems for both T1 and E1 operation using the LXT380/1/4/6.

Table 2. Operation Mode Summary

RPD	TCLK	Receive Mode	Transmit Mode
L	Clocked	Power Down	NRZ
L	L	Power Down	Power Down[1]
L	H	Power Down	RZ
H	Clocked	Data Recovery	NRZ
H	L	Data Recovery	Power down[1]
H	H	Data Recovery	RZ

1. In Remote loopback the driver will not power down.

Figure 5. External Transmit/Receive Line Circuitry



COMPONENT	APPLICATION	
	75Ω COAX	120Ω TWISTED PAIR
R_T	11 Ω ±1%	11 Ω ±1%
R_R	37.5 Ω ±1%	60 Ω ±1%
D1 - D4	INTERNATIONAL RECTIFIER 11DQ04 or 10BQ060 MOTOROLA MBR0540T1	
TVS1	SGS-THOMSON SMLVT 3V3 3.3V	

1 Common decoupling capacitor for all TVCC and TGND pins.

2 Typical value. Adjust for actual board parasitics to obtain optimum return loss.

3 Transformer turns ratio tolerance is ± 2%. See Test Specifications Section for transformer specifications.

3.0 JTAG Boundary Scan

3.1 Overview

The LXT381 supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

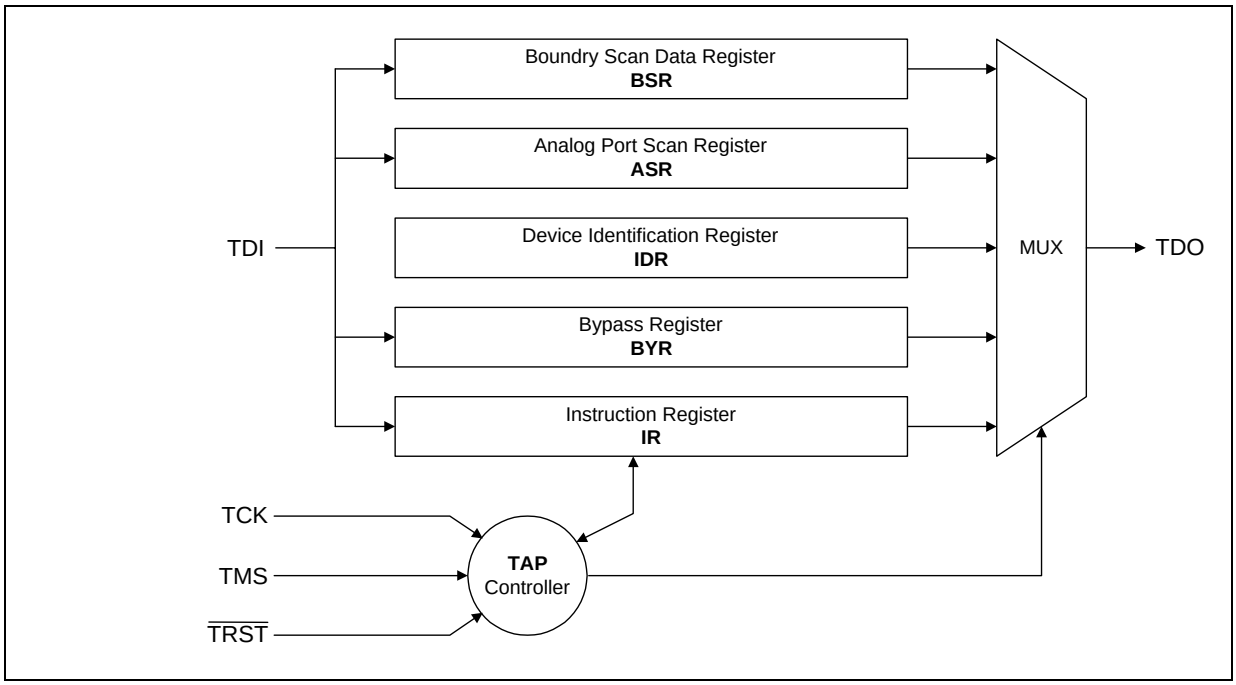
In addition to the traditional IEE1149.1 digital boundary scan capabilities, the LXT381 also includes analog test port capabilities. This feature provides access to the TIP and RING signals in each channel (transmit and receive.) This way, the signal path integrity across the primary winding of each coupling transformer can be tested.

3.2 Architecture

Figure 6 represents the LXT381 basic JTAG architecture.

The LXT381 JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

Figure 6. LXT381 JTAG Architecture



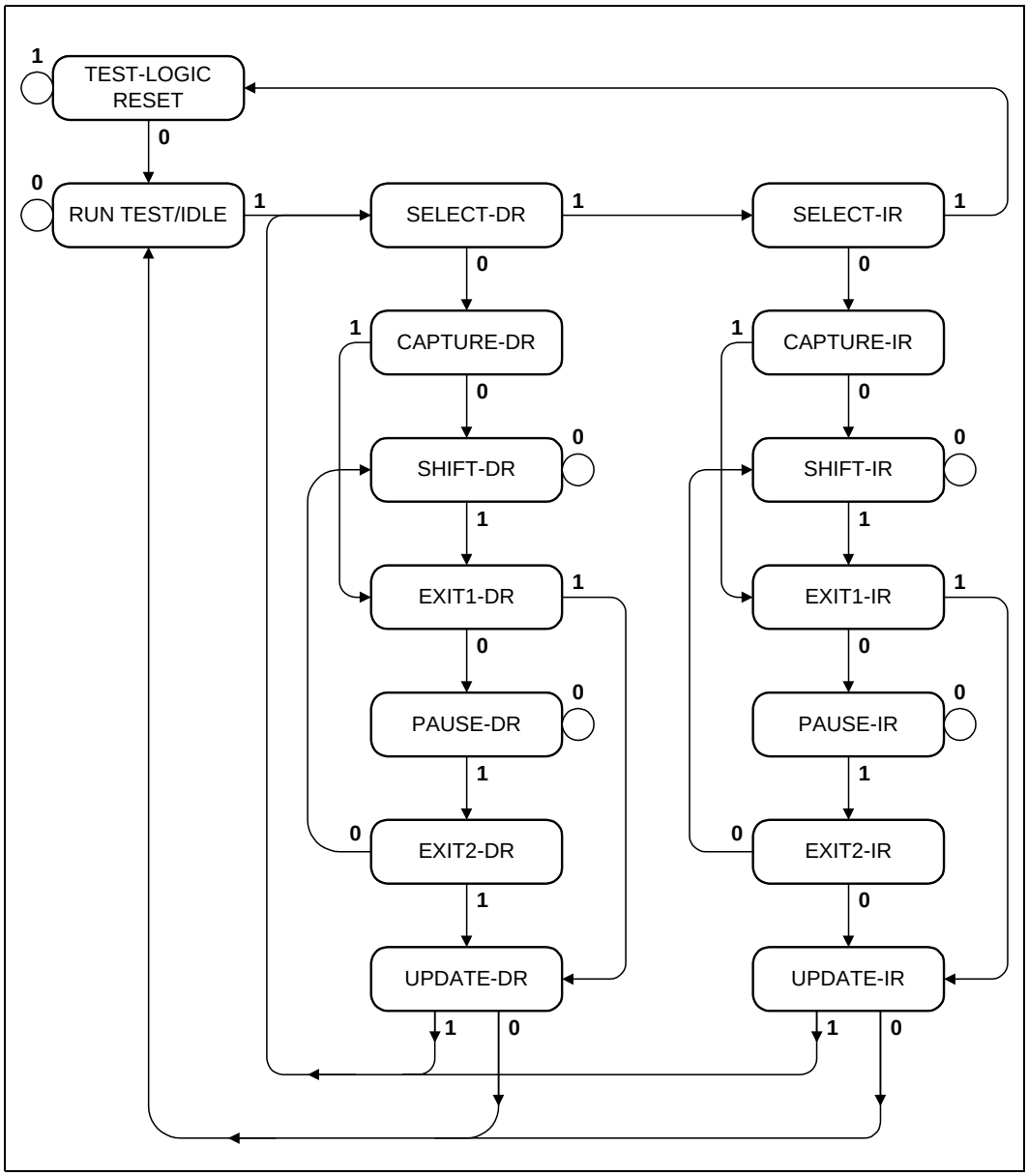
3.2.1 TAP Controller

The TAP controller is a 16 state synchronous state machine controlled by the TMS input and clocked by TCK. See Figure 7. The TAP controls whether the LXT381 is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 3 describes in detail each of the states represented in Figure 7.

Table 3. TAP State Description

State	Description
Test logic reset	In this state the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -test/idle	The TAP controller stays in this state as long as TMS is low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift - DR	Shifts the selected test data registers by one stage toward its serial output.
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

Figure 7. JTAG State Diagram



3.3 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 6.

3.3.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristatable pins require more than one position in the register. Table 4 shows the BSR scan cells and their functions. Data into the BSR is shifted in LSB first

Table 4. Boundary Scan Register (BSR)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
0	LOOP0	I/O	PDO0	
1	LOOP0	I/O	PADD0	
2	LOOP1	I/O	PDO1	
3	LOOP1	I/O	PADI1	
4	LOOP2	I/O	PDO2	
5	LOOP2	I/O	PADI2	
6	LOOP3	I/O	PDO3	
7	LOOP3	I/O	PADI3	
8	LOOP4	I/O	PDO4	
9	LOOP4	I/O	PADI4	
10	LOOP5	I/O	PDO5	
11	LOOP5	I/O	PADI5	
12	LOOP6	I/O	PDO6	
13	LOOP6	I/O	PADI6	
14	LOOP7	I/O	PDO7	
15	LOOP7	I/O	PADI7	
16	N/A	-	PDOEN	PDOEN controls the LOOP0 through LOOP7 pins. Setting PDOEN to “1” configures the pins as outputs. The output value to the pin is set in PDO[0..7]. Setting PDOEN to “0” tristates all the pins. The input value to the pins can be read in PADD[0.7].
17	TCLK1	I	TCLK1	
18	TPOS1	I	TPOS1	
19	TNEG1	I	TNEG1	
20	RCLK1	O	RCLK1	
21	RPOS1	O	RPOS1	
22	RNEG1	O	RNEG1	
23	N/A	-	HIZB1	HIZB1 controls the RPOS1, RNEG1 and RCLK1 pins. Setting HIZB1 to “1” enables output on the pins. Setting HIZB1 to “0” tristates the pins.
24	LOS1	O	LOS1	
25	TCLK0	I	TCLK0	
26	TPOS0	I	TPOS0	
27	TNEG0	I	TNEG0	

Table 4. Boundary Scan Register (BSR) (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
28	RCLK0	O	RCLK0	
29	RPOS0	O	RPOS0	
30	RNEG0	O	RNEG0	
31	N/A	-	HIZB0	HIZB0 controls the RPOS0, RNEG0 and RCLK0 pins. Setting HIZB0 to “1” enables output on the pins. Setting HIZB0 to “0” tristates the pins.
32	LOS0	O	LOS0	
33	-	-	RESERVED1	
34	LOS3	O	LOS3	
35	RNEG3	O	RNEG3	
36	RPOS3	O	RPOS3	
37	N/A	-	HIZB3	HIZB3 controls the RPOS3, RNEG3 and RCLK3 pins. Setting HIZB3 to “1” enables output on the pins. Setting HIZB3 to “0” tristates the pins.
38	RCLK3	O	RCLK3	
39	TNEG3	I	TNEG3	
40	TPOS3	I	TPOS3	
41	TCLK3	I	TCLK3	
42	LOS2	O	LOS2	
43	RNEG2	O	RNEG2	
44	RPOS2	O	RPOS2	
45	N/A	-	HIZB2	HIZB2 controls the RPOS2, RNEG2 and RCLK2 pins. Setting HIZB2 to “1” enables output on the pins. Setting HIZB2 to “0” tristates the pins.
46	RCLK2	O	RCLK2	
47	TNEG2	I	TNEG2	
48	TPOS2	I	TPOS2	
49	TCLK2	I	TCLK2	
50	-	-	RESERVED2	
51	-	-	RESERVED3	
52	-	-	RESERVED4	
53	-	-	RESERVED5	
54	-	-	RESERVED6	
55	-	-	RESERVED7	
56	-	-	RESERVED8	
57	-	-	RESERVED9	
58	TCLK5	I	TCLK5	
59	TPOS5	I	TPOS5	
60	TNEG5	I	TNEG5	
61	RCLK5	O	RCLK5	
62	RPOS5	O	RPOS5	

Table 4. Boundary Scan Register (BSR) (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
63	RNEG5	O	RNEG5	
64	N/A	-	HIZB5	HIZB5 controls the RPOS5, RNEG5 and RCLK5 pins. Setting HIZB5 to “1” enables output on the pins. Setting HIZB5 to “0” tristates the pins.
65	LOS5	O	LOS5	
66	TCLK4	I	TCLK4	
67	TPOS4	I	TPOS4	
68	TNEG4	I	TNEG4	
69	RCLK4	O	RCLK4	
70	RPOS4	O	RPOS4	
71	RNEG4	O	RNEG4	
72	N/A	-	HIZB4	HIZB4 controls the RPOS4, RNEG4 and RCLK4 pins. Setting HIZB4 to “1” enables output on the pins. Setting HIZB4 to “0” tristates the pins.
73	LOS4	O	LOS4	
74	OE	I	OE	
75	RPOL	I	RPOL	
76	LOS7	O	LOS7	
77	RNEG7	O	RNEG7	
78	RPOS7	O	RPOS7	
79	N/A	-	HIZB7	HIZB7 controls the RPOS7, RNEG7 and RCLK7 pins. Setting HIZB7 to “1” enables output on the pins. Setting HIZB7 to “0” tristates the pins.
80	RCLK7	O	RCLK7	
81	TNEG7	I	TNEG7	
82	TPOS7	I	TPOS7	
83	TCLK7	I	TCLK7	
84	LOS6	O	LOS6	
85	RNEG6	O	RNEG6	
86	RPOS6	O	RPOS6	
87	N/A	-	HIZB6	HIZB6 controls the RPOS6, RNEG6 and RCLK6 pins. Setting HIZB6 to “1” enables output on the pins. Setting HIZB6 to “0” tristates the pins.
88	RCLK6	O	RCLK6	
89	TNEG6	I	TNEG6	
90	TPOS6	I	TPOS6	
91	TCLK6	I	TCLK6	
92	-	-	RESERVED10	
93	-	-	RESERVED11	
94	-	-	RESERVED12	
95	-	-	RESERVED13	

Table 4. Boundary Scan Register (BSR) (Continued)

Bit #	Pin Signal	I/O Type	Bit Symbol	Comments
96	-	-	RESERVED14	
97	-	-	RESERVED15	
98	-	-	RESERVED16	

3.3.2 Device Identification Register (IDR)

The IDR register provides access to the manufacturer number, part number and the LXT381 revision. The register is arranged per IEEE 1149.1 and is represented in Table 5. Data into the IDR is shifted in LSB first

Table 5. Device Identification Register (IDR)

Bit #	Comments
31 - 28	Revision Number
27 - 12	Part Number
11 - 1	Manufacturer Number
0	Set to ‘1’

3.3.3 Bypass Register (BYR)

The Bypass Register is a 1 bit register that allows direct connection between the TDI input and the TDO output.

3.3.4 Analog Port Scan Register (ASR)

The ASR is a 5 bit shift register used to control the analog test port at pins AT1, AT2. When the INTEST_ANALOG instruction is selected, TDI connects to the ASR input and TDO connects to the ASR output. After 5 TCK rising edges, a 5 bit control code is loaded into the ASR. Data into the ASR is shifted in LSB first.

Table 6 shows the 16 possible control codes and the corresponding operation on the analog port. The Analog Test Port can be used to verify continuity across the coupling transformers primary winding

Table 6. Analog Port Scan Register (ASR)

ASR Control Code	AT1 Forces Voltage To:	AT2 Senses Voltage From:
11111	TTIP0	TRING0
11110	TTIP1	TRING1
11101	TTIP2	TRING2
11100	TTIP3	TRING3
11011	TTIP4	TRING4
11010	TTIP5	TRING5

Table 6. Analog Port Scan Register (ASR) (Continued)

ASR Control Code	AT1 Forces Voltage To:	AT2 Senses Voltage From:
11001	TTIP6	TRING6
11000	RTIP7	RRING7
10111	RTIP0	RRING0
10110	RTIP1	RRING1
10101	RTIP2	RRING2
10100	RTIP3	RRING3
10011	RTIP4	RRING4
10010	RTIP5	RRING5
10001	RTIP6	RRING6
10000	RTIP7	RRING7

The Analog Test Port can be used to verify continuity across the coupling transformer's primary winding. By applying a stimulus to the AT1 input, a known voltage will appear at AT2 for a given load. This, in effect, tests the continuity of a receive or transmit interface. See Figure 8.

3.3.5 Instruction Register (IR)

The IR is a 3 bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 7 shows the valid instruction codes and the corresponding instruction description.

Figure 8. Analog Test Port Application

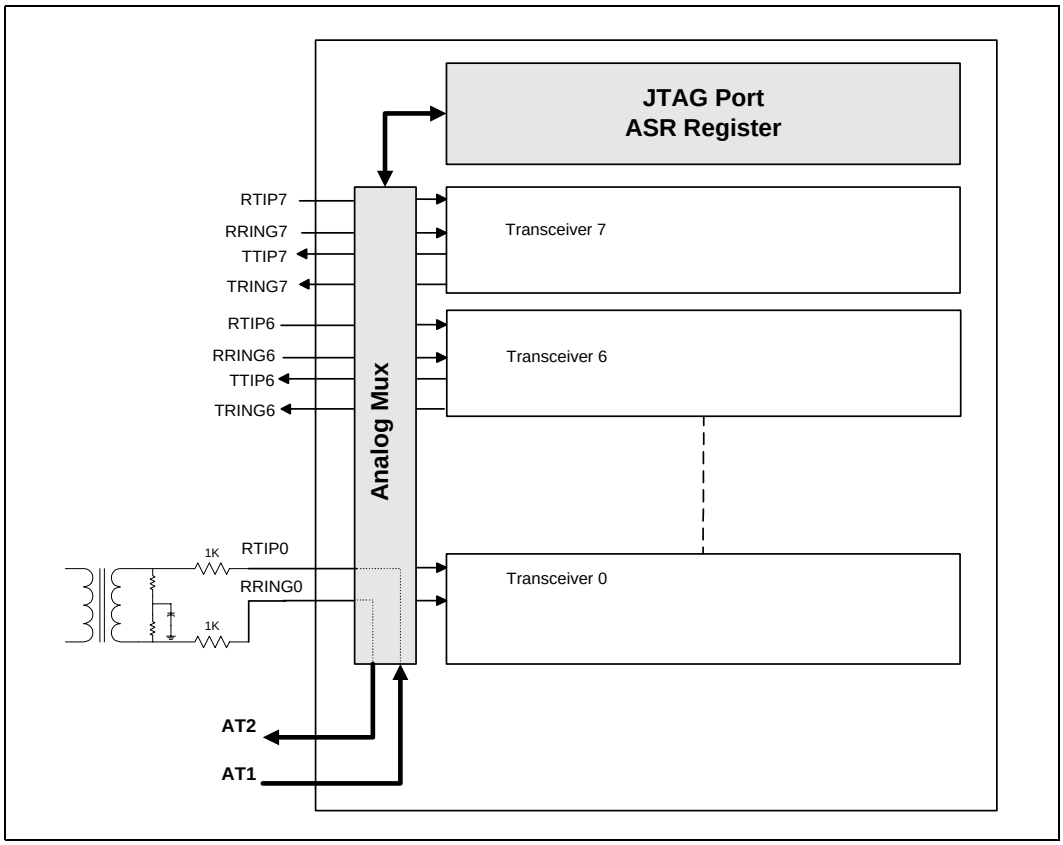


Table 7. Instruction Register (IR)

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/sensing through AT1 and AT2. Refer to Table 6.
SAMPLE / PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the LXT381 logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

4.0 Test Specifications

Note: Table 8 through Table 18 and Figure 9 through Figure 12 represent the performance specifications of the LXT381 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 10 through Table 18 are guaranteed over the recommended operating conditions specified in Table 9.

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
DC supply voltage	Vcc0, Vcc1, Tvcc 0-7	-0.5	4.0	V
DC supply voltage	Vccio0, Vccio1,	-0.5	7.0	V
Input voltage on any digital pin	Vin	GND-0.5 GND-0.5	VCCIO0 + 0.5 VCCIO1 + 0.5	V V
Input voltage on RTIP, RRING[1]	Vin	GND-0.5	VCC0 + 0.5 VCC1 + 0.5	V
ESD voltage on any Pin [2]	Vin	2000	-	V
Transient latch-up current on any pin	Iin	-	100	mA
Input current on any digital pin [3]	Iin	-10	10	mA
DC input current on TTIP, TRING [3]	Iin	-	±100	mA
DC input current on RTIP, RRING [3]	Iin	-	±100	mA
Storage temperature	Tstor	-65	+150	°C
Maximum package power dissipation	P_P		850	mW
Thermal resistance, junction to ambient, 144 pin LQFP package			28	°C/W
Thermal resistance, junction to ambient, 160 pin PBGA package			28	°C/W

Caution: Exceeding these values may cause permanent damage.

Caution: Functional operation under these conditions is not implied.

Caution: Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Referenced to ground.
2. Human body model.
3. Constant input current.

Table 9. Recommended Operating Conditions

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
DC supply voltage	Vcc	3.135	3.3	3.465	V	3.3V ± 5%
Digital I/O DC supply voltage	Vcc	3.135	3.3	5.25	V	
Ambient operating temperature	Ta	-40	25	+85	°C	

1. Current consumption over the full operating temperature and power supply voltage range.
2. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.

Table 9. Recommended Operating Conditions (Continued)

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Average transmitter power supply current [1]	75 Ω, coax cable 120 Ω, TWP cable 75 Ω, coax cable 120 Ω, TWP cable	I_{TVCC}	-	- - 125 100	265 210 - -	mA mA mA mA	100% 1's density 100% 1's density 50% 1's density 50% 1's density
Average core power supply current [1]		I_{VCC}	-	80	100	mA	
Average I/O power supply current [1, 2]		I_{VCCIO}		18	25	mA	
Output load at TTIP and TRING		Rl	40	-	-	Ω	

1. Current consumption over the full operating temperature and power supply voltage range.
2. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50pF load.

Table 10. DC Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
High level input voltage		VIH	2	-	-	V	
Low level input voltage		VIL	-	-	0.8	V	
High level output voltage[1]		VOH	2.4		VCCIO	V	IOUT= 400µA
Low level output voltage[1]		VOL	-	-	0.4	V	IOUT= 1.6mA
LOOP 0-7	Low level input voltage	VINL	–	–	1/3VCC-0.2	V	The VCC supply refers to VCCIO0 or VCCIO1 only.
	Midrange level input voltage	VINM	1/3VCC+0.2	1/2VCC	2/3VCC-0.2	V	
	High level input voltage	VINH	2/3VCC+0.2	-	-	V	
	Low level input current	IINL	–	–	50	µA	
	High level input current	IINH	–	–	50	µA	
Input leakage current		IIL	-10	–	+10	µA	
Tri state leakage current		IHZ	-10	–	+10	µA	
Tri state output current		IHZ	-	-	1	µA	TTIP, TRING
Line short circuit current		-	-	-	50	mA RMS	2 x 11 Ω series resistors and 1:2 transformer
Input leakage: TMS TDI $\overline{TRST}$		-	-	-	50	µA	

1. Output drivers will output CMOS logic levels into CMOS loads.

Table 11. Transmit Transmission Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Output pulse amplitude	75 Ω 120 Ω	-	2.14 2.7	2.37 3.0	2.60 3.3	V V	Tested at the line side
Peak voltage of a space	75 Ω 120 Ω	-	-0.237 -0.3	-	0.237 0.3	V V	
Transmit amplitude variation with supply		-	-1	-	+1	%	

1. Guaranteed by design and other correlation methods.

Table 11. Transmit Transmission Characteristics (Continued)

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Difference between pulse sequences		-	-	-	200	mV	For 17 consecutive pulses
Pulse width ratio of the positive and negative pulses		-	0.95	-	1.05	-	At the nominal half amplitude
Transmit transformer turns ratio for 75/120 Ω characteristic impedance		-	-	1:2	-	-	Rt = 11 Ω ± 1%
Transmit return loss 75 Ω coaxial [1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	-	15 15 15	17 18 17	-	dB dB dB	Using components in the LXD381 evaluation board
Transmit return loss, 120 Ω twisted pair cable [1]	51kHz to 102 kHz 102 kHz to 2.048 MHz 2.048 MHz to 3.072 MHz	-	15 15 15	18 19 18	-	dB dB dB	Using components in the LXD381 evaluation board
Transmit intrinsic jitter; 20Hz to 100kHz		-	-	0.030	0.050	U.I.	Tx path TCLK is jitter free

1. Guaranteed by design and other correlation methods.

Table 12. Receive Transmission Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Permissible cable attenuation		-	-	-	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	-	-	Vp	
Signal to noise interference margin		S/I	-15	-	-	dB	Per G.703, O.151 @ 6 dB cable attenuation
Data decision threshold		SRE	43	50	57	%	Rel. to peak input voltage
Data receiver squelch level		-	-	150	-	mV	
Loss of signal threshold		-	-	200	-	mV	
LOS hysteresis		-	-	50	-	mV	
Receiver input impedance		-	-	70	-	k Ω	@ 1.024 MHz
Input termination resistor tolerance		-	-		±1	%	
Input return loss[1]	51 kHz - 102 kHz 102 - 2048 kHz 2048kHz - 3072 kHz	-	20 20 20	-	-	dB dB dB	Measured against nominal impedance
LOS delay time		-	-	30	-	µs	
LOS reset		-	10	-	255	marks	

1. Guaranteed by design and other correlation methods.

Table 13. Analog Test Port Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
3 dB Bandwidth	at13db	-	5	-	MHz	
Input voltage range	at1iv	0	-	VCC0 VCC1	V	
Output voltage range	at2ov	0	-	VCC0 VCC1	V	

Table 14. Transmit Timing Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
Output pulse width	TW	219	244	269	ns	
Transmit clock frequency	TCLK	-	2.048	-	MHz	
Transmit clock tolerance	TCLKT	-50	-	+50	ppm	
Transmit clock duty cycle	tDC	10	-	90	%	NRZ mode
TPOS/TNEG pulse width (RZ mode)	tMPW	236	-	252	ns	RZ mode (TCLK = H for >16 clock cycles)
TPOS/TNEG to TCLK setup time	TSUT	20	-	-	ns	
TCLK to TPOS/TNEG hold time	THT	20	-	-	ns	
Delay time OE Low to driver Hi-Z	TOEZ	-	-	1	µS	
Delay time TCLK Low to driver Hi-Z	TTZ	8	-	15	µS	

Figure 9. Transmit Clock Timing

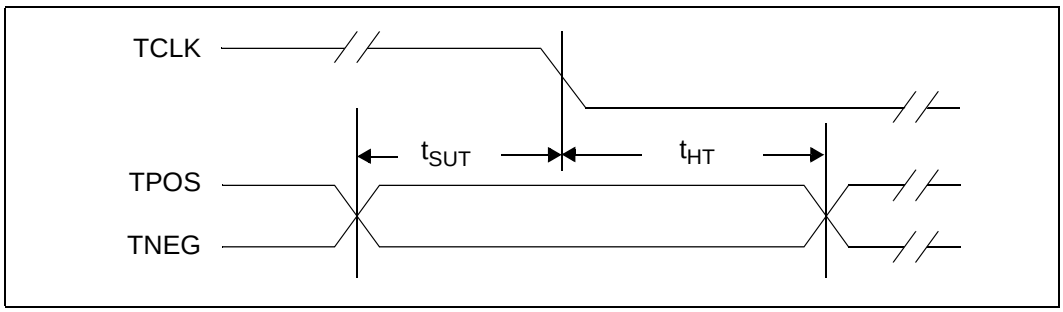


Table 15. Receive Timing Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit	Test Condition
Rise/fall time [1]	Tr	20	-	-	ns	@ CL=15 pF
RPOS/RNEG pulse width	Tpwl	200	244	300	ns	
Receiver throughput delay	Trxd	-	85	-	ns	
Delay time between RPOS/RNEG and RCLK	-	-	-	5	ns	

1. For all digital outputs.

Figure 10. Receive Timing Diagram

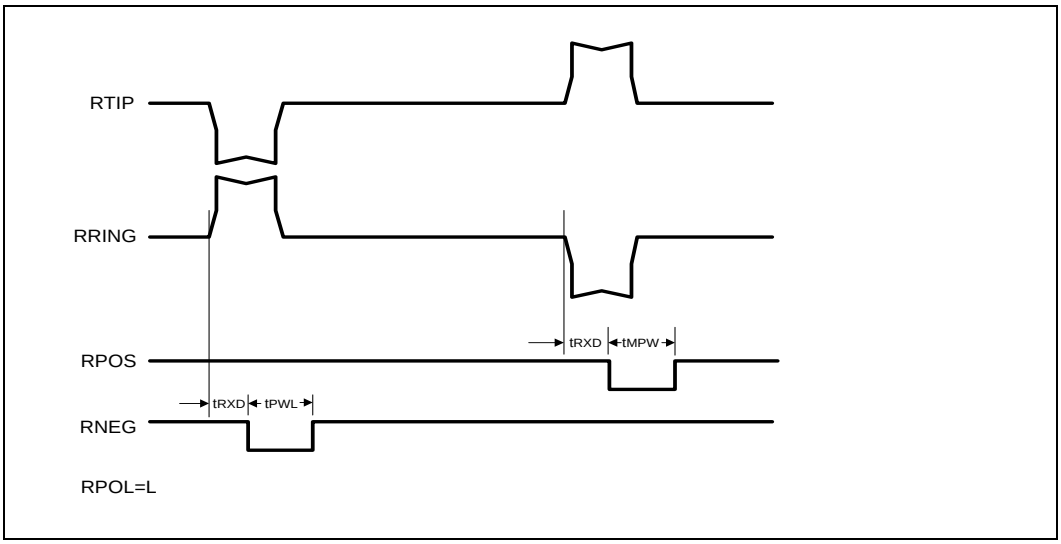


Table 16. JTAG Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Cycle time	t_{CYC}	200	-	-	ns	
J-TMS/J-TDI to J-TCK rising edge time	t_{SUT}	50	-	-	ns	
J-CLK rising to J-TMS/L-TDI hold time	t_{HT}	50	-	-	ns	
J-TCLK falling to J-TDO valid	t_{DOD}	-	-	50	ns	

Figure 11. JTAG Timing

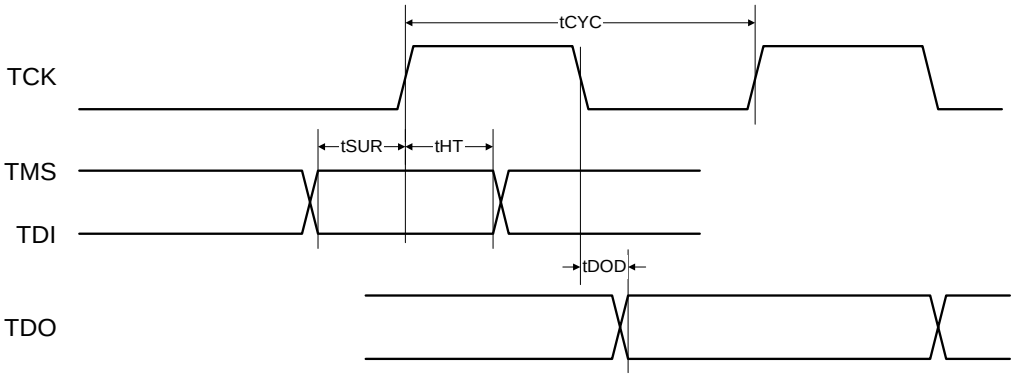


Table 17. Transformer Specifications

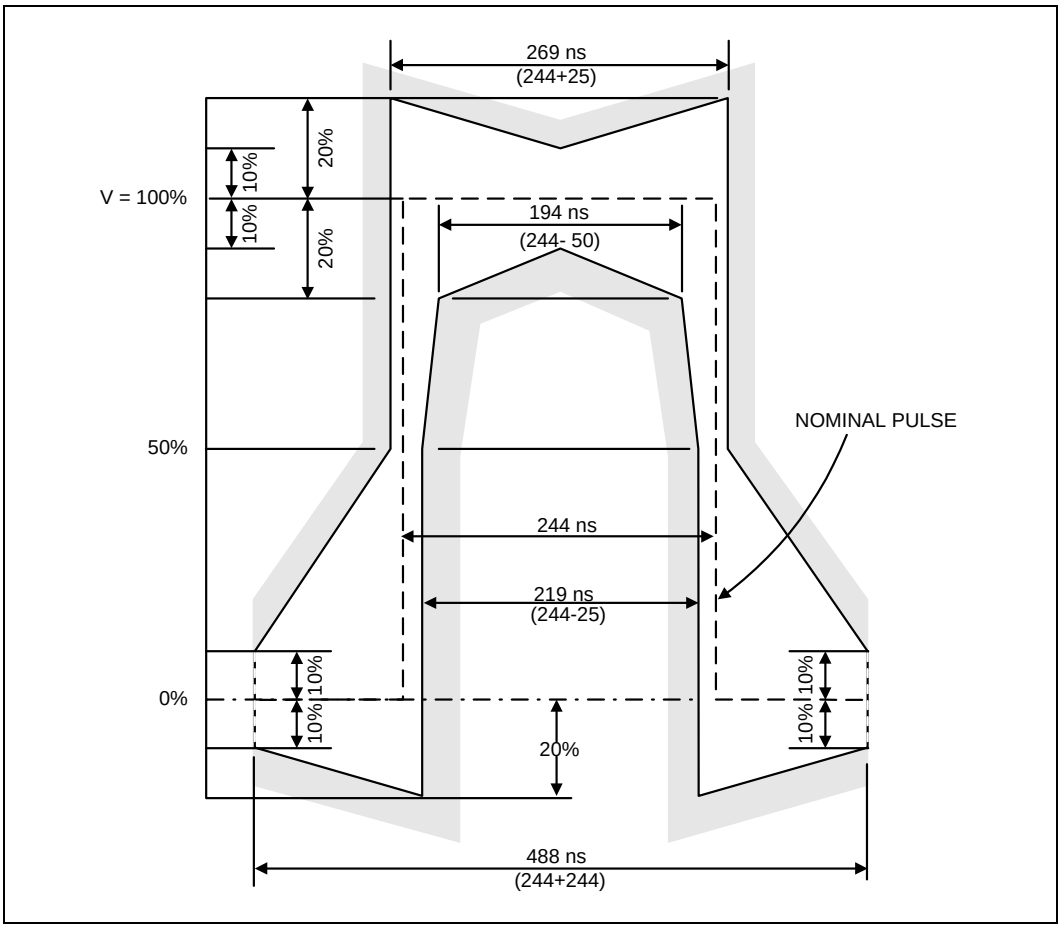
Tx/Rx	Turns Ratio	Primary Inductance mH (min.)	Leakage Inductance µH (max.)	Interwinding Capacitance pF (max.)	DCR Ω (max.)	Dielectric Breakdown Voltage V[1] (min.)
TX	1:2	1.2	0.60	60	0.70 pri 1.20 sec	1500 Vrms
RX	1:1	1.2	0.60	60	1.10 pri 1.10 sec	1500 Vrms

1. This parameter is application dependent.

Table 18. G.703 2.048 Mbit/s Pulse Mask Specifications

Parameter	Cable		Unit
	TWP	Coax	
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 12. E1 Mask Templates

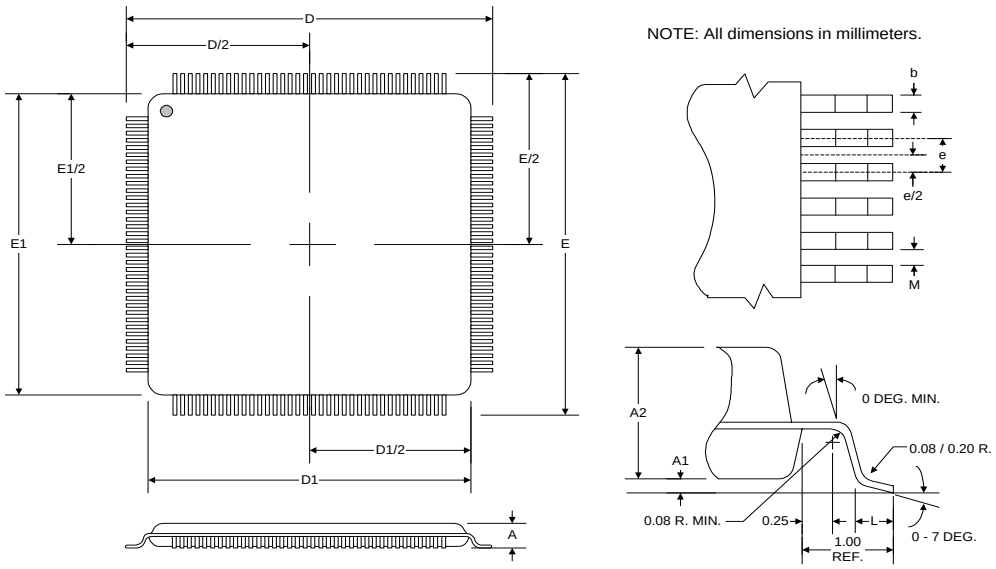


5.0 Mechanical Specifications

Figure 13. LXT381 144 Pin LQFP Package Dimensions

144-Pin Low-Profile Quad Flat Package

- Part Number LXT381LE
- Extended Temperature Range (-40 °C to 85



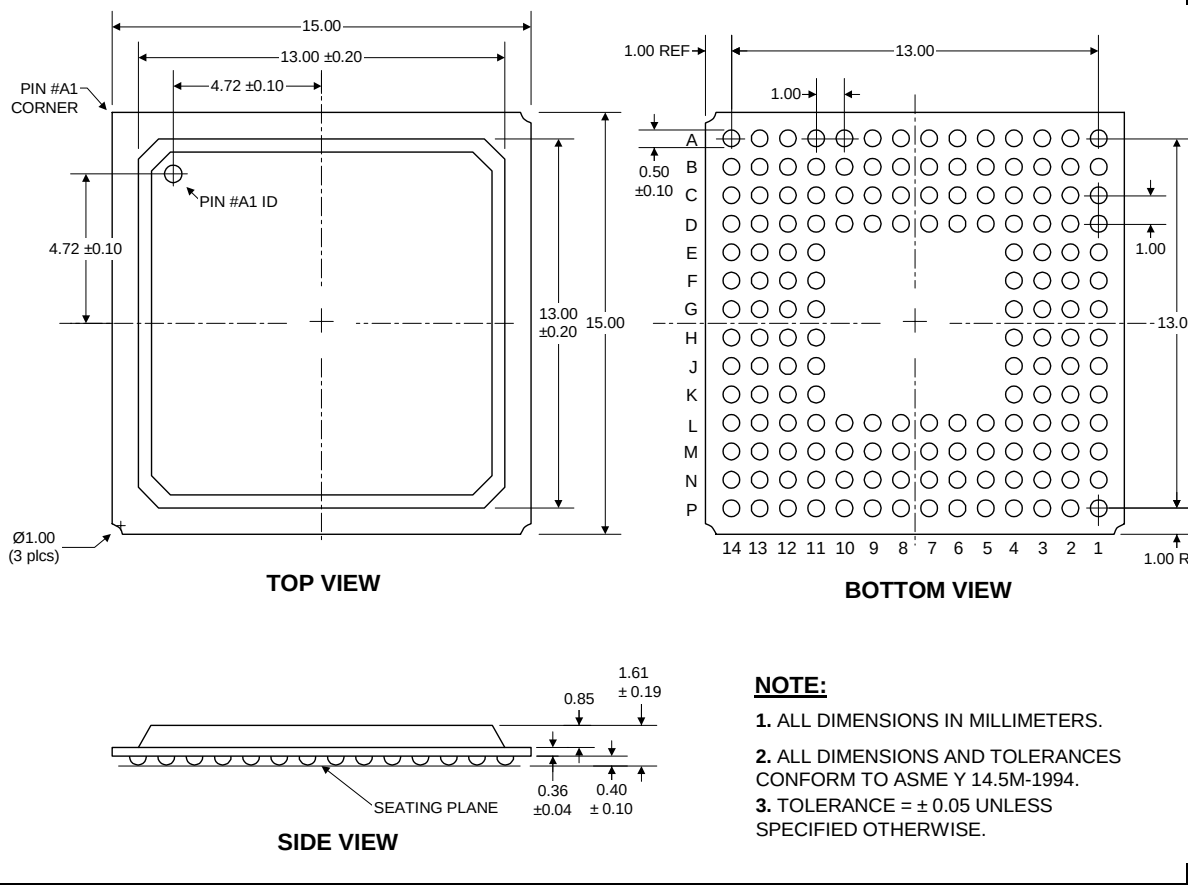
Dimension[1]	Millimeters		
	Minimum	Nominal	Maximum
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		22.00 B.S.C.	
D1		20.00 B.S.C.	
E		22.00 B.S.C.	
E1		20.00 B.S.C.	
e		0.50 B.S.C.	
L	0.45	0.60	0.75
M	0.14	-	-

1. See JEDEC Publication for additional specifications.

Figure 14. LXT381 160 Pin PBGA Package Dimensions

160-Pin Plastic Ball Grid Array

- Part Number LXT381BE
- Extended Temperature Range (-40 °C to 85 °C)



NOTE:

1. ALL DIMENSIONS IN MILLIMETERS.

2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.

3. TOLERANCE = ± 0.05 UNLESS SPECIFIED OTHERWISE.