LXT9784 Octal 10/100 Transceiver Hardware Integrity Function Overview

Application Note

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Application Note

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1.0 Connection Types

Cabling problems can be the cause of significant network downtime. With today's network manager more concerned about "Total Cost of Ownership", features that can help solve cabling problems provide valuable benefits. The Hardware Integrity (HWI) function incorporated into the LXT9784 is one such feature.

The Hardware Integrity function uses transmission line theory to measure the arrival time and electrical characteristics of the wave reflected back from an incident test wave launched on the media. With these measurements, opens, shorts, and degraded cable quality can be located along the wire, and lead the network manager to the location of the problem.

This document provides a theoretical overview of the HWI function implemented in the LXT9784.

1.1 Isolating Cabling Problems

When looking at cabling plant installation, it consists of many different pieces:

- The cable connection from the PC to the wall plate
- The wall plate
- The cables from the wall plate to the wiring closet
- The wiring closet patch panels
- The RJ45 connectors everywhere
- The patch cables to the network hub.

Hand-held CAT-5 UTP cable testers are frequently used to isolate cabling problems. A typical cable test involves connecting one end of the cable to the tester, and connecting a remote node terminator or loopback module to the other end.

Then the tester performs cable link analysis and is able to detect the following conditions:

- **Short** – when two or more lines are short-circuited together.
- **Open** – Lack of continuity between pins at both ends of the cable.
- **Crossed pair** – When a pair is connected to different pins at each end (i.e. Pair 1 is connected to pins 1&2 at one end and pins 3&6 at the other).
- **Reversed pair** – when two lines in a pair are connected to opposite pins at each end of the cable (i.e. the line on pin 1 is connected to pin 2 at the other end, the line on pin 2 is connected to pin 1), also called polarity reversal.
- **Distance** – In addition it is able to locate the distance to an open or short and to measure cable length.

The tester uses a technique called TDR (Time Domain Reflection) based on transmission line theory. This technique transmits a pulse down the cable, and measures the elapsed time until it receives a reflection from the far end of the cable.

The LXT9784 10/100 Ethernet Octal PHY device uses a similar approach. Each of the device ports has the capability to independently detect and report cabling problems via the MII management interface (MDIO) - without the need to unplug cables, connect test equipment or install a loopback

module on the far end. Each of the LXT9784 ports is able to detect cable problems such as open, short, or other anomalies and report the distance to the fault. This results in reduction of networking downtime when tracing and isolating cabling problems and ease of network maintenance.

2.0 Transmission Lines and Return Wave Theory

All transmission lines have two coexisting waves propagating through the media at the same time. The main wave is the forward wave propagating from the transmitter to the receiver. The second wave is a return wave created by an imperfect line or load and propagates from the load to the source (or transmitter).

2.1 Cable Terminations and Return Loss

A perfectly terminated line is defined as a line with no attenuation and an impedance that is equal to the source's impedance and with a load that is equal to the line impedance as well. For a perfectly terminated line the return wave is zero. In that case the load receives all the forward wave energy.

In an open line, meaning there is no load connected to its end, the return wave amplitude is equal to the forward wave amplitude. The same applies for a short circuit line.

The reflection coefficient is defined as:

$$T_L = \frac{Reflected\_wave}{Forward\_wave} = \frac{V-}{V+} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Where Z_L is the load impedance

Z_0 is the cable impedance

The return loss in (dB) is defined as:

$$RL(db) = 20\log_{10}|1/T_L| = 20\log_{10}\left|\frac{Z_L + Z_0}{Z_L - Z_0}\right|$$

Figure 1 illustrates the forward and return waves within a cable system. Table 1 describes the Return Loss as a function of Load Impedance for cable with characteristic impedance of 100Ω (typical CAT5 UTP cable impedance).

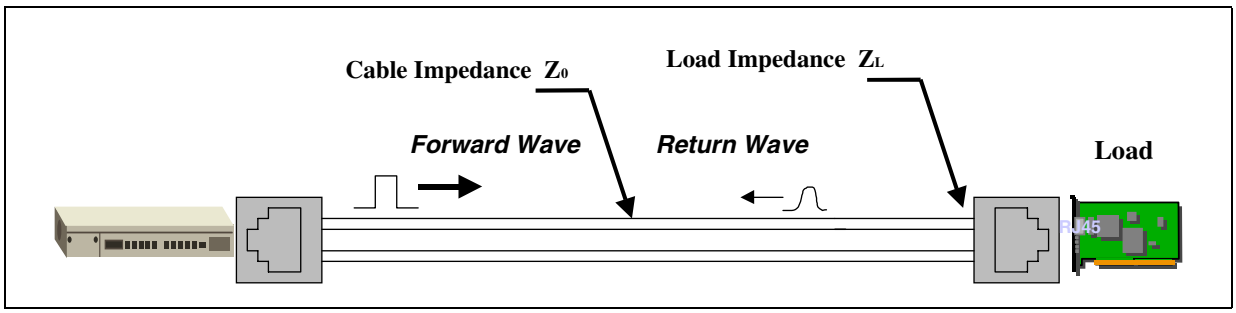
Table 1. Typical CAT5 Return Loss

Load Impedance (Ω)	Return Loss (dB)	V-/V+
∞ (open load)	0	1
300	6	0.5
192	10	0.316
138	16	0.158
100 (perfectly terminated load)	∞	0
73	16	-0.158

Table 1. Typical CAT5 Return Loss

Load Impedance (Ω)	Return Loss (dB)	V-/V+
52	10	-0.316
33.3	6	-0.5
0 (short load)	0	-1

Figure 1. Forward and Return Waves



The System return loss performance is determined by three elements:

- The transmitter return loss
- The cable characteristic impedance and return loss
- The receiver return loss

IEEE 802.3 specifies that the receiver and transmitter return loss must meet the following criteria:

Table 2. Tx and Rx Return Loss

Frequency (MHz)	I/O Minimum Return Loss (dB)
2-30	16
30-60	16 to 10 by 16-20log(f/30 MHz)
60-100	10

There are additional factors that may affect the accuracy of the return loss measurement which are:

- Connectors and patch panels
- CAT5 UTP cable impedance can vary ± 15Ω

All this means that setting a threshold of 6db return loss in a system return loss measurement should cover transmitter, receiver connector and cable impedance variances and should trigger a cable problem or anomaly indication. In other words, a good indication for a problem or an anomaly in a cable is when the return wave is equal to or greater than one-half of the incident wave.

2.2 Checking for Cable Length

Checking the distance to the cable perturbation, or cable length is done by measuring the elapsed time from transmitting a pulse down the cable, until it receives the reflection wave from the far end of it. Each type of cable transmits signals at something less than the speed of light. This propagation constant is usually provided in [nsec/m] or in decimal fraction of the speed of light.

The propagation constant for CAT5 UTP cable is typically about 4.7 nsec/m with maximum of 5.2 nsec/m.

From the elapsed time and the propagation constant of the cable, it is easy to calculate the cable length, or the distance to the cable perturbation.

2.2.1 Accuracy of Measurement

The accuracy of the cable length measurement is a function of various factors. Some of them are:

- Counter clock resolution - The LXT9784 uses a clock of 125 MHz. This yields a counting resolution of 8 nsec. This corresponds to a resolution of 1.7 meter (assuming cable propagation constant of 4.7 nsec/m) of round trip, or 0.85m of cable length.
- Cable propagation delay distribution – The cable propagation constant can vary ± 0.5 n sec/m. This variation can be compensated at final calculations if the actual cable propagation constant is known.
- Process, temperature and voltage – The implementation uses comparators. Comparator levels change with process, temperature and voltage. As the level of the returned signal is directly related to the voltage of the transmitted wave, the comparator reference level should be referenced to the same voltage.
- Constant delay in the transmitter and comparator – This delay can be calibrated out by subtracting a constant offset from the measured distance.

For a given cable with a known propagation constant, the distance to the cable perturbation is given by the following equation:

$$\mathbf{Distance} = \frac{\mathbf{N} * 8(n.Sec)}{2 * \beta(n.Sec/m)} - \mathbf{ConstantOffset}(meters)$$

Where **N** is the HWI register distance measured (bits D8:D0 of HWI MII register, see "Hardware Integrity Management Register" on page 10), and β represents the propagation constant in ns/meter (4.7 ns/meter for a typical CAT5 cable). The ***Constantoffset*** is a function of the chip and the board design and is usually on the order of less than 2 meters.

3.0 Hardware Integrity Management Register

Hardware Integrity is controlled and activated by software. There is an MII management register in each of the PHYs that is used for activating the check.

Table 3. Register 29 (1D Hex) Hardware Integrity Control Register Bit Assignments

D15	D14	D13	D12:11	D10	D9	D8:D0
HWI Enable	Ability Check	Test Exec	Reserved	lowZ	HighZ	Distance

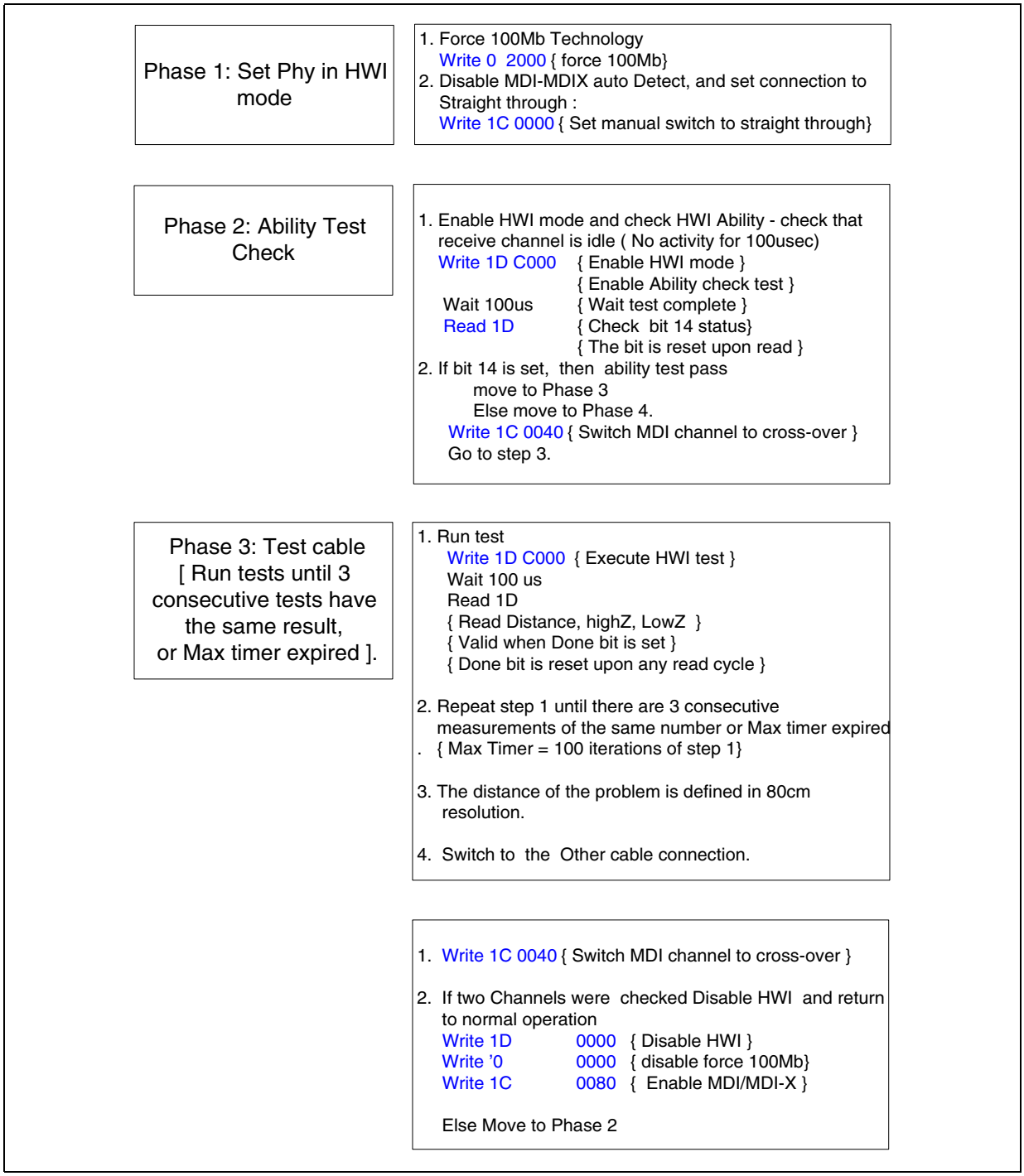
Table 4. Register 29 (1D Hex) Hardware Integrity Control Register Bit Definitions

Bit(s)	Name	Definition	Type[1]
29.15	HWI Enable	Enables the HWI feature (causing the PHY to go into HWI test mode). When set, the LXT9784 immediately starts executing the ability check. 1 = Enabled. **default 0** = Disabled.	R/W
29.14	Ability check	Results of the HWI ability check. Valid 100 µsec after HWI Enable bit was set (29.15). 1 = Test passed. 0 = Test failed (ability not detected).	RO
29.13	Test Exec	PHY launches test pulses on the wire, to determine the distance to cable High or Low impedance point. 1 = Execute test.	WO
29.12	Reserved	Constant “0”	RO
29.11	Reserved	Constant “0”	RO
29.10:9	LowZ / HighZ	Indicates type of perturbation on the line. Valid 100 µsec after Test Exec bit is set. 1 = Short (Low Z) or Open (High Z).	RO
29.8:0	Distance	Defines distance to cable perturbation, in granularity of 80 cm (35 inches). Valid 100 µsec after Test Exec bit is set.	RO

1. R/W = Read / Write
   RO = Read Only.
   WO = Write Only
   P = Affected by external pin.

4.0 Hardware Integrity Test Function

Figure 2. HWI Test Algorithm



5.0 Hardware Integrity Test Program

The following script is written in TCL, using the TCL scripting language as it was written for the Ipanema SV board

```
#Check Hardware Integrity
source "include/ipanema.tcl"
source "include/mii.tcl"
source "include/megiddo.tcl"

use $TARGETBOARD

proc Init {} {
  global PHY
  source "include/constants.tcl"

  Log [ format "Opening target board on COM%d." $COM_TB ]
   TB_Open $COM_TB

# main loop
  set end 1
  while {$end < 2} {
    set MainCommand [Input [format \
              "Insert number of PHY or Exit(x)" ] ]
    if {$MainCommand == "x" || $MainCommand == "X"} {
     incr end
     continue
     } else {
          set PHY [string tolower $MainCommand]
          InitHWI
     }
  }
#end of Init procedure
}

proc InitHWI {} {
  global  PHY PS TC

  Log "----- Starting RMII mode -----"
    TB_BrdRmii
  Log [ format "Writing 0x2100 to reg 0, PHY%d (100 Mbps; FDX)." $PHY ]
    TB_BrdWrMii 0 $PHY 0 0x2100
  set ReadVal [format "%#x" [TB_BrdRdMii 0 $PHY 0 ]]
  if { $ReadVal == 0x2100 } {
          Log [ format "Read $ReadVal from Register 0 as was written." ]
     unset ReadVal
          } else {
                Error [ format "# ERROR in reading Register 0.  Expected 0x2100 \
              and got %#x instead" $ReadVal ]
              set returnVal FAIL
                        return returnVal
              }
```

```
  Log "----- Starting HWI test -----"
  Log "Writing 0x8000 to Reg 1D(H): HWI Enable"
    TB_BrdWrMii 0 $PHY 0x1d 0x8000
    sleep 1
    set ReadVal [format "%#x" [TB_BrdRdMii 0 $PHY 0x1d]]
# check bits 14 and 15 are "1"
    if { [expr 0xc000 & $ReadVal] == 0xc000 } {
          Log [ format "Read $ReadVal from Register 1D(H) as expected" ]
      Log " "
                  } else {
                        Error [ format "# ERROR in reading Register 1D(H)" ]
                set returnVal FAIL
                        return returnVal
                  }
  Log [format "The Phy#%d" $PHY]
          for each mode {MDI MDIX} {
              Log " "
              Log "= The current mode is $mode "
              if {"$mode" == "MDI"} {
                  TB_BrdWrMii 0 $PHY 0x1c 0
              } else {
                  TB_BrdWrMii 0 $PHY 0x1c 0x0040

              }
             for {set j 1} {$j <= 5} {incr j } {

                   TakeData

                 }

   }
# end of InitHWI procedure
}

proc TakeData {} {
    global PHY

# set bit 13 & 15 - "1"
    sleep 1
    TB_BrdWrMiM 0 $PHY 0x1d 0xa000 0xa000
    sleep 1
    set res  [format "%#x" [TB_BrdRdMii 0 $PHY 0x1d]]
    set type [format "%#x" [expr $res & 0x0f00]]
    set distn [format "%d" [expr $res & 0x00ff]]
    switch -exact $type {
        0x200 {set type "High Impedance" ; set dist [expr 0.915*${distn}*8/9.4]}
        0x400 {set type "Low Impedance" ; set dist [expr 0.895*${distn}*8/9.4]}
        default {set type "100 ohm" ; set dist [expr 0.895*${distn}*8/9.4]}
     }
    Log [format "The HWI data is %#x; %s %5.2f m" $res $type $dist]
# set bit 13 - "0"
    TB_BrdWrMiM 0 $PHY 0x1d 0x0000 0x2000

}
```

```
proc HWIMain {} {

        set returnVal PASS
            # Catch all errors and close down gracefully.
            if { [ catch { set returnVal [ Init ] } errorMsg ] } {
                        Error $errorMsg
            }

            TB_Close
            return $returnVal
}

RegisterTest "Check HWI" HWIMain
```