Network Communications Group - Cable Network Operation

intel®

STEL-2040B

Data Sheet

STEL-2040B

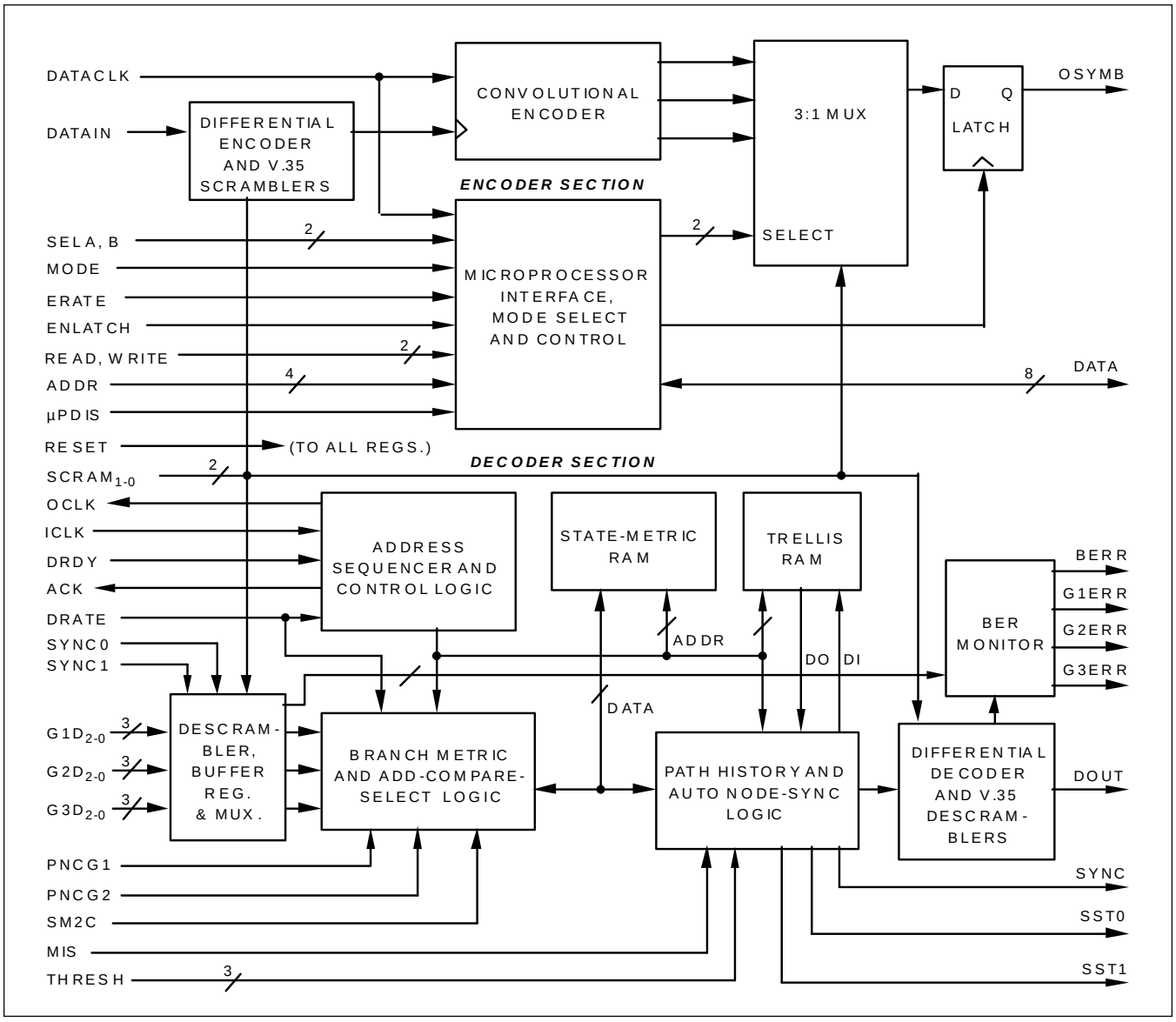
Convolutional Encoder

Viterbi Decoder

FEATURES

- Constraint Length 7
- Rates $^1/_3$, $^1/_2$, $^2/_3$* and $^3/_4$* (*Punctured)
- Built in BER Monitor
- Programmable Scrambler: V.35 (CCITT or IESS)
- Differential Encoder and Decoder
- Three Bit Soft Decision Inputs in Signed Magnitude or 2's Complement Formats
- Up to 256 Kbps Data Rate (0° to 70° C)
- Coding Gain of 5.2 dB (@ 10^{-5} BER, Rate $^1/_2$)
- Industry Standard Polynomials $G1=171_8$, $G2=133_8$, $G3=145_8$,
- Microprocessor Interface
- Low Power Consumption
- 68-pin PLCC and CLDCC Packages
- Commercial and Military Temperature Ranges Available

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

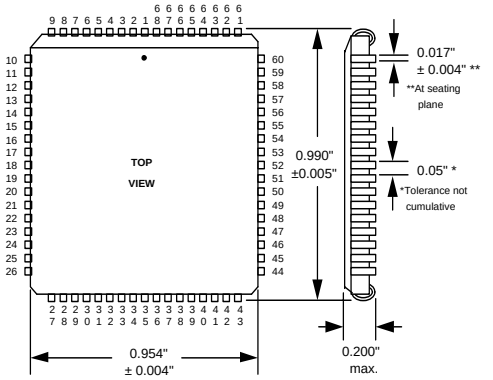
Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-2040B is a specialized product designed to perform this specific communications related function.

The encoder creates a stream of symbols which are transmitted at 2 (Rate $^1/_2$) or 3 (Rate $^1/_3$) times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link. The coding overhead can be reduced at the expense of the coding gain by puncturing (deleting) some of the symbols. The STEL-2040B is designed to operate in this way at Rate $^3/_4$. In this case 4 symbols are transmitted for every 3 bits encoded. The resulting bandwidth overhead is just 33% in this case, compared with 100% at Rate $^1/_2$.

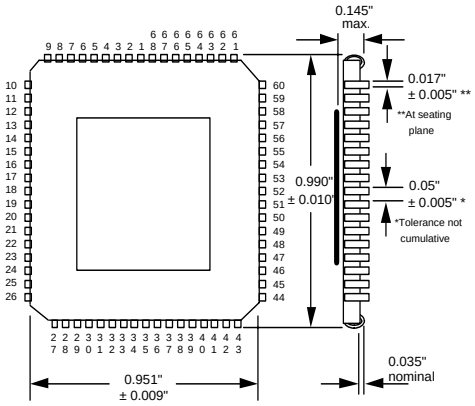
The STEL-2040B incorporates all the memories required to perform these functions. In addition, the STEL-2040B incorporates a differential encoder and decoder, two scrambling algorithms, a BER monitor and a microprocessor interface. The STEL-2040B is available in a 68-pin PLCC (plastic leaded chip carrier) and also in a ceramic leaded chip carrier (J-bend leads).

PIN CONFIGURATION

Package: 68 pin PLCC
Thermal coefficient, θ_{ja} = 36°C/W



Package: 68 pin CLDCC
Thermal coefficient, θ_{ja} = 34°C/W



Notes: (1) Tolerances on pin spacing are not cumulative.
(2) Dimensions apply at seating plane.
(3) PLCC and CLDCC packages have different corners and may not fit into sockets designed for the other type. Universal sockets are available without alignment locators.

PIN CONNECTIONS

1	SYNC	13	PNCG2	25	G2ERR	37	$DATA_6$	49	$THRESH_2$	61	ERATE
2	V_{SS}	14	$G2D_2$	26	G3ERR	38	$DATA_5$	50	MIS	62	ENLATCH
3	ACK	15	$G2D_1$	27	$ADDR_3$	39	$DATA_4$	51	V_{SS}	63	OSYMB
4	DATACLK	16	$G2D_0$	28	$ADDR_2$	40	$DATA_3$	52	RESET	64	V_{DD}
5	DRDY	17	PNCG1	29	$ADDR_1$	41	$DATA_2$	53	V_{DD}	65	ICLK
6	DATAIN	18	$G1D_2$	30	$ADDR_0$	42	$DATA_1$	54	SM2C	66	OCLK
7	MODE	19	$G1D_1$	31	V_{SS}	43	$DATA_0$	55	µPDIS	67	SCRAM1
8	SEL A	20	$G1D_0$	32	V_{SS}	44	V_{SS}	56	DOUT	68	SCRAM0
9	SEL B	21	DIFEN	33	WRITE	45	I.C.	57	SST0		
10	$G3D_2$	22	BERR	34	READ	46	DRATE	58	SYNC0		
11	$G3D_1$	23	V_{SS}	35	V_{DD}	47	$THRESH_0$	59	SST1		
12	$G3D_0$	24	G1ERR	36	$DATA_7$	48	$THRESH_1$	60	SYNC1		

Notes: 1. I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.
2. Connect all unused inputs except **READ** to V_{SS}, leave unused outputs unconnected. If the **READ** input is not used it should be connected to V_{DD}.

FUNCTION BLOCK DESCRIPTION

ENCODER

The convolutional coder is functionally independent of the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **DATA CLK**. There are two modes of operation, controlled by the **MODE** input. When **MODE** is low the timing of the **SEL A**, **SEL B** and **ENLATCH** signals determine whether 2 or 3 symbol bits are generated for every data bit. When **MODE** is high the symbols are automatically generated sequentially every clock cycle. In this case, the state of **ERATE** determines whether the device generates symbols for Rate $^1/_2$ or Rate $^1/_3$ operation. The symbols G1, G2, and G3 are generated from the modulo-2 sum (exclusive-OR) of the inputs to the 3 generators from the taps on the shift register. The 3 polynomials are 171_8 (G1), 133_8 (G2), and 145_8 (G3). Example inputs are shown in the timing diagram for both rate $^1/_2$ and rate $^1/_3$ operation.

DECODER

The STEL-2040B is designed to accept symbols either synchronously or in a handshake mode. Symbols are latched into the decoder input registers on the falling edge of the **DRDY** input. **ACK** is returned by the decoder to indicate that the symbols have been accepted.

The **RATE** input determines whether the decoder will operate in Rate $^1/_2$ or Rate $^1/_3$ mode. When operating at Rate $^1/_2$ the G3 symbol is ignored by the decoder.

For hard decision binary symbols the G1, G2, G3 symbol bits should be connected to pins $\mathbf{G1D_2}$, $\mathbf{G2D_2}$ and $\mathbf{G3D_2}$ respectively, and the other symbol input pins should be tied high (V_{DD}). Three-bit soft decision symbols may be input in Signed Magnitude or Inverted Two's Complement code, according to the setting of the code control pin, **SM2C**. The code should be set to Signed Magnitude when using hard decision data.

A single decoded data bit is output for every set of input symbols. The data bit corresponding to a particular symbol set will be output after a delay of 71 symbols. Therefore, when using the STEL-2040B to decode blocks of data 71 additional dummy symbols and 71 **DRDY** signals need to be added to the data stream to flush the last 71 decoded data bits out of the decoder.

Node synchronization (correctly grouping incoming symbols into G1, G2, and G3 sets) is inherent with many communication techniques such as TDMA and spread spectrum systems. If node synchronization is not an inherent property of the communications link then the internal auto node sync circuit can be used to do this. This is accomplished by connecting the node sync outputs (**SST0** and **SST1**) to the node sync inputs (**SYNC0** and **SYNC1**). The threshold for determining the out of sync condition is user selectable by means of the $\mathbf{THRESH_{2-0}}$ inputs. Alternatively, the **SYNC0** and **SYNC1** pins can be used with an external algorithm to achieve the same result.

Further information on the theory of operation of Viterbi decoders may be obtained from text books such as "Error-Correcting Codes", by Peterson and Weldon (MIT Press), or "Error Control Coding", by Lin and Costello (Prentice-Hall). An alternative source of information is the many papers on this subject that have appeared in the IEEE transactions, such as "Convolutional Codes and their Performance in Communication Systems", by Dr. A. J. Viterbi, IEEE Trans. on Communications Technology, October 1971.

INPUT SIGNALS

RESET

Asynchronous master **Reset**. A logic low on this pin will clear all registers on the STEL-2040B in both the encoder and decoder sections of the chip. **RESET** should remain low for at least 3 cycles of **ICLK**.

DATACLK

This is the encoder Shift Register Clock. A rising edge on this clock latches **DATAIN** into the encoder shift register. This signal should nominally be a square wave with a maximum frequency of 256 KHz.

DATAIN

This is the encoder input. The data present at this pin is latched into the encoder shift register on the rising edge of **DATACLK**. This signal should be stable at the rising edge of **DATACLK**.

MODE

The state of the **MODE** input determines the method of symbol sequencing in the encoder. When **MODE** is set low the sequencing is generated externally under the control of the **SEL A** and **SEL B** inputs, and when **MODE** is set high it is generated automatically.

SEL A, SEL B

When **MODE** is set low **SEL A** and **SEL B** select the encoded symbol, G1, G2 or G3, which will appear on the **OSYMB** pin on the next rising edge of **ENLATCH** according to the table:

SEL A	SEL B	SYMBOL	POLYNOMIAL
0	1	G1	171_8 (1111001_2)
1	0	G2	133_8 (1011011_2)
0	0	G3	145_8 (1100101_2)

When **MODE** is set high the symbol sequence is generated automatically and the **SEL A** and **SEL B** inputs are inactive.

ERATE

When **MODE** is high the **E**ncoder **Rate** input determines whether symbols for Rate $^1/_2$ (**ERATE**=1) or Rate $^1/_3$ (**ERATE**=0) operation are generated. When **MODE** is low this input is inactive.

DIFEN

When the **DIFEN** input is set high the differential encoder and decoder in the STEL-2040B are enabled. Differential encoding is done after V.35 scrambling (when used) but before Invert G2 scrambling (when used) in the encoder. The sequence is reversed in the decoder. Note that the BER monitor function will only operate correctly when **DIFEN** is set low.

SCRAM0, SCRAM1

The **Scram**ble inputs are used to enable the two scrambler functions included in the STEL-2040B, as shown in the table below:

SCRAM0	SCRAM1	FUNCTION
0	0	Scrambler disabled
0	1	V.35 (CCITT compatible)
1	1	V.35 (IESS compatible)

Two different "V.35" scrambler formats are provided since there are two versions of this standard in exixtence: the true CCITT version of the standard, and the IESS version, which has become a de facto standard through widespread use. In each case, the scrambling function is provided at the encoder and the descrambler is provided at the decoder.

ENLATCH

This is the **en**coder Output **Latch** Enable. The new symbol is clocked into the output latch and appears on the **OSYMB** pin on the rising edge of **ENLATCH**. When **MODE** is low the symbol selected will depend on the states of the **SEL A** and **SEL B** lines, which should be stable on the rising edge of **ENLATCH**. When **MODE** is high the symbol selection is internal, and the frequency of the **ENLATCH** signal should be 2 or 3 times the frequency of the **DATACLK**, depending on the rate selected.

ICLK, OCLK

System Clock. A crystal may be connected between **ICLK** and **OCLK** or a CMOS level clock may be fed into **ICLK** only. The clock frequency should be at least 70 times the data rate but no more than 18 MHz.

DRATE

The **D**ecoder **Rate** input selects whether the decoder will read two symbols (**DRATE** set high) or three symbols (**DRATE** set low)) for every data bit decoded. During Rate $^1/_2$ operation the symbol G3 on inputs $\mathbf{G3D_{2\text{-}0}}$ is completely ignored by the decoder. **DRATE** should be set high for Rate $^3/_4$ operation.

$G1D_{2\text{-}0}$, $G2D_{2\text{-}0}$, $G3D_{2\text{-}0}$

The three 3-bit soft decision symbols are connected to these inputs and loaded into the input registers on the falling edge of **DRDY**. The order in which the symbols are entered into the decoder from the registers depends on the state of the **SYNC0** and **SYNC1** inputs. The decoder can make use of soft decision information, which includes both polarity information and a confidence measure, to improve the decoder performance. If hard decision (single bit) symbols are used the signals are connected to pins $\mathbf{G1D_2}$, $\mathbf{G2D_2}$ and $\mathbf{G3D_2}$ and the other inputs are connected to V_{DD}. See **SM2C** for a description of the input data codes.

SM2C

The state of the **S**igned **M**agnitude/**2**'s **C**omplement input determines the format of the incoming soft-decision symbols into the decoder. When SM2C is high the input code is Signed Magnitude, and when it is low the code is Two's Complement. The codes are shown in the following table:

CODE CONTROL:	SM2C=1	SM2C=0
SYMBOL INPUT:	GXD2-GXD0	GXD2-GXD0
Most Confident '+' level	0 1 1	0 1 1
Data = 0	0 1 0	0 1 0
	0 0 1	0 0 1
Least Confident '+' level	0 0 0	0 0 0
Least Confident '–' level	1 0 0	1 1 1
Data = 1	1 0 1	1 1 0
	1 1 0	1 0 1
Most Confident '–' level	1 1 1	1 0 0

SM2C should be set high when using hard decision data.

DRDY

The **D**ata **R**ea**dy** signal is used to load symbols into the decoder. A new set of symbols is latched into the input registers on each falling edge of the **DRDY** input.

SYNC0, SYNC1

The Symbol **Sync0** and Symbol **Sync1** inputs are used for auto node sync operation. When using the internal auto node sync mode these two pins are connected to **SST0** and **SST1**, respectively. The operation of the decoder is affected as shownin the following table:

			Symbol entered into decoder during symbol period N		
DRATE	**SYNC0**	**SYNC1**	**G1**	**G2**	**G3**
1	0	0	$G1_N$	$G2_N$	–
1	1	0	$G2_{N-1}$	$G1_N$	–
1	0	1	$\overline{G2_N}$	$G1_N$	–
1	1	1	Invalid state		
0	0	0	$G1_N$	$G2_N$	$G3_N$
0	1	0	$G3_{N-1}$	$G1_N$	$G2_N$
0	0	1	$G2_{N-1}$	$G3_{N-1}$	$G1_N$
0	1	1	Invalid state		

Note that whenever the states of the **SYNC0** and **SYNC1** inputs are changed there will be a delay of 71 bit periods before valid data starts appearing at **DOUT**.

$THRESH_{2-0}$

A counter is used to determine the number of either traceback mismatches or metric renormalizations per 256 bits in the auto node-sync circuit, and the threshold at which the counter triggers the **SST0** and **SST1** outputs to change states is set with the data on the **$THRESH_{2-0}$** inputs. The threshold values will be as shown in the following table.

$THRESH_{2-0}$	Threshold value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Since the actual error rate obtained will depend on the signal to noise ratio (E_b/N_0) in the signal, the optimum value of the threshold will also depend on E_b/N_0 and should be set accordingly. The actual mismatch or renomalization count is stored in and can be read from the register at address E_H.

MIS

Two algorithms for auto node-sync are incorporated into the STEL-2040B. When **MIS** is set high the Traceback **Mis**match algorithm is selected, and when it is set low the Metric Renormalization algorithm is selected.

PNCG1, PNCG2

The **PNCG1** and **PNCG2** signals are used to control the STEL-2040B when operating in punctured mode. In normal (Rate=$^1/_2$) operation these pins should be set low. In punctured mode the **PNCG1** signal must be set high to indicate that the G1 symbol is punctured and the **PNCG2** signal must be set high to indicate that the G2 symbol is punctured. A symbol will be punctured when the **PNCG1** or **PNCG2** signals are high during the falling edge of **DRDY**. Zero value metrics will be substituted internally for the actual metrics corresponding to the signals present on the **$G1_{2-0}$** or **$G2_{2-0}$** pins at that time.

OUTPUT SIGNALS

OSYMB

Output Symbol from the Encoder. This output depends on the seven most recent data bits (**DATAIN**) clocked into the encoder shift register and on the select lines **SEL A** and **SEL B**. The individual symbols are formed by the modulo-2 sum of the inputs to the generators from the 7-bit shift register.

ACK

A low level pulse on the **Ack**nowledge pin indicates that the decoder has input the current set of two or three symbols. The signal will pulse low between 68 and 69 clock cycles after the falling edge of **DRDY**.

DOUT

Decoded **D**ata **Out**. The signal is latched into the output register on the falling edge of **DRDY**. There is a delay of 71 data bits from the time a set of symbols is input to the time the corresponding data bit is output. Consequently, in order to flush the last 71 bits of data out of the system at the end of a burst it is necessary to continue pulsing the **DRDY** line for 71 symbol periods after the last valid symbol has been entered.

SST0, SST1

The **S**ync **St**ate **0** and **S**ync **St**ate **1** signals are the outputs of the internal auto node sync circuit. They should be connected to **SYNC0** and **SYNC1** respectively to use the internal auto node sync capability. They may also be used in conjunction with an external node sync algorithm implementation which can use the **SST0** and **SST1** outputs.

SYNC

The **Sync** output provides an indication of the status of the internal auto node sync circuit. When it is high it indicates that node sync has been lost, and when it is low it indicates that the system is assumed to be in sync, as determined by the error rate estimate.

G1ERR, G2ERR and G3ERR

The **G1 Err**or, **G2 Err**or and **G3 Err**or outputs indicates that an error has been detected in the G1, G2 or G3 symbols, respectively, corresponding to the current output bit. These outputs will only be valid when operating at Rates $^1/_2$ and $^1/_3$ with **DIFEN** = 0.

BERR

The **B**it **Err**or output indicates that an error has been detected in any of the symbols corresponding to the current output bit. This function is the logical OR of **G1ERR**, **G2ERR**, and (at Rate $^1/_3$) **G3ERR**. This output will only be valid when operating at Rates $^1/_2$ and $^1/_3$ with **DIFEN** = 0.

MICROPROCESSOR INTERFACE

µPDIS

The microprocessor interface is selected by setting the **µPDis**able input low. All I/O and control functions are then accessed via the **$DATA_{7-0}$** bus with the associated control signals. The STEL-2040B is then used as a memory or I/O mapped peripheral to the host processor. The **RESET** input must be set high, but all other inputs will be ignored and the outputs will be invalid. When this input is set high the microprocessor interface is disabled and all I/O and control functions are accessed via the corresponding pins.

$DATA_{7-0}$

When using the STEL-2040B in the microprocessor interface mode (**µPDIS**=0) all data I/O and control is done via this bus.

$ADDR_{3-0}$

The 4-bit address bus is used to access the various I/O functions in the microprocessor interface mode, as shown in the table below.

WRITE

The **Write** input is used to write data to the microprocessor data bus. Data will be latched into the STEL-2040B on the rising edge of this signal.

READ

The **Read** input is used to read data from the microprocessor data bus; the **$DATA_{7-0}$** bus will be active in the output mode whenever this input is low.

MICROPROCESSOR INTERFACE MEMORY MAP

$ADDR_{3-0}$	**$DATA_7$**	**$DATA_6$**	**$DATA_5$**	**$DATA_4$**	**$DATA_3$**	**$DATA_2$**	**$DATA_1$**	**$DATA_0$**
0	PNCG1	G1D2	G1D1	G1D0	PNCG2	G2D2	G2D1	G2D0
1						G3D2	G3D1	G3D0
2	DRATE	SM2C	SCRAM1	SCRAM0	MIS	$THRESH_2$	$THRESH_1$	$THRESH_0$
3							SYNC1	SYNC0
4								DATAIN
5				DIFEN	MODE	SEL A	SEL B	ERATE
6								RESET
7								DRDY
8								DATACLK
9								ENLATCH
A				BERR*	G3ERR*	G2ERR*	G1ERR*	DOUT*
B				RNORM*	MSMCH*	SST1*	SST0*	SYNC*
C								OSYMB*
D								
E	$COUNT_7$*	$COUNT_6$*	$COUNT_5$*	$COUNT_4$*	$COUNT_3$*	$COUNT_2$*	$COUNT_1$*	$COUNT_0$*

* Indicates a read only function.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

***Warning**: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.*

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD}+0.3	volts
I_i	DC input current	±10	mA

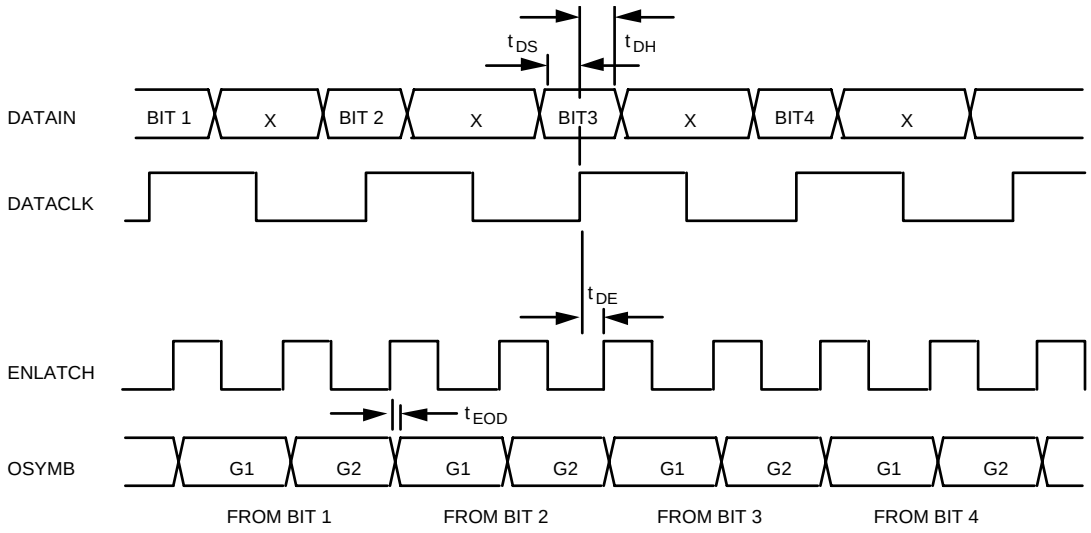
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5% +5 ± 10%	Volts (Commercial grade) Volts (Military grade)
T_a	Operating Temperature (Ambient)	0 to +70 –55 to +125	℃ (Commercial grade) ℃ (Military grade)

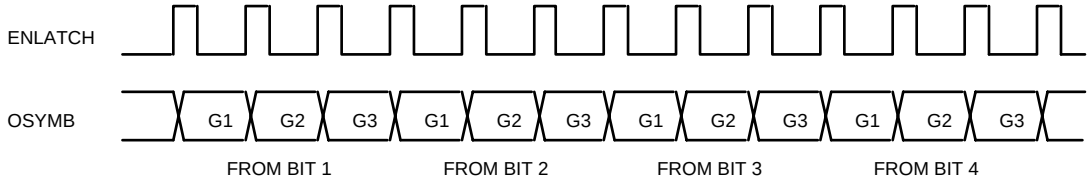
D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS}=0 V, T_a = 0° to 70° C, Commercial
V_{DD} = 5.0 V ±10%, V_{SS}=0 V, T_a =–55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**DRDY**, V_{IN} = V_{DD}
$I_{IL(max)}$	Low Level Input Current	–130	–45	–15	µA	All other inputs, V_{IN} = V_{SS}
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –6.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +6.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	V_{OUT} = V_{DD}, V_{DD} = max
		–10	–45	–130	mA	V_{OUT} = V_{SS}, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

ENCODER TIMING. MODE=1



RATE $^1/_3$ OPERATION



ENCODER ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS

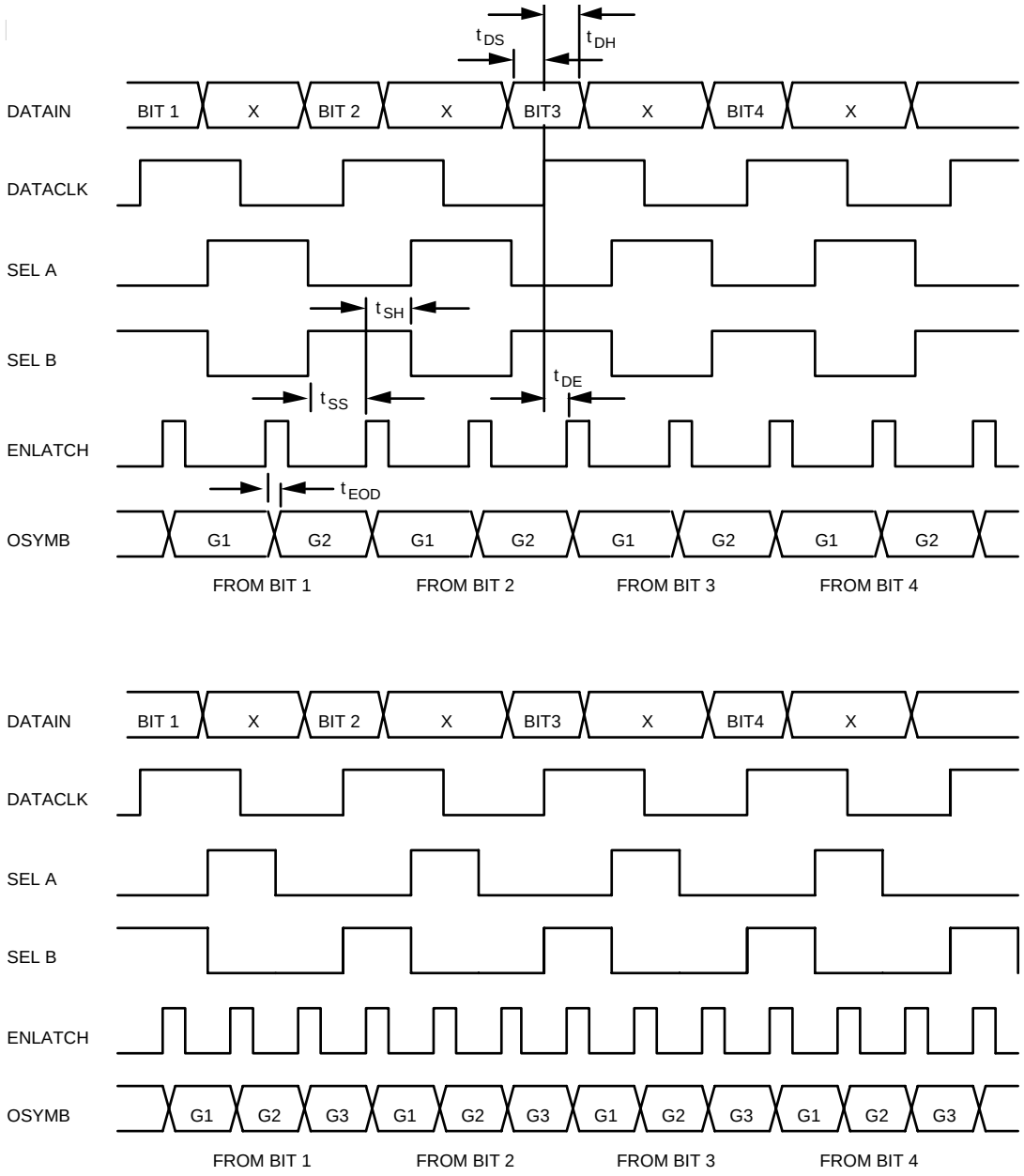
(Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{SR}	**RESET** pulse width	$3*t_{CLK}$		$3*t_{CLK}$		nsec.
t_{SR}	**RESET** to **ICLK** setup	2		3		nsec.
t_{DS}	**DATAIN** to **DATACLK** setup	10		12		nsec.
t_{DH}	**DATAIN** to **DATACLK** hold	10		12		nsec.
t_{SS}	**SEL A** or **SEL B** to **ENLATCH** setup	10		12		nsec.
t_{SH}	**SEL A** or **SEL B** to **ENLATCH** hold	5		8		nsec.
t_{DE}	**DATACLK** to **ENLATCH** delay	10		12		nsec.
t_{EOD}	**ENLATCH** to **OSYMB** stable delay		10		12	nsec.

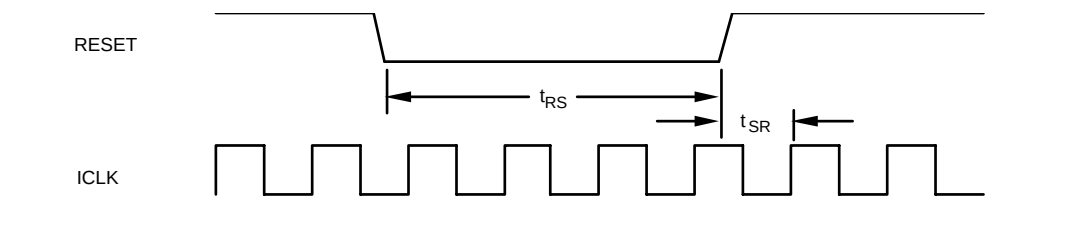
Notes: t_{CLK} = Period of **ICLK** =(1/ f_{CLK}).

t_{SR} is only relevant if operation is to commence during the first clock cycle after **RESET** goes high.

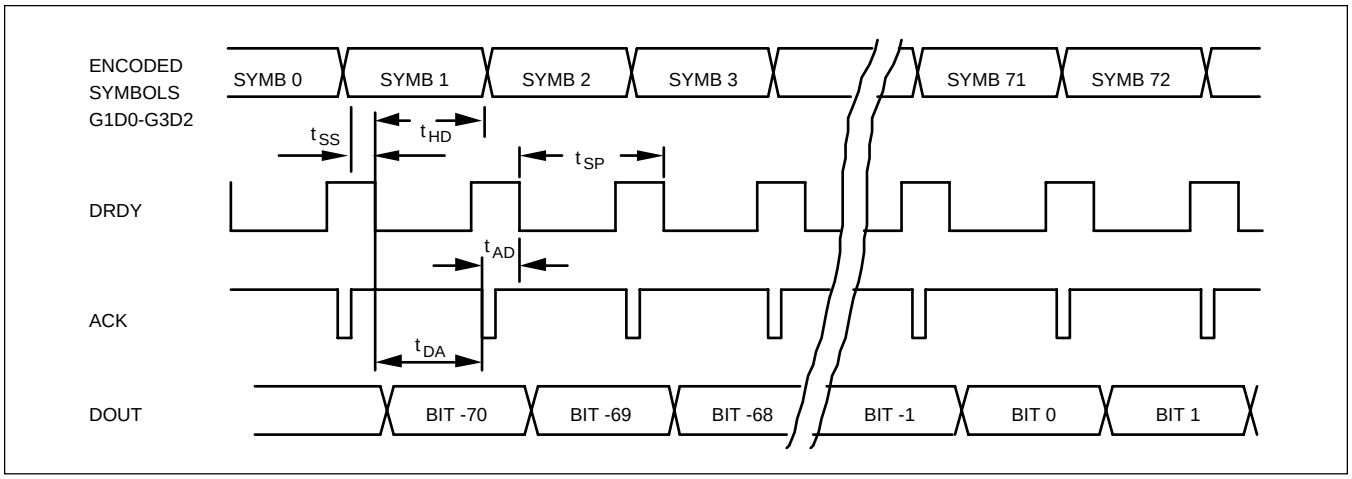
ENCODER TIMING. MODE=0 (STEL-5268 EMULATION MODE)

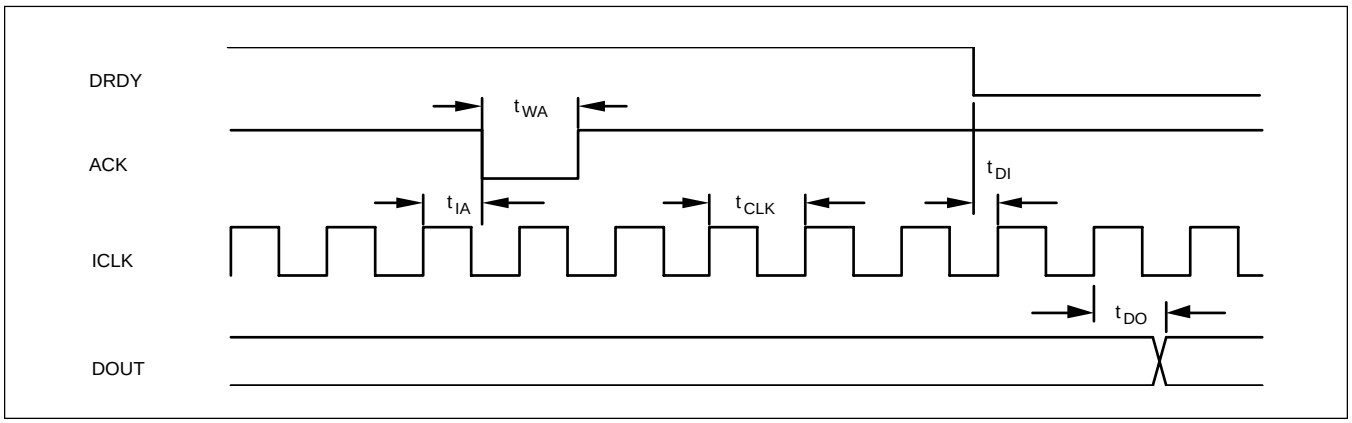


RESET TIMING



DECODER TIMING





DECODER ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS

(Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

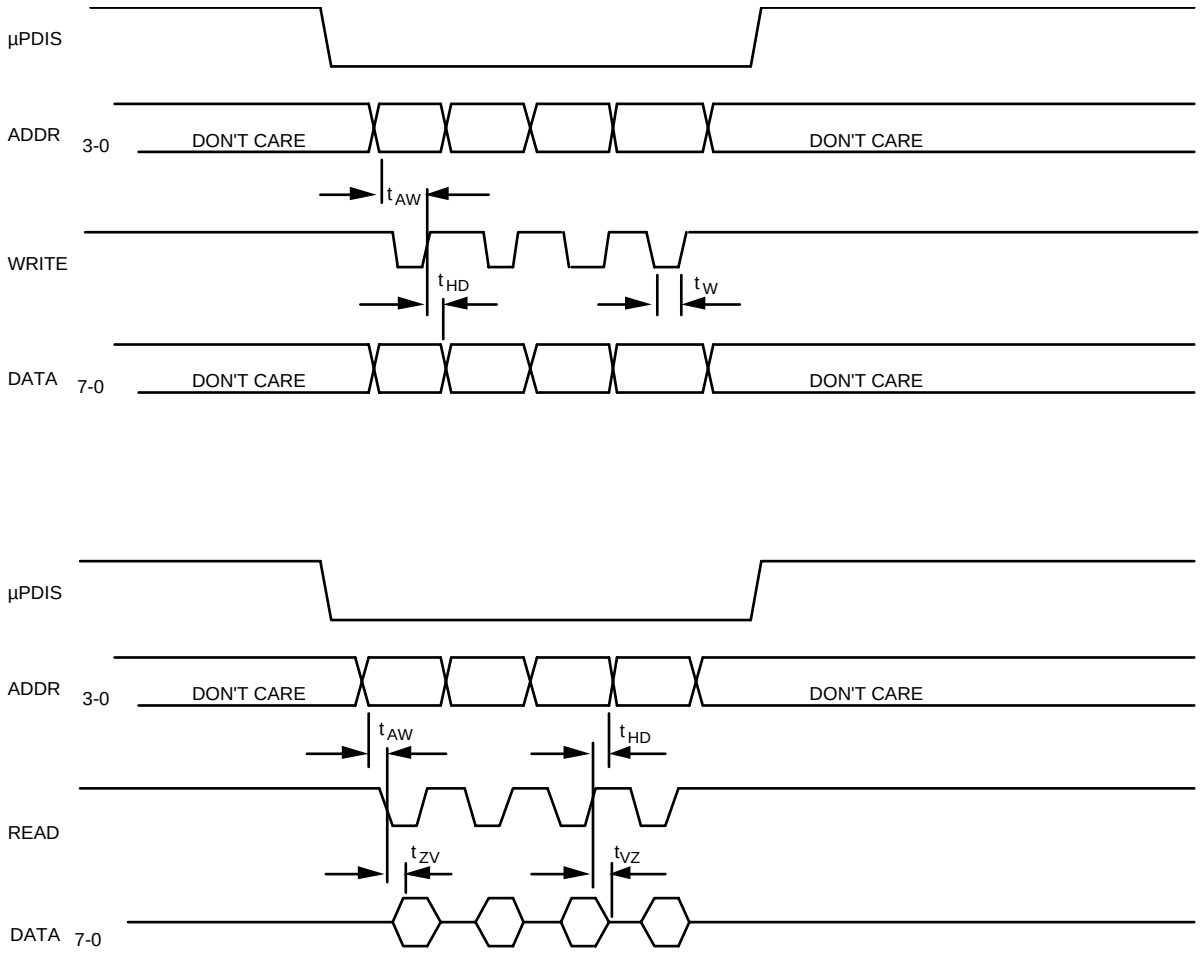
Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
f_{CLK}	**ICLK** Frequency	70*f_{DRDY}	18	70*f_{DRDY}	14	MHz
t_{SS}	**SYMBOL** to **DRDY** setup	20		25		nsec.
t_{HD}	**SYMBOL** to **DRDY** hold	5		8		nsec.
t_{SP}	**SYMBOL** Period	3.9		5		µsec.
t_{DA}	**DRDY** to **ACK**	35 + 68*t_{CLK}	30 + 69*t_{CLK}	35 + 68*t_{CLK}	30 + 69*t_{CLK}	nsec.
t_{AD}	**ACK** to **DRDY**	2*t_{CLK}		2*t_{CLK}		nsec.
t_{WA}	**ACK** pulse width	t_{CLK}		t_{CLK}		nsec.
t_{DI}	**DRDY** to **ICLK** setup	5		8		nsec.
t_{IA}	**ICLK** to **ACK**	10	31			nsec.
t_{DO}	**ICLK** to **DOUT**	10	35			nsec.
t_{SR}	**RESET** to **ICLK** setup	2		3		nsec.

Notes: f_{DRDY} = Frequency of **DRDY,** t_{CLK} = Period of **ICLK** =(1/ f_{CLK}).

t_{SR} is only relevant if operation is to commence during the first clock cycle after **RESET** goes high.

MICROPROCESSOR INTERFACE TIMING

1. WRITE OPERATIONS



MICROPROCESSOR INTERFACE ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS

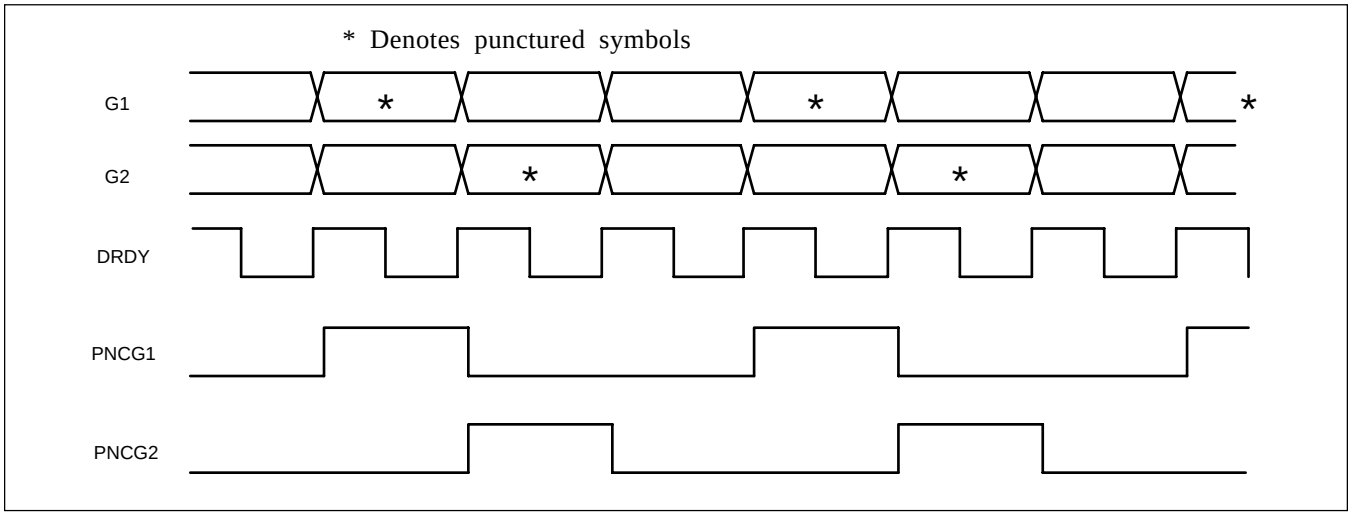
(Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_W	**WRITE** pulse width	5		8		nsec.
t_{AW}	**ADDR** to **WRITE** or **READ** setup	5		8		nsec.
t_{WA}	**WRITE**or **READ** to **ADDR** hold	5		8		nsec.
t_{ZV}	**DATA** Hi-Z to valid		20		27	nsec.
t_{SR}	**DATA** valid to Hi-Z		20		27	nsec.

PUNCTURED MODE OPERATION

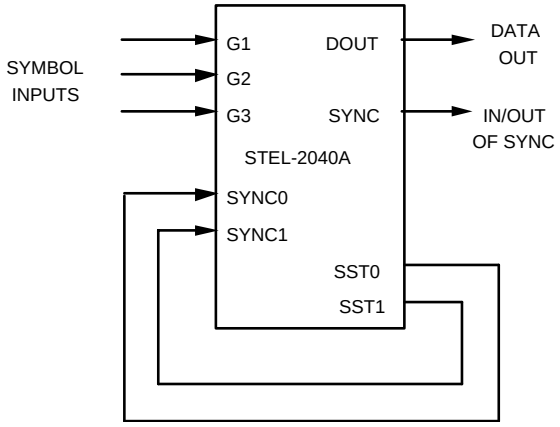
In punctured codes some of the symbols generated by the convolutional encoder are deleted, or punctured, from the transmitted sequence. For example, in an unpunctured Rate $^1/_2$ sequence, four bits would be transmitted for every two data bits. If every fourth bit was punctured from the sequence then only three bits would be transmitted for every two data bits. This would result in a Rate $^2/_3$ code. The STEL-2040B is designed to operate in punctured mode as well as normal, Rate $^1/_2$, mode. This is easily accomplished by means of the **PNCG1** and **PNCG2** signals, which delete the symbol which would normally have been loaded into the device at the time when either of these signals is set high. The punctured symbols are replaced by zero metric values. Zero weight is given to these values in the computations relative to the other symbols. The coding gain is significantly less than that for unpunctured operation, but this is the trade-off for the reduced bandwidth required to transmit the symbols. The recommended puncturing sequences for Rates $^2/_3$ and $^3/_4$ punctured operation are shown in the table. The sequences shown in boldface are the basic sequence, which are then repeated. The use of the **PNCG1** and **PNCG2** signals is shown below for Rate $^3/_4$. The punctured symbols are marked with asterisks. Rates higher than $^3/_4$ are not recommended with the STEL-2040B. Note that the BER monitor will indicate an error each time a symbol is punctured, and consequently the BER monitor is not valid when operating in punctured mode.

Rate	Symbol sequence
$^2/_3$	**G1 G2 G1 P** G1 G2 G1 P G1 G2 G1 P G1 G2 G1 P G1 G2
$^3/_4$	**G1 G2 P G2 G1 P** G1 G2 P G2 G1 P G1 G2 P G2 G1 P



USING AUTOMATIC NODE SYNC

The automatic node sync circuit built into the STEL-2040B can be used to provide node sync in applications where this is not intrinsic to the nature of the operation. The automatic node sync is enabled by connecting the SST1 and SST0 outputs to the SYNC1 and SYNC0 inputs, as shown below. The threshold should be set according to the expected signal to noise ratio of the input signal for optimum operation of the system.

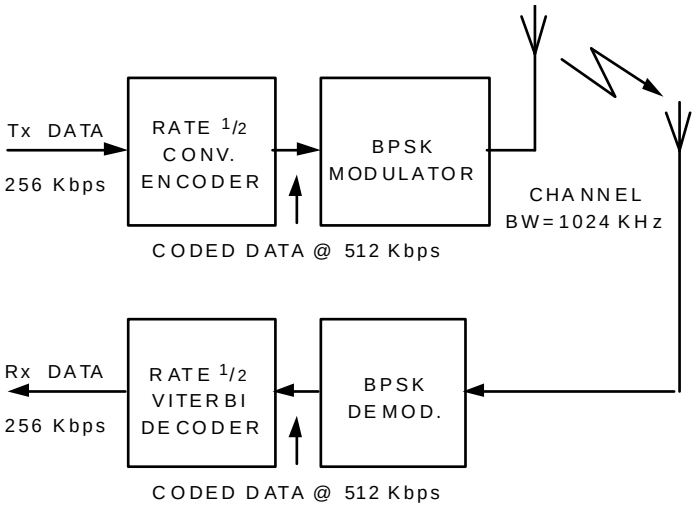


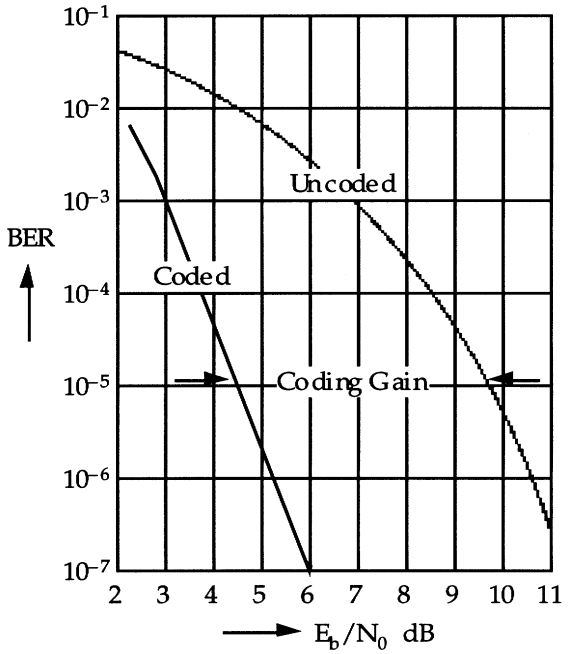
BPSK COMMUNICATION SYSTEM USING CONVOLUTIONAL ENCODING AND VITERBI DECODING. RATE = 1/2

The STEL-2040B can be used in a variety of different environments. One example is shown below. It cannot be used as a common encoder or decoder in multi-channel applications because of the memory incorporated on the chip which is dedicated to a single channel.

An example of a system using the convolutional coder and Viterbi decoder is illustrated here. The system modulates a data stream of rate 512 Kbps using binary PSK (BPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate 1/2 encoding). Alternatively, the system could make use of two parallel channels to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder. A single data bit is clocked into the 7 bit shift register on the rising edge of **DATA CLK**. The decoder portion of the STEL-2040B is designed to accept symbols synchronously. **DRDY** is supplied by the user to clock in the symbols. The maximum data rate is 256 Kbps, using a clock frequency of 18 MHz. This corresponds to 512 K symbols per second at rate 1/2 and 768 K symbols per second at rate 1/3. 18 MHz crystals are readily available, and this clock frequency can be used at all data rates, although the power consumption can be reduced by using lower clock frequencies.





BPSK Communication System using Convolutional Encoding and Viterbi Decoding. Rate = 1/2

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