STEL-9244

Data Sheet

STEL-9244

5 - 40 MHz

QPSK Burst Receiver

intel

Key Features

- **Burst QPSK demodulation**
- **Data rate is 2.56 Mbps**
- **Tunable 5 - 40 MHz RF input frequency for system flexibility**
- **Fast acquisition time to minimize channel overhead; short preamble & short guard time between bursts**
- **MAC friendly features (see Page 9)**

Easy-to-Implement Solution to the Upstream Demodulation Challenge

Stanford Telecom's burst QPSK demodulator products provide the fastest, easiest way to design complete headend QPSK receivers. The STEL-9244 offers a ready-made solution to one of the most difficult technical challenges in implementing interactive broadband services -- providing the upstream demodulation functions which enable information transmitted by subscribers to be received by the headend equipment. As a companion product, the STEL-1108 provides QPSK modulation from a set-top box or cable modem.

High Performance for Efficient Utilization of Upstream Spectrum

The STEL-9244 delivers extremely fast acquisition times to minimize channel overhead. Our digital approach, using differential encoding and coherent detection, results in robust performance in the presence of impulse noise and provides stable, repeatable performance. The unit is tunable to receive TDMA and FDMA signals over a broad input frequency range of 5 - 40 MHz. QPSK (Quaternary Phase Shift Keying) has been shown to be robust and reliable in field proven tests and is an emerging industry standard for the upstream channel.

Ideal for High Speed Data, Voice, and Video Upstream Applications

Data bit length per burst is programmable by the user for compatibility with ATM and other packet lengths. The bit rate is 2.56 Mbps for optimal T1 data and telephony performance.

Compact Form Factor

The unit measures 4.5″ x 5.5″ x .5″, which makes it an ideal size for mounting as a daughter card.

Functional Description

The STEL-9244 (STEL-9244A for the final version using a custom ASIC in place of the two Altera FPGAs) is a burst QPSK receiver designed for fast acquisition of closely spaced TDMA burst signals. Figure 1 below is a simplified block diagram.

Operation

The unit is initially configured using the Serial Control input to the Microprocessor. After the input frequency is programmed, the desired signal will be tuned to 70 MHz for digitization and processing. The input signal consists of a 14 symbol preamble followed by the data packet. The packet length may be programmed. When the input signal is demodulated, the data bits are framed by the DATAVAL signal. An average of the input signal and input noise power is available on the RSSI bus.

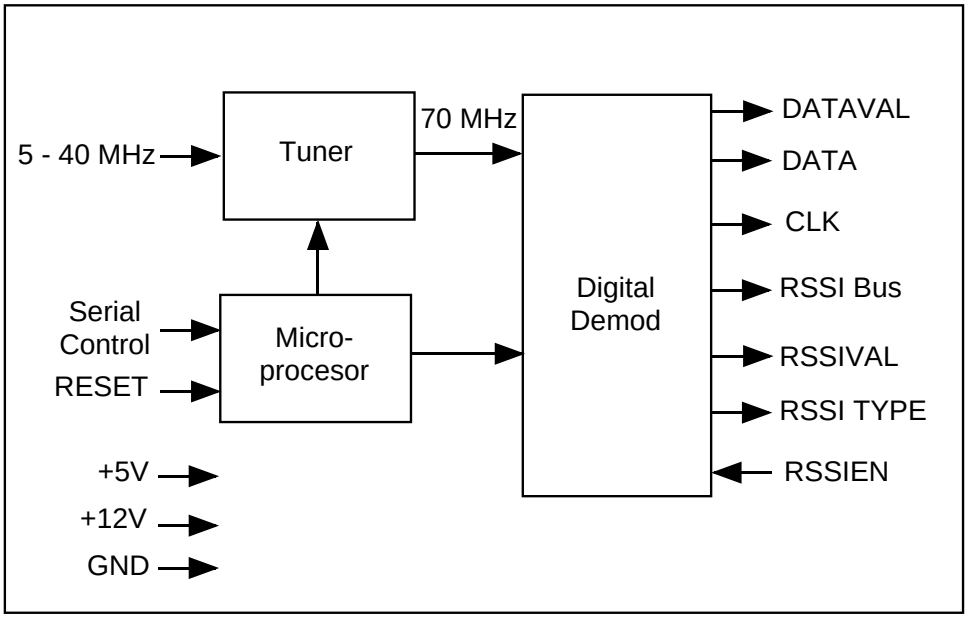


Figure 1 - Receiver Block Diagram

Specifications

Input Characteristics

Frequency Range	5 to 40 MHz
Input Signal Level	> -5 dBmV
Input Noise Level	< -10 dBmV
Minimum Eb/No	9 dB for input > -3 dBmV 13 dB for input < -3 dBmV
Input Impedance	75 Ohms
Max Input Power	-20 dBm
PLL Tuning Time	Approx. 30 ms
Input Freq. Accuracy	Symbol Rate x 0.6% = 1.28 Msps x 0.6% = 7.68 kHz

Performance

BER	5 x 10-6 max. for Eb/No=13 dB @ signal input level = +5 dBmV
Guard Time	2 symbols min.
Preamble	1111110000 110000000000000000 (14 symbols = 28 bits)
Data Rate	2.56 Mbps QPSK (differentially encoded)
Burst Length	Up to 2K bytes*
Retune Rate	Up to 25 command strings/second

Master Clock Input (option)

Frequency	43.52 MHz
Stability	25 ppm
Duty Cycle	45/55

Temperature Range

Operational	0 to 70° C
Storage	-40 to +85° C

Supply Voltages

Digital	+5 V @ 850 mA typ.
Analog	+12 V @ 280 mA typ.

*Long burst lengths may require precision Tx bit clk or locked Tx & Rx clocks (See Fig. 2).

Packet Length Considerations

The maximum packet length is determined by the transmitter bit clock accuracy. Since the STEL-9244 performs a one-time bit synchronization during the preamble, the bit timing accuracy will degrade as the transmitted bit timing drifts with respect to the STEL-9244's bit clock. This can cause the BER performance to degrade near the end of the packet when long packets are transmitted.

Figure 2 shows the transmit bit clock accuracy requirements vs. packet length. This effect can be eliminated by frequency locking the receiver's time base to the transmitter's time base.

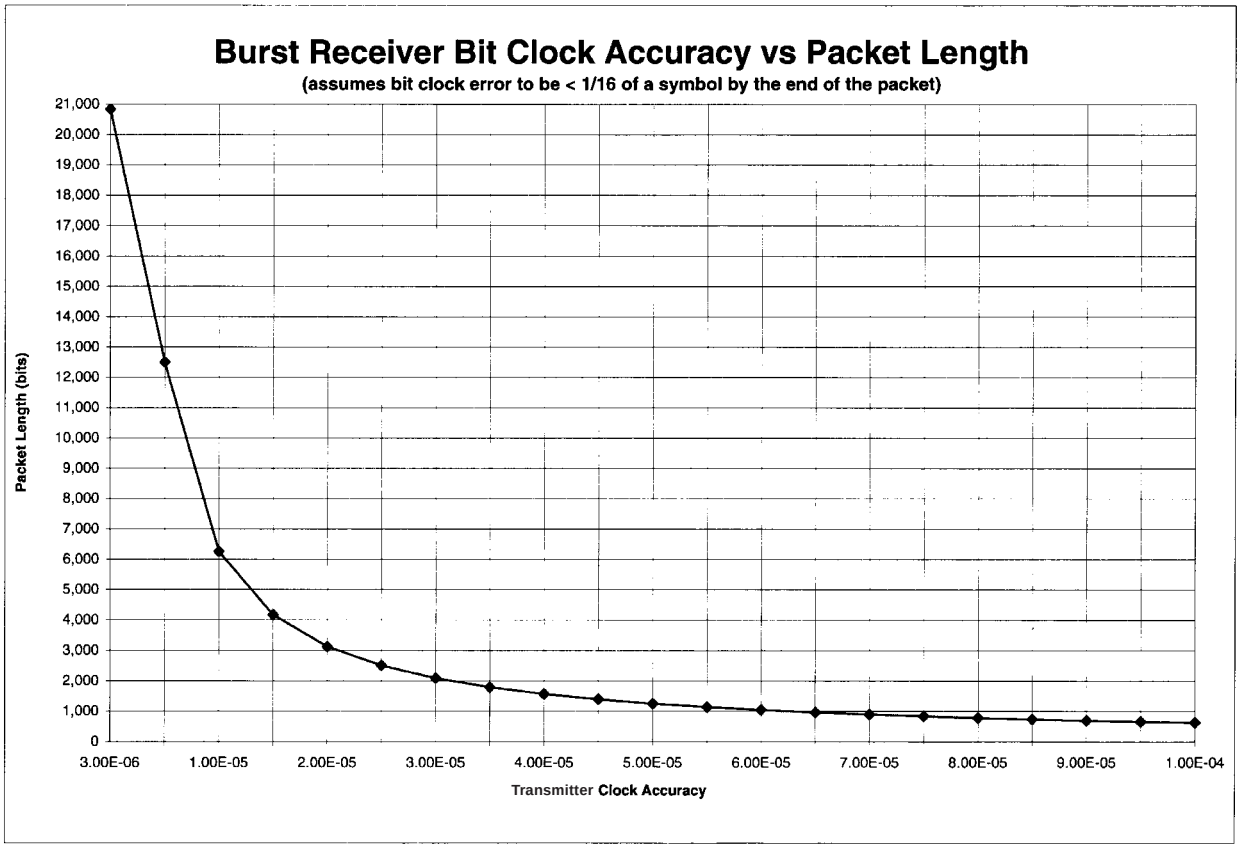


Figure 2

Tx Filter Coefficients

The receiver works well with a transmit spectrum designed for alpha = 0.4, root raised cosine. The following recommended transmit FIR filter coefficients (Set A) are as calculated in the STEL-1208, the STEL-1108 evaluation board. The FIR filter coefficients (Set B) form a specially shaped / matched filter for use with the STEL-9244. Set B may improve the Bit Error Rate performance by approximately 0.5 dB, compared to Set A, when using the STEL-1108 as the modulator.

Set A

FIR Filter Coefficients

0, 31	0	4, 27	-5	8, 23	8	12, 19	7
1, 31	3	5, 26	-2	9, 22	-15	13, 18	99
2, 29	3	6, 25	7	10, 21	-41	14, 17	203
3, 28	-2	7, 24	15	11, 20	-41	15, 16	272

Set B

FIR Filter Coefficients

0, 31	0	4, 27	-14	8, 23	29	12, 19	-36
1, 31	6	5, 26	-7	9, 22	-25	13, 18	139
2, 29	5	6, 25	17	10, 21	-93	14, 17	346
3, 28	-5	7, 24	39	11, 20	-114	15, 16	485

WCP 52121.c-8/19/96

Input Level Dynamic Range

The input level dynamic range of the receiver is a function of Eb/No, as shown in Figure 3. In a typical data-over-CATV system, as the transmit level is increased, the Eb/No will increase, and the burst receiver will continue proper reception for over a 30 dB range.

Figure 3 shows the typical operational area of an STEL-9244 board. It shows that the best operating condition requires greater than 0 dBmV input signal level and less than -10 dBmV noise level.

Note: In general, higher input signal is required when S/N ratio is low.

The S/N ratio can be obtained from the chart by subtracting signal level from the noise level. The Eb/No can be calculated by subtracting 3 dB from the S/N ratio (for QPSK).

Adaptive Threshold Function

In order for the adaptive threshold function to operate correctly, an occasional measurement of the background channel noise must be made by the STEL-9244. The measurement period is equal to the user-programmed Noise Accumulator Length (Serial Byte #13). This should be left at the factory setting of 191 symbols.

The measurement need only be performed frequently enough to allow the receiver to track the average background channel noise level (on the order of minutes).

Burst Demod Dynamic Range

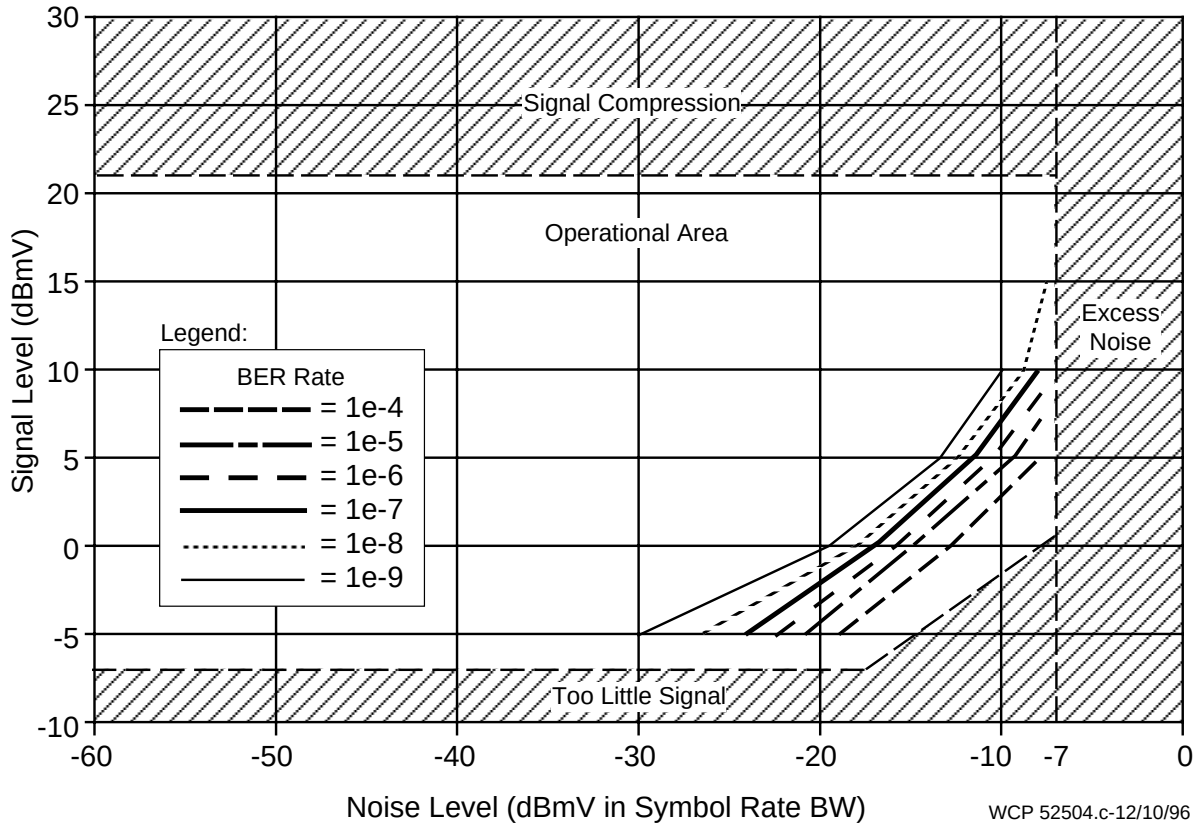


Figure 3. Burst Demod Dynamic Range (Typical)

Command Strings

The unit is controlled via a serial TTL interface, using industry standard UART timing, having the following parameters: 19.2 K baud, 1 start bit, 8 data bits, 1 stop bit, no parity. The unit can accept up to 25 command strings per second. A command string consists of bytes 1 through n for n = 1 . . . 19.

Download command software is also included in the STEL-9244 shipping package that can be used to configure the unit. Note that "not" all bytes must be sent in order to configure the unit. Normally, only the first five (5) command bytes need to be sent, overwriting the default values. See the following example.

A recommended STEL-9244 test fixture design is provided, Figure 6, to simplify I/O interface connection.

Serial Configuration Example

To configure the STEL-9244 for 10 MHz input and 60 byte packet length, send:

04, F4, 01, 10, FF

Byte 1 04: 4 command bytes follow (stream length)

Byte 2,3 F4,01: (10 MHz-5 MHz)/10 kHz

= 500 (decimal) = 01, F4 (hex)

Byte 4,5 10,FF: 60 byte x (4 symbols/byte)

= 240 symbols (decimal) = F0 (hex)

Value = 10000 (hex) - F0 (hex)

= FF, 10 (hex)

The remaining configuration values are factory pre-set for optimal performance.

Byte #	Value	Description	Default Setting (Hex)
1	2 → 0F	Number of command bytes following.	
2 3	00-FF (LSB) 00-0F (MSB)	Tuning steps in 10 kHz increments from 5 MHz. Default = 10 MHz	F4 01
4 5	00-FF (LSB) 00-FF (MSB)	16 Bit number specifying packet length "A" in symbols. Value = 10000 hex - "Packet Length" hex	00 FE
6	0/1	Spectral Inversion, 0 = default (not enabled)	00
7	00-FF	Threshold Gain: Sets ratio of detection threshold to noise average. This determines the false detection vs. missed detection performance. (not enabled)	00
8 9	00-FF (LSB) 00-FF (MSB)	Threshold Lower Limit: Sets minimum adaptive threshold value. Prevents threshold from falling too low, causing excessive false detects.	80 00
10 11	00-FF (LSB) 00-FF (MSB)	Threshold Upper Limit: Sets maximum adaptive threshold value. Prevents threshold from rising too high, causing missed detects. Setting upper threshold equal to lower threshold results in a fixed threshold.	F0 00
12	00-FF	Signal Accumulator Length: Sets number of symbols over which accumulator averages signal power. Default=191 symbols. (Length=256-programmed byte) Changing this default will necessitate recalibration of the signal RSSI table (Table 1).	40
13	00-FF	Noise Accumulator Length: Number of symbols over which accumulator averages noise power. Default=191 symbols. (Length=256-programmed byte) (Do not change)	40
14	00-FF	Threshold Offset (not enabled)	00
15	00-88	RSSI View Port Byte: upper 4 bits = signal; lower 4 bits = noise	51
16 17	00-FF (LSB) 00-FF (MSB)	16 Bit number specifying packet length "B" in symbols. Value = 10000 hex - "Packet Length" hex	00 FE
18	00-0E	Unique Word Detect Qualifier: Number of zeroes out of 14 to search for in preamble.	0C
19 20	00-FF 00-FF	RSSI Noise Holdoff Value: 16 bit number specifying number of symbols to wait before taking a second RSSI noise measurement. Value = FFFF hex - number of symbols.	FF FF

RSSI

The received signal strength output bus gives signal power as an 8 bit number. This function supplies both a measurement of the noise between bursts and of the signal power. When the RSSIVAL signal goes high, and the RSSI type signal is high, then a valid signal power measurement is available on the RSSI bus. When the RSSIVAL signal goes high, and the RSSI type signal is low, then a valid noise power measurement is available on the RSSI bus. RSSIVAL goes high in relation to the Signal/Noise Accumulator completing a measurement, as shown in the timing diagram, Figure 5.

The input signal is temperature compensated and the analog supply has local regulation in order to make the RSSI measurement accurate to within ± 2 dB, typical, over a 0 to 70°C range.

Use RSSI output signal strength look-up tables 1 and 2 to convert the RSSI number (in Hex) to a power reading.

I/O Signal Description

5.1 J3 40 pin straight header connector, SAMTEC TLW-120-06-6-D (suggested mating connector: 3M Part #3448-89140 with strain relief (or) Digit Key Part #MKSR40-ND)

Pin Number	Signal Name	Description
1	+5V	Digital Power
2	+5V	Digital Power
3	+12V	Analog Power
4	GND	Ground
5	+12V	Analog Power
6	RxData	Serial Data Input for configuring the 9244.
7	GND	Ground
8	N/C	Reserved
9	N/C	Spare
10	GND	Ground
11	Reset	Active high reset. Must be held high for >100us after 9244 is powered up.
12	N/C	Spare
13	N/C	Spare
14	N/C	Spare
15	GND	Ground
16	GND	Ground
17	N/C	Reserved
18	AcqEn	Acquisition enable input. (1k pull-up to +5v) Hi = receiver will acquire Low = receiver will not acquire
19	PktLenSel	Packet length select. (1k pull-up to +5v) Hi = packet length "A" Low = packet length "B"
20	N/C	Spare

I/O Signal Description, Cont'd.

5.1 J3, Cont'd.

Pin Number	Signal Name	Description
21	MCLKIN	Master Clock Input, 43.52 MHz, TTL level (future)
22	N/C	Spare
23	RSSINHOFF	RSSI noise measurement holdoff input. (1k pull-down to ground) Hi = RSSI noise measurements disabled. Low = RSSI noise measurements enabled.
24	DataOut	Demodulated data output at 2.56 Mbps.
25	DataVal	Data Valid output. Frames entire data packet. Active high.
26	RSSI TYPE	Hi = signal measurement; Low = noise measurement
27	ClkOut	Recovered clock output. Rises at the center of each demodulated data bit. Runs continuously.
28	RSSIVAL	Rising edge occurs when RSSI data & RSSI Type change to new state. Pulse width = 1 symbol
29	RSSIEN	Enables the RSSI lines to drive out. Active low input.
30	N/C	Spare
31	GatedClk	Gated clock output. Same as ClkOut above, except that it is enabled by DataVal, and is thus not continuously running.
32	RSSI7	Received Signal Strength Indicator (msb)
33	RSSI6	Received Signal Strength Indicator
34	RSSI5	Received Signal Strength Indicator
35	RSSI4	Received Signal Strength Indicator
36	RSSI3	Received Signal Strength Indicator
37	RSSI2	Received Signal Strength Indicator
38	RSSI1	Received Signal Strength Indicator
39	RSSI0	Received Signal Strength Indicator (lsb)
40	N/C	Spare

Power-on Configuration

After power is applied to the board, the Reset input must be asserted. After the Reset is released, the board requires approximately 10 seconds to configure itself for operation.

STEL 9244 Burst Demodulator
Added Features as of 10/9/96

1. Dual Packet Length Control
The packet length of the received burst is selectable between two values by an external TTL signal, called Packet Length Select, applied to pin 19 of connector J3. A high input will select packet length "A" and a low input will select packet length "B." Packet lengths "A" and "B" are specified by downloading a command via the serial interface. The format for these commands is described on page 6. Packet length "A" is specified in bytes #4 and #5, and packet length "B" is specified in bytes #16 and #17. The packet lengths can be programmed for up to 64K symbols. If no signal is applied to pin 19, the default is packet length "A."

2. External Acquisition Enable
An external TTL signal, called Acquisition Enable, applied to pin 18 of connector J3 will control whether or not the receiver will attempt to acquire. A high input will allow the receiver to acquire and a low input will disable all acquisition functions. If no signal is applied the default state allows acquisition. When the acquisition is disabled, the noise RSSI function is still enabled and output measurements will continue as normal.

3. Noise RSSI Measurement Hold Off Pin
This feature enables synchronization of the noise RSSI measurements with packet length boundaries via a control pin. An external TTL signal, called Noise RSSI Hold Off, applied to pin 23 of connector J3 controls when noise RSSI measurements are taken and output. If this signal is low, noise RSSI measurements are enabled, when it is high, noise RSSI measurements are disabled. This control signal is sampled on the rising edge of an internal version of RSSI Valid. Therefore, if Noise RSSI Hold Off is asserted after RSSI Valid goes high to indicate a completed signal measurement, one noise RSSI measurement will be performed, and then the circuit will be disabled untill Noise RSSI Hold Off is deasserted. If no signal is connected to this pin, the default is that noise RSSI measurements will be enabled.

4. Noise RSSI Measurement Hold Off Register
This enables synchronization of the Noise RSSI measurements with packet length boundaries via a programmable counter value. After the end of a burst, a Noise RSSI measurement will be taken. Subsequent Noise RSSI measurements will then be held off until after the programmed number of symbol periods has passed. This delay can be programmed by downloading a command via the serial interface. It is specified in bytes #19 and #20, and can be programmed for zero to 64K - 1 symbols periods. If a data burst comes along before the delay has elapsed, then a Signal RSSI measurement and a subsequent Noise RSSI measurement will be performed, and then the hold off count will start from the beginning. The default hold off delay is zero symbols.

5. Unique Word Detect to Qualify Acquisition
A circuit has been added to qualify the acquisition process and therefore reduce false detects. The circuit looks for the string of zeroes that is present at the end of the packet's preamble. When the receiver gets a signal detection, it will either continue the acquisition process or cancel it, depending on whether the string of zeroes has been found. The number of zeroes in the preamble is fourteen, and the number of zeroes that the circuit searches for is programmable from zero to fourteen via the serial interface using byte #18. The default match value is 12.

RSSI Output Signal Strength Look-up Table

Signal

Signal RSSI Value (Hex)	Typical* Standard Deviation (LSB)	Absolute** Power (dBmV)	Absolute** Power (dBm) (BW= 1.28 MHz)
11	1.0	-6.35	-55.10
12	1.0	-5.73	-54.48
15	1.0	-4.56	-53.31
18	1.0	-3.54	-52.29
1B	1.0	-2.71	-51.46
1E	1.0	-1.66	-50.41
22	1.0	-0.65	-49.40
26	1.0	0.33	-48.42
2B	1.0	1.33	-47.42
2F	1.0	2.36	-46.39
36	1.0	3.35	-45.40
3D	1.0	4.36	-44.39
45	1.0	5.43	-43.32
4D	1.0	6.39	-42.36
58	1.0	7.40	-41.35
61	1.0	8.39	-40.36
6D	1.0	9.41	-39.34
79	1.5	10.39	-38.36
89	1.5	11.40	-37.35
95	1.5	12.40	-36.35
AA	1.5	13.38	-35.37
BC	2.0	14.37	-34.38
C9	2.0	15.40	-33.36
D2	2.0	16.40	-32.35
DA	2.0	17.47	-31.28
DE	2.0	18.37	-30.38
E2	2.0	19.29	-29.46
E6	2.0	20.40	-28.46

Table 1

Noise

Signal RSSI Value (Hex)	Typical* Standard Deviation (LSB)	Absolute** Power (dBmV)	Absolute** Power (dBm) (BW= 1.28 MHz)
22	2.0	-21.40	-70.15
26	2.0	-20.37	-69.12
2A	2.0	-19.43	-68.18
30	2.5	-18.35	-67.10
37	2.5	-17.36	-66.11
3E	3.0	-16.30	-65.05
46	3.0	-15.33	-64.08
4F	3.5	-14.34	-63.09
5A	4.0	-13.32	-62.07
63	4.5	-12.36	-61.11
73	6.0	-11.33	-60.09
82	7.0	-10.35	--59.10
93	8.0	-9.38	-58.13
A6	10.0	-8.37	-57.12
BF	12.0	-7.37	-56.12

Table 2

* Expected variation in RSSI measurement.

** 75 ohm system

Data Timing

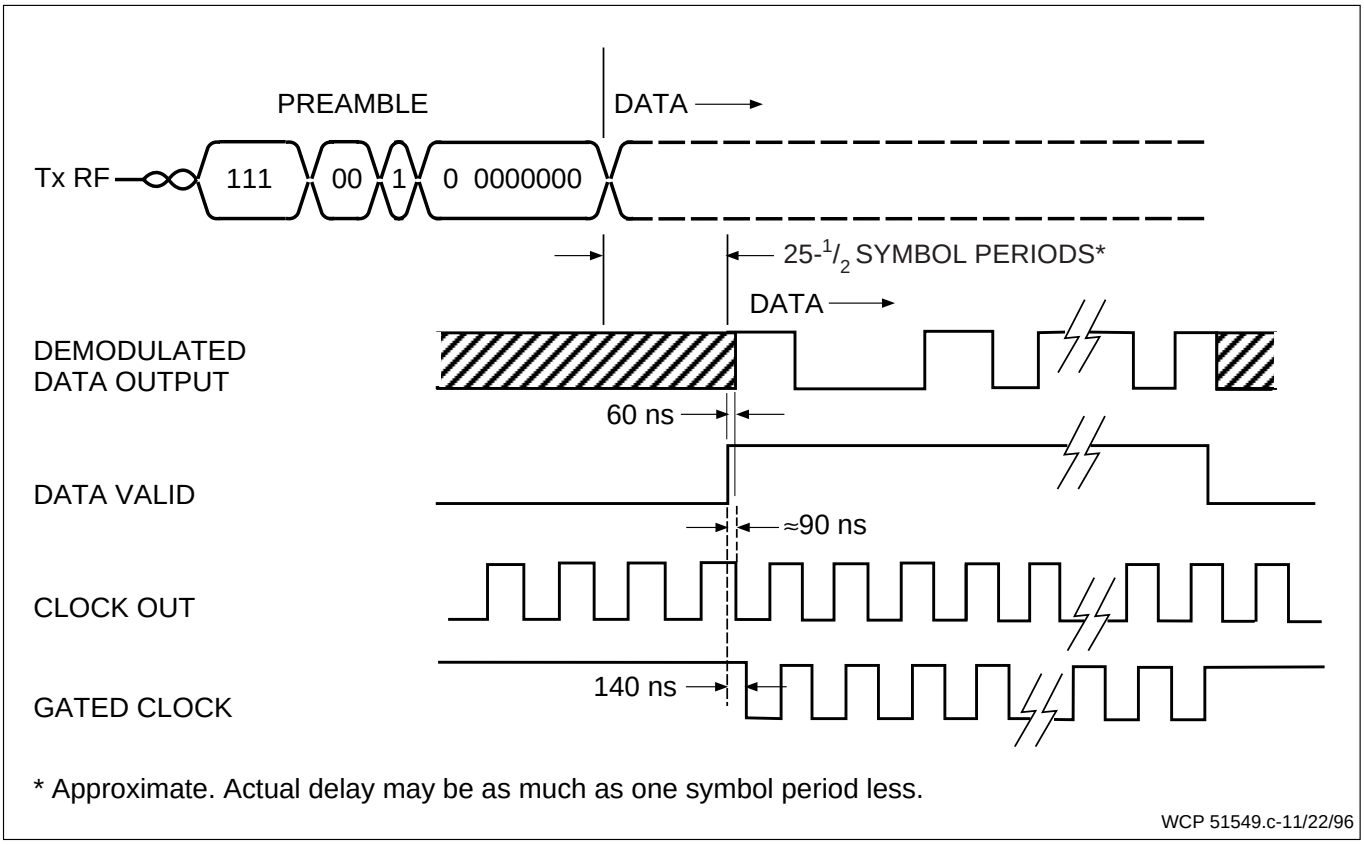


Figure 4

RSSI Timing Diagram

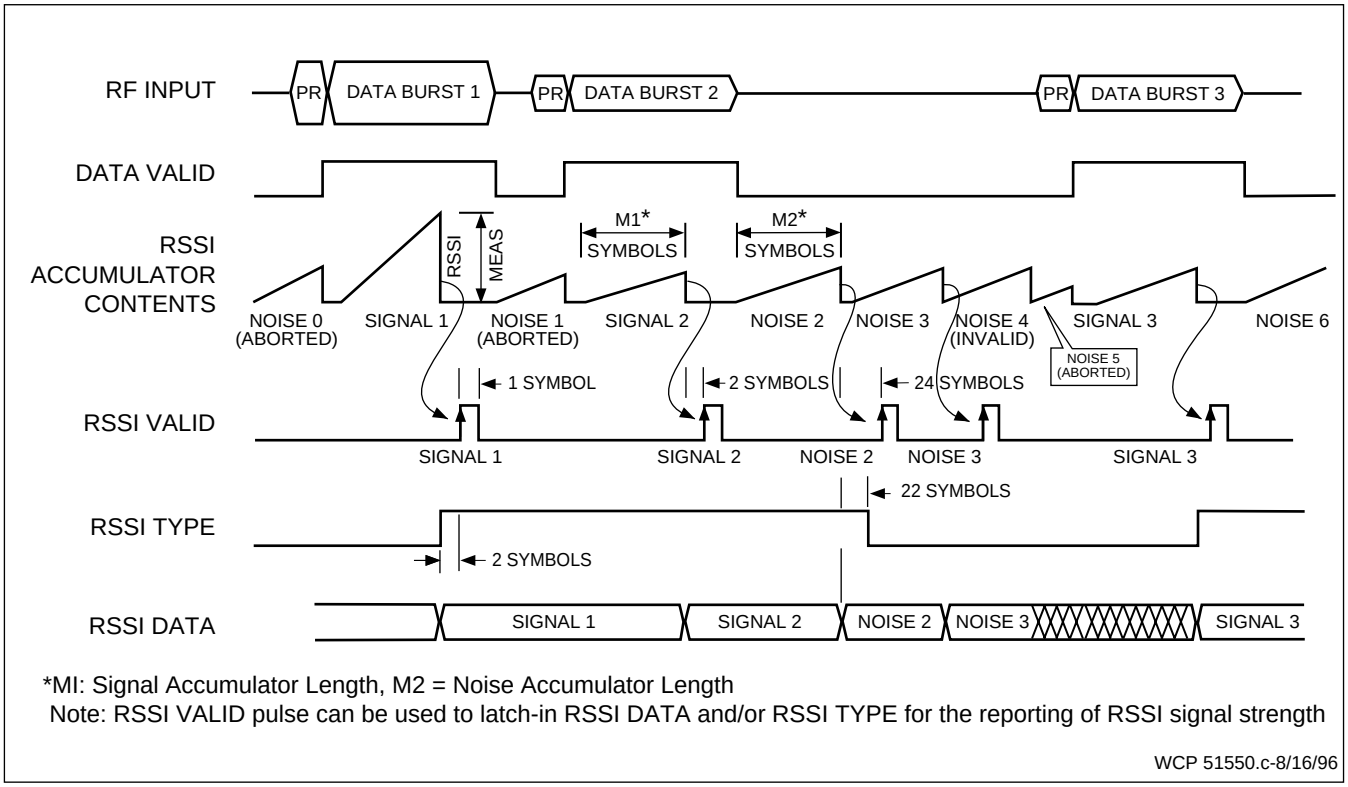
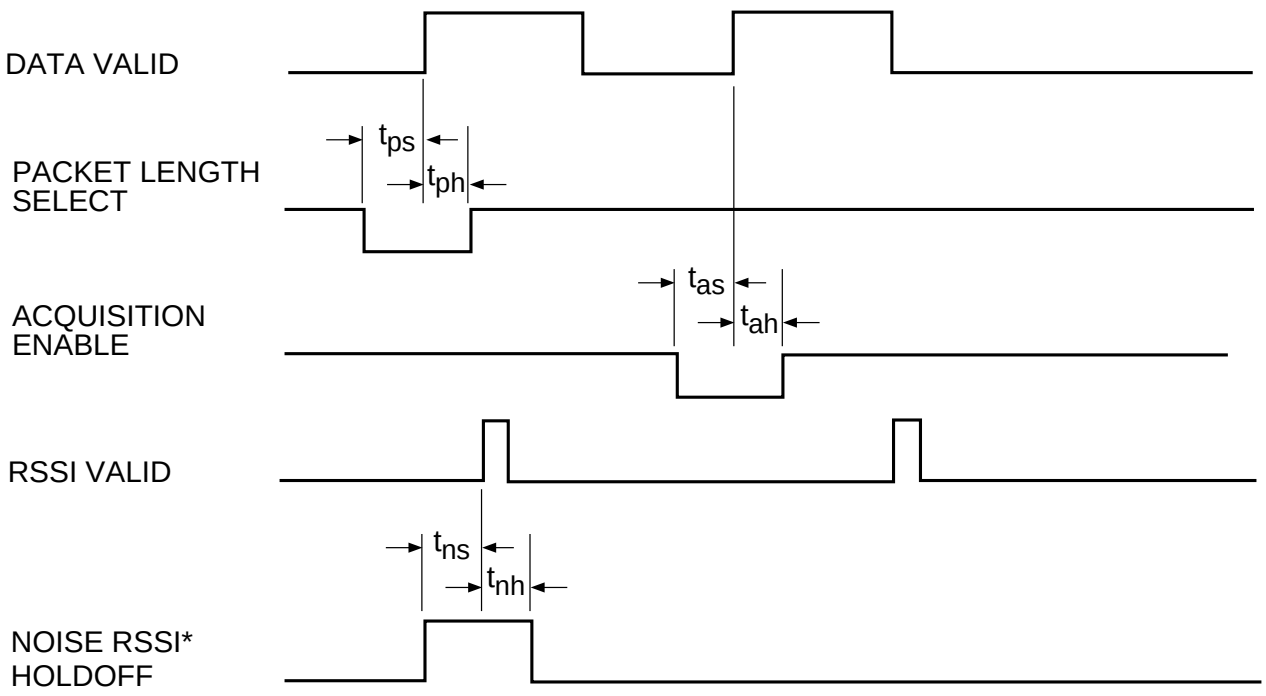


Figure 5



* Noise RSSI Holdoff is recognized at the rising edge of an earlier version of RSSI VALID.

Symbol	Parameter	Min
t_{ps}	Packet Length Select Setup Time	5µs
t_{ph}	Packet Length Select Hold Time	0µs
t_{as}	Acquisition Enable Setup Time	23µs
t_{ah}	Acquisition Enable Hold Time	0µs
t_{ns}	Noise RSSI Holdoff Setup Time	22µs
t_{nh}	Noise RSSI Holdoff Hold Time	0µs

WCP 52488.c-11/22/96

Figure 6

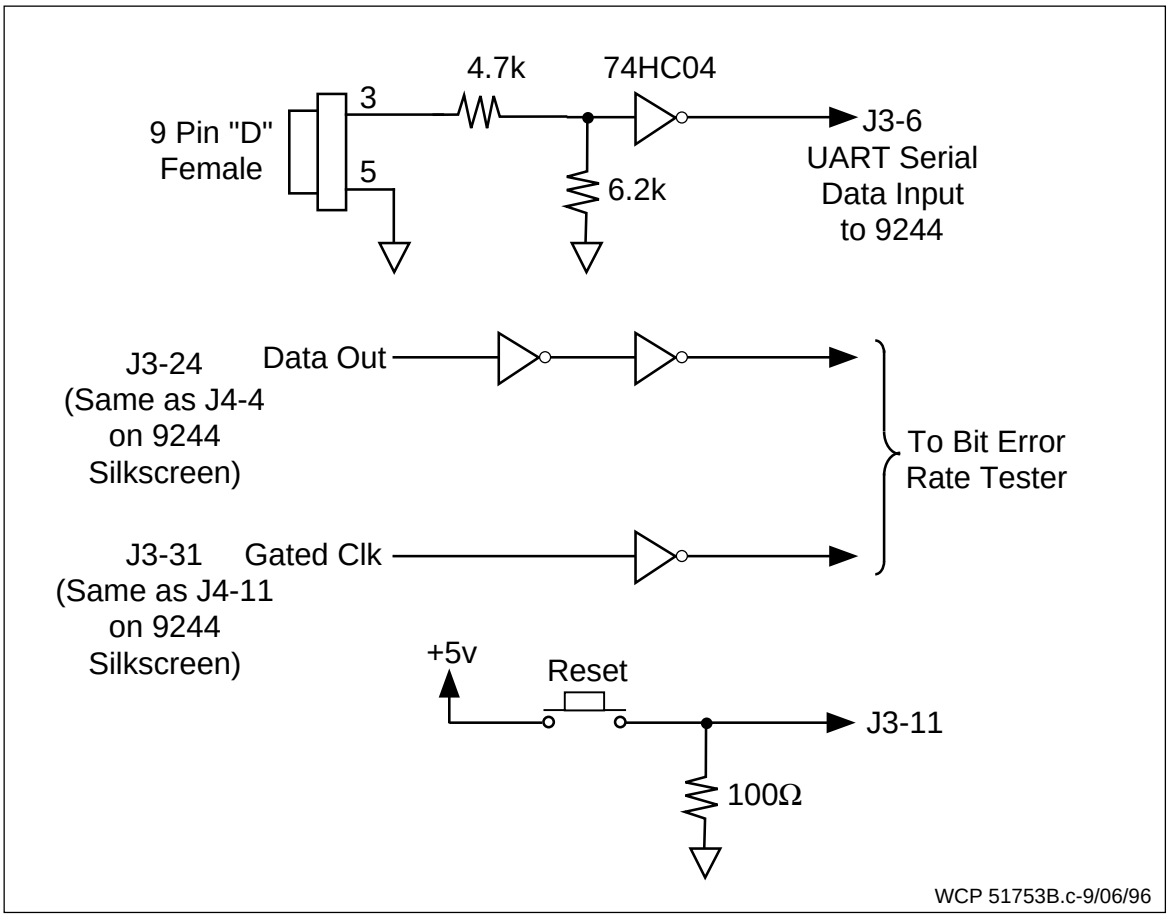


Figure 7 - Test Fixture

Mechanical

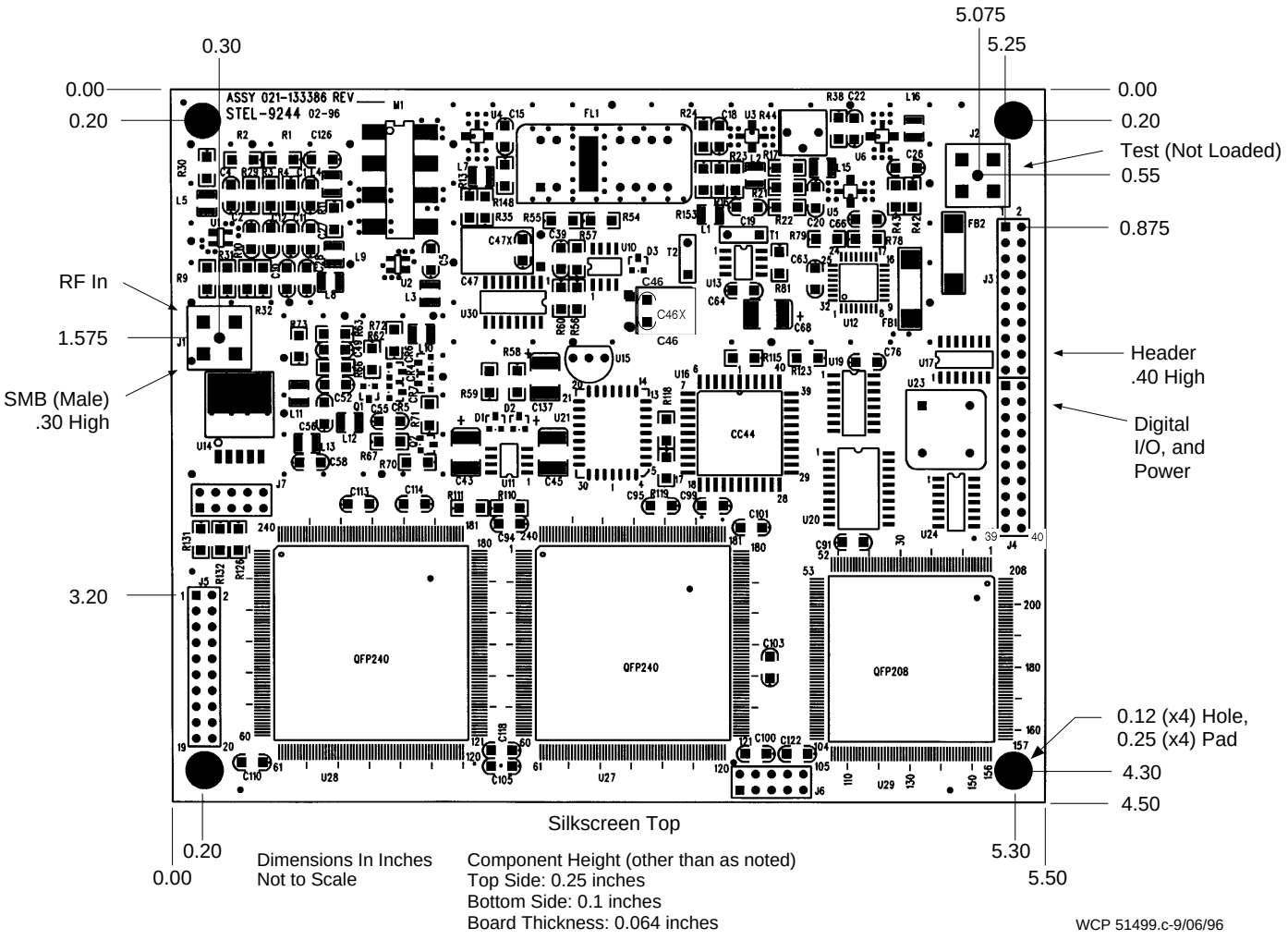


Figure 8 - Board Mechanical

For Further Information Call or Write

INTEL CORPORATION
Cable Network Operation
350 E. Plumeria Drive, San Jose, CA 95134
Customer Service Telephone: (408) 545-9700
Technical Support Telephone: (408) 545-9799
FAX: (408) 545-9888