CD22202, CD22203

January 1997

5V Low Power DTMF Receiver

Features

- **Central Office Quality**
- **No Front End Band Splitting Filters Required**
- **Single, Low Tolerance, 5V Supply**
- **Detects Either 12 or 16 Standard DTMF Digits**
- **Uses Inexpensive 3.579545MHz Crystal for Reference**
- **Excellent Speech Immunity**
- **Output in Either 4-Bit Hexadecimal Code or Binary Coded 2-of-8**
- **Synchronous or Handshake Interface**
- **Three-State Outputs**
- **Excellent Latch-Up Immunity**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD22202E	0 to 70	18 Ld PDIP	E18.3
CD22203E	0 to 70	18 Ld PDIP	E18.3

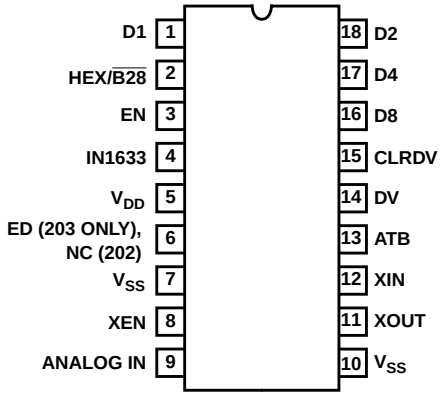
Description

The CD22202 and CD22203 complete dual-tone multiple frequency (DTMF) receivers detect a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.579545MHz TV “colorburst” crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the clock output of a crystal connected CD22202/CD22203 receiver to drive the time bases of additional receivers. This is a monolithic integrated circuit fabricated with low-power, complementary symmetry CMOS processing. It only requires a single low tolerance power supply.

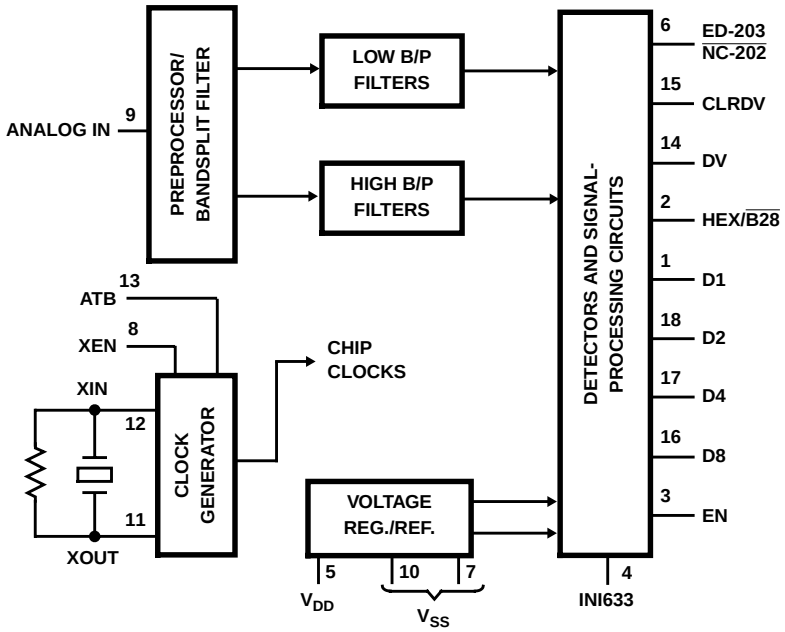
The CD22202 and CD22203 employ state-of-the-art circuit technology to combine the digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60Hz reject and band splitting filters and then hard limited to provide AGC. Eight Bandpass filters detect the individual tones. The digital post processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus oriented architectures.

Pinout

CD22202, CD22203
(PDIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage (V_{DD})(Referenced to V_{SS} Terminal). 7V
Power Dissipation
T_A = 25°C (Derate above T_A = 25°C at 6.25mW/°C. 65mW
Input Voltage Range
All Inputs Except Analog In. . . . . (V_{DD} +0.5V) to -0.5V
Analog in Voltage Range . . . . . (V_{DD} +0.5V) to (V_{DD} -10V)
DC Current into any Input or Output . . . . . ±20mA

NOTE: Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.

Thermal Information

Maximum Junction Temperature . . . . . 175°C
Maximum Junction Temperature (Plastic) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range . . . . . 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

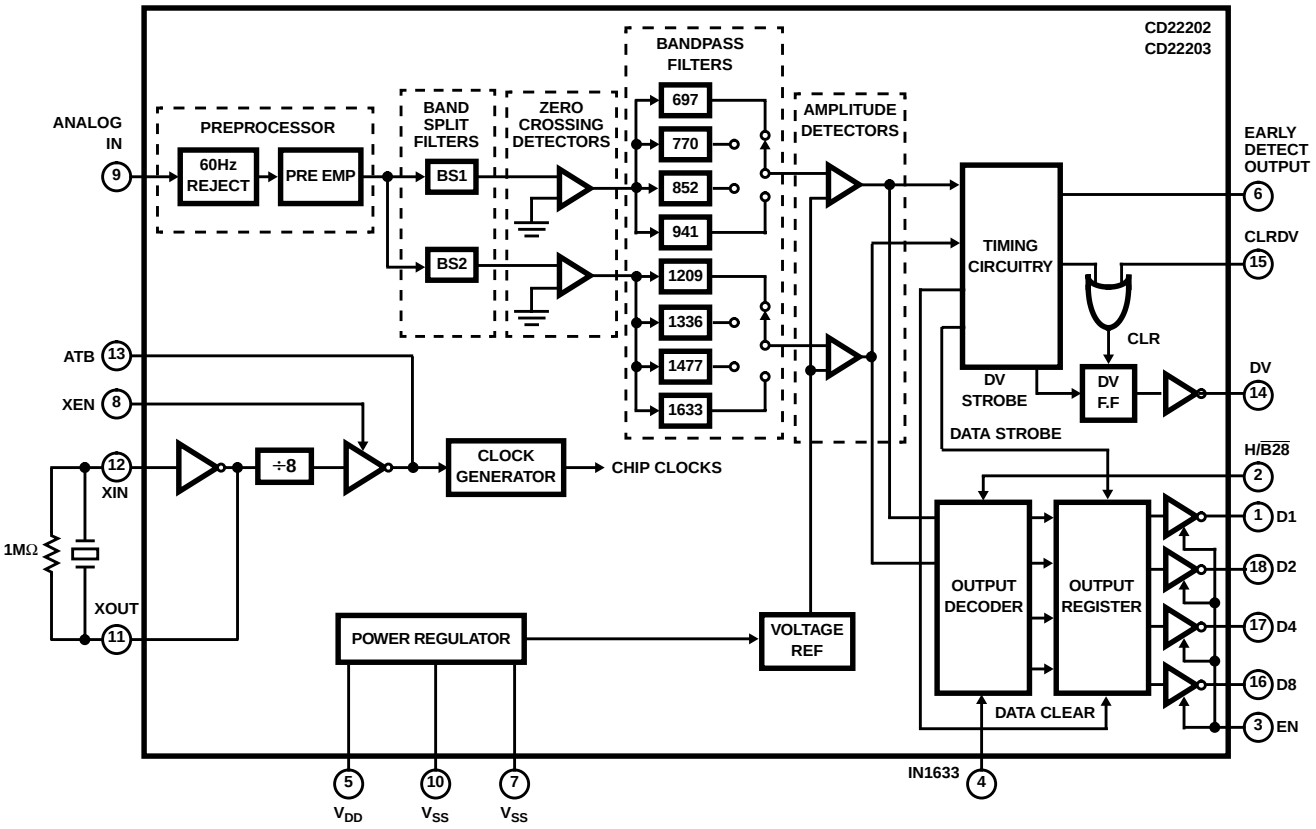
$0°C \le T_A \le +70°C$, V_{DD} = 5V ±10%

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5 + 2Hz)	±2.3	±3.5	% of f_O
Amplitude for Detection	Each Tone	-32	-	-2	dBm Referenced to 600Ω
Minimum Acceptable Twist	$Twist = \frac{High\ Tone}{Low\ Tone}$	-10	-	+10	dB
60Hz Tolerance		-	-	0.8	V_{RMS}
Dial Tone Tolerance	"Precise" Dial Tone	-	-	0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM7291	-	2	-	Hits
Digital Outputs (except XOUT)	"0" Level, 400µA Load	0	-	0.5	V
	"1" Level, 200µA Load	V_{DD} -0.5	-	V_{DD}	V
Digital Inputs	"0" Level	0	-	$0.3V_{DD}$	V
	"1" Level	$0.7V_{DD}$	-	V_{DD}	V
Supply Current	T_A = +25°C	-	10	16	mA
Noise Tolerance	MITEL Tape #CM7291 (Note 1)	-	-	-12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{DD} \ge V_{IN} \ge (V_{DD}$ -10)	100kΩ//15pF	300kΩ	-	

NOTE:

1. Bandwidth limited (3kHz) Gaussian noise.

Functional Block Diagram



NOTE: Pin 6: Early detect output on CD22203 only.

System Functions

Analog In

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

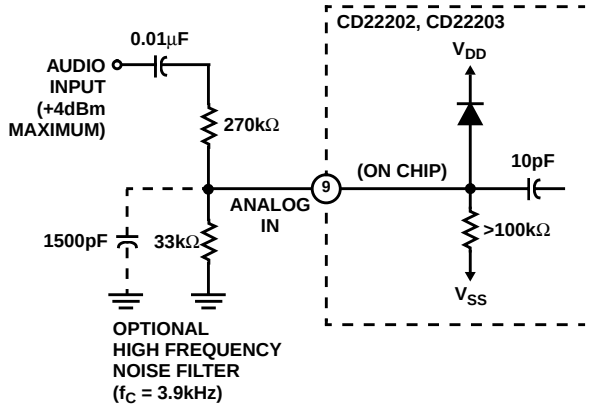


FIGURE 1. ANALOG IN

The CD22202 and CD22203 are designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20dB below the fundamental.

Crystal Oscillator

The CD22202 and CD22203 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television “color-burst” (3.579545MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ resistor is also connected between these pins in this mode. ATB is a clock frequency output. Other CD22202 and CD22203 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal connected CD22202 and CD22203 as shown in Figure 2.

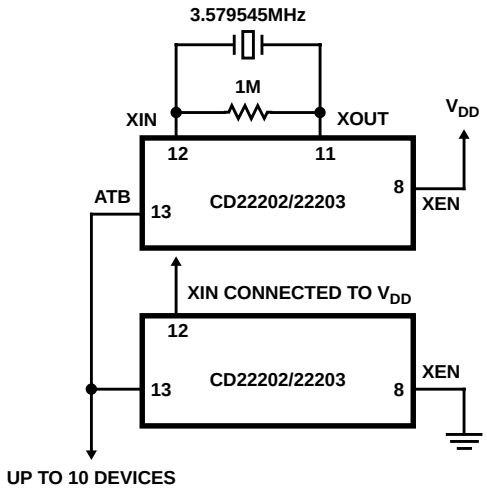


FIGURE 2. CRYSTAL OSCILLATOR

HEX/$\overline{B28}$

This pin selects the format of the digital output code. When HEX/$\overline{B28}$ is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The following table describes the two output codes.

TABLE 1. OUTPUT CODES

DIGIT	HEXADECIMAL				BINARY CODED 2-OF-8			
	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

ED

This pin, on the CD22203 only, indicates the presence of frequencies which are likely to be DTMF digits, but have not yet been verified by a DV signal. It is comparable to a “button-down” output, and it is useful as an EARLY DETECT signal to interrupt a microprocessor for digit storage and validation.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or CLRDV is raised high, whichever is sooner. This handshake can save microprocessor time.

DTMF Dialing Matrix

	COL 0 1209Hz	COL 1 1336Hz	COL 2 1477Hz	COL 3 1633Hz
ROW 0 697Hz	1	2	3	A
ROW 1 770Hz	4	5	6	B
ROW 2 852Hz	7	8	9	C
ROW 3 941Hz	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

N/C Pin

This pin has no internal connection and should be left floating.

Digital Inputs and Outputs

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the “analog in” pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the “maximum ratings” section.

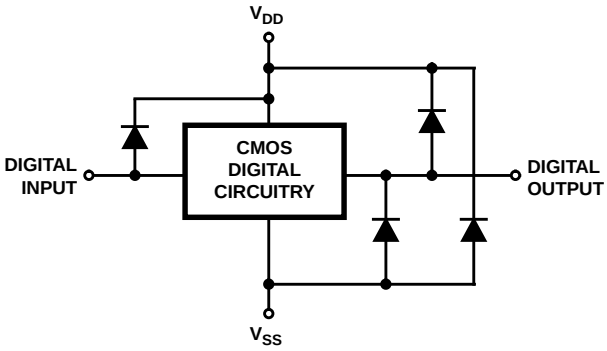


FIGURE 3. DIGITAL INPUTS AND OUTPUTS

Input Filter

The CD22202 and CD22203 will tolerate total input noise of a maximum of 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present

above 28kHz, the simple RC filter shown below may be used to band limit the incoming signal. The cut off frequency is 3.9kHz.

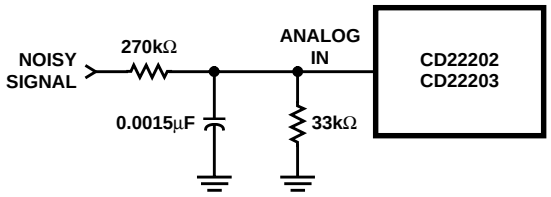
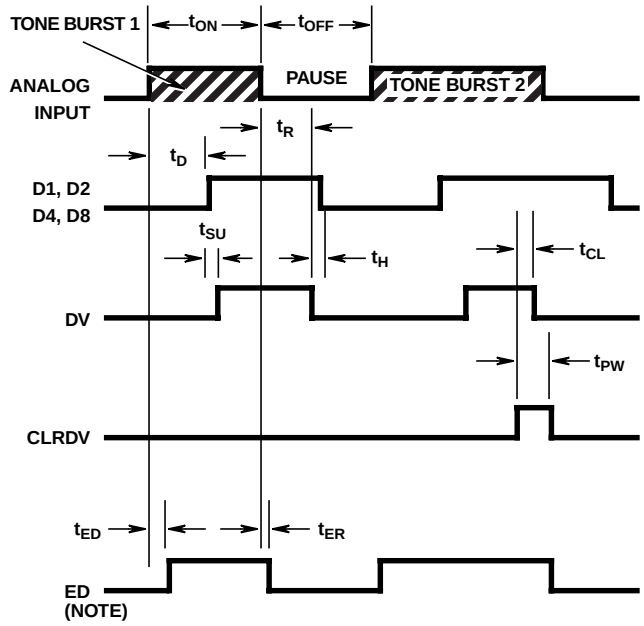


FIGURE 4. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

Timing Waveforms



NOTE: Early Detect output is available only on the CD22203.

FIGURE 5.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Tone Time					
For Detection	t_{ON}	40	-	-	ms
For Rejection	t_{ON}	-	-	20	ms
Pause Time					
For Detection	t_{OFF}	40	-	-	ms
For Rejection	t_{OFF}	-	-	20	ms
Detect Time	t_D	25	-	46	ms
Release Time	t_R	35		50	ms
Data Setup Time	t_{SU}	7	-	-	μs
Data Hold Time	t_H	4.2	-	5	ms
DV Clear Time	t_{CL}	-	160	250	ns
CLRDV Pulse Width	t_{PW}	200	-	-	ns
ED Detect Time	t_{ED}	7	-	22	ms
ED Release Time	t_{ER}	2	-	18	ms
Output Enable Time C_L = 50pF, R_L = 1kΩ	-	-	200	300	ns
Output Disable Time C_L = 35pF, R_L = 500Ω	-	-	150	200	ns
Output Rise Time C_L = 50pF	-	-	200	300	ns
Output Fall Time C_L = 50pF	-	-	160	250	ns

Guard Time

Whenever the DTMF receiver is continually monitoring a voice channel containing distorted or musical voices or tones, additional guard time may be added in order to prevent false decoding. This may be done in software by verifying that both ED and DV are present simultaneously for about 55ms. An appropriate guard time should be selected to balance the fastest expected dialing speed against the rejection of distorted or musical voices or tones (most autodialers operate in the 65ms to 75ms range although a few generate 50ms tones). A hardware guard time circuit is shown in Figure 6. R_3 and R_4 should keep the voice amplitude as low as practical, while R_2 and R_5 adjust detection speed.

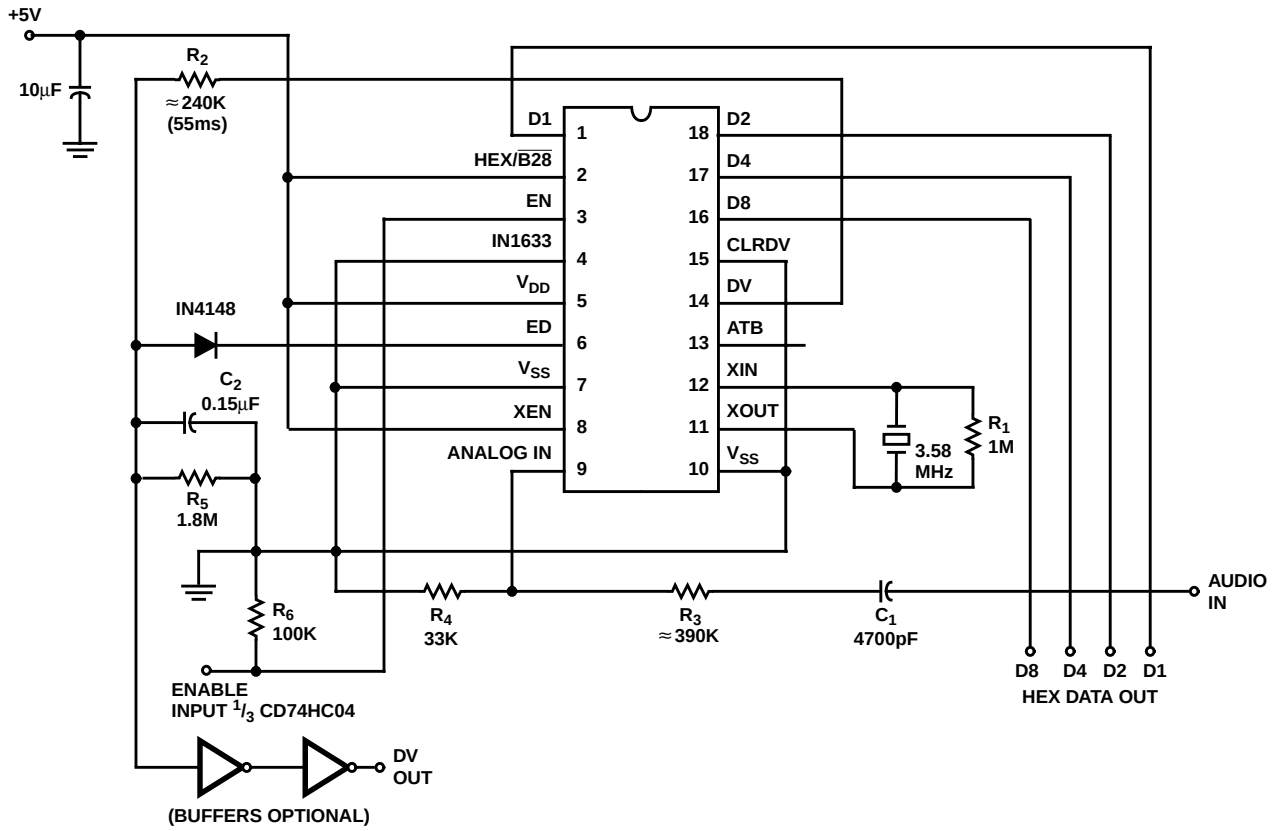


FIGURE 6. CD22203 DTMF RECEIVER WITH GUARD TIME CIRCUIT TO PROVIDE EXCEPTIONAL TALK-OFF PERFORMANCE

Operating and Handling Considerations

Handling

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 “Guide to Better Handling and Operation of CMOS Integrated Circuits”.

Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turnoff transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.