CDP1824, CDP1824C

March 1997

32-Word x 8-Bit Static RAM

Features

- **Fast Access Time**
  - **V_{DD} = 5V 710ns**
  - **V_{DD} = 10V 320ns**
- **No Precharge or Clock Required**

Description

The CDP1824 and CDP1824C are 32-word x 8-bit fully static CMOS random-access memories for use in CDP-1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a pre-charge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

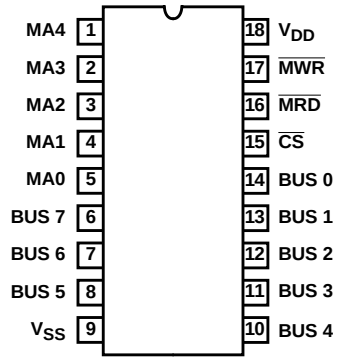
The CDP1824C is functionally identical to the CDP1824. The CDP1824 has an operating range of 4V to 10.5V, and the CDP1824C has an operating voltage range of 4V to 6.5V. The CDP1824 and CDP1824C are supplied in 18 lead hermetic dual-in-line ceramic packages (D suffix), and in 18 lead dual-in-line plastic packages (E suffix).

Ordering Information

5V	10V	PACKAGE	TEMPERATURE RANGE	PKG. NO.
CDP1824CE	CDP1824E	PDIP	-40°C to +85°C	E18.3
CDP1824CEX	CDP1824EX	Burn-In		E18.3
CDP1824CD	CDP1824D	SBDIP	-40°C to +85°C	D18.3

Pinout

CDP1824, CDP1824C (PDIP, SBDIP)
TOP VIEW



OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	DATA PINS STATUS
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	Output Disabled: High-Impedance State

Logic 1 = High Logic 0 = Low X = Don't Care

File Number **1103.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1824 . . . . . -0.5V to +11V
CDP1824C. . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range (T_A)
Package Type D . . . . . -55^oC to $+125^oC$
Package Type E . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	75	20
PDIP Package	75	N/A

Storage Temperature Range (T_{STG}). . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering)
At distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . $+265^oC$

Recommended Operating Conditions

At T_A = Full Package Temperature Range.For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CONDITION	LIMITS				UNITS
		CDP1824D		CDP1824CD		
	V_{DD} (V)	MIN	MAX	MIN	MAX	
Supply Voltage Range	-	4	10.5	4	6.5	V
Recommended Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time (Note 1)	5	-	5	-	5	µs
t_R, t_F	10	-	2	-	-	µs

NOTE:

1. Input signal rise or fall times longer than these maxima can cause loss of stored data in either the selected or deselected mode.

Static Electrical Specifications

At T_A = -40^oC to $+85^oC$, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1824			CDP1824C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	-	5	-	25	50	-	100	200	µA
		-	-	10	-	250	500	-	-	-	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	1.8	2.2	-	1.8	2.2	-	mA
		0.5	0, 10	10	3.6	4.5	-	-	-	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-0.9	-1.1	-	-0.9	-1.1	-	mA
		9.5	0, 10	10	-1.8	-2.2	-	-	-	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1.9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		1.9	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	± 0.1	± 1	-	± 0.1	± 1	µA
			0, 10	10	-	± 0.1	± 1	-	-	-	µA
Operating Current (Note 2)	I_{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA

Static Electrical Specifications At T_A = -40°C to +85°C, Except as Noted: (Continued)

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1824			CDP1824C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	± 0.2	±2.0	-	± 0.2	± 2	µA
		0, 10	0, 10	10	-	± 0.2	±2.0	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

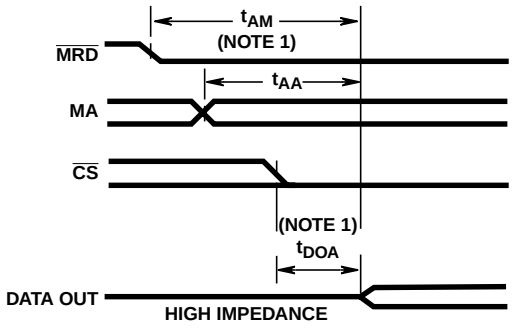
1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, Input t_R, t_F = 10ns, C_L = 50pF, R_L = 200kΩ; See Figure 1

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CDP1824D, CDP1824E			CDP1824CD, CDP1824CE			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
READ OPERATION									
Access Time From Address Change	t_{AA}	5	-	400	710	-	400	710	ns
		10	-	200	320	-	-	-	ns
Access Time From Chip Select	t_{DOA}	5	-	300	710	-	300	710	ns
		10	-	150	320	-	-	-	ns
Output Active From $\overline{MRD}$	t_{AM}	5	-	300	710	-	300	710	ns
		10	-	150	320	-	-	-	ns

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Time required by a typical device to allow for the indicated function. Typical values are for T_A = +25°C and nominal V_{DD}.



NOTES:

1. Minimum timing for valid data output longer times will initiate an earlier, but invalid output.

FIGURE 1. READ CYCLE TIMING DIAGRAMS

Dynamic Electrical Specifications at T_A = -40°C to +85°C, V_{DD} ±5%, Input t_R, t_F = 10ns, C_L = 50pF, R_L = 200kΩ; See Figure 2

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			CDP1824D, CDP1824E			CDP1824CD, CDP1824CE			
		V_{DD} (V)	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
WRITE OPERATION									
Write Pulse Width	t_{WRW}	5	390	200	-	390	200	-	ns
		10	180	150	-	-	-	-	ns
Data Setup Time	t_{DS}	5	390	100	-	390	100	-	ns
		10	180	50	-	-	-	-	ns
Data Hold Time	t_{DH}	5	70	40	-	70	40	-	ns
		10	35	20	-	-	-	-	ns
Chip Select Setup Time	t_{CS}	5	425	210	-	425	210	-	ns
		10	215	110	-	-	-	-	ns
Address Setup Time	t_{AS}	5	640	500	-	640	500	-	ns
		10	390	300	-	-	-	-	ns

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Time required by a typical device to allow for the indicated function. Typical values are for T_A = +25°C and nominal V_{DD}.

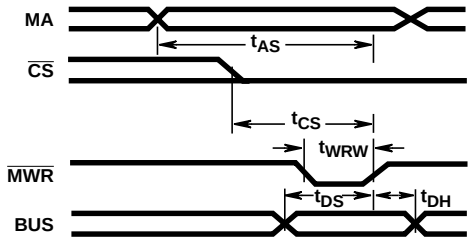
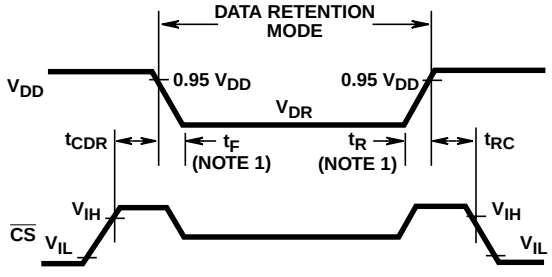


FIGURE 2. WRITE CYCLE TIMING DIAGRAM



NOTE: t_R, t_F > 1µs.

FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS AND TIMING DIAGRAM

Data Retention Specifications at T_A = -40°C to +85°C; See Figure 3

PARAMETER	SYMBOL	TEST CONDITIONS	V_{DD} (V)	LIMITS				UNITS
				CDP1824		CDP1824C		
				MIN	MAX	MIN	MAX	
Data Retention Voltage	V_{DR}		-	2.5	-	2.5	-	V
Data Retention Quiescent Current	I_{DD}	V_{DR} = 2.5V	-	-	10	-	40	µA
Chip Deselect to Data Retention Time	t_{CDR}	V_{DR} = 2.5V	5	600	-	600	-	ns
			10	300	-	-	-	ns
Recovery to Normal Operation Time	t_{RC}	V_{DR} = 2.5V	5	600	-	600	-	ns
			10	300	-	-	-	ns

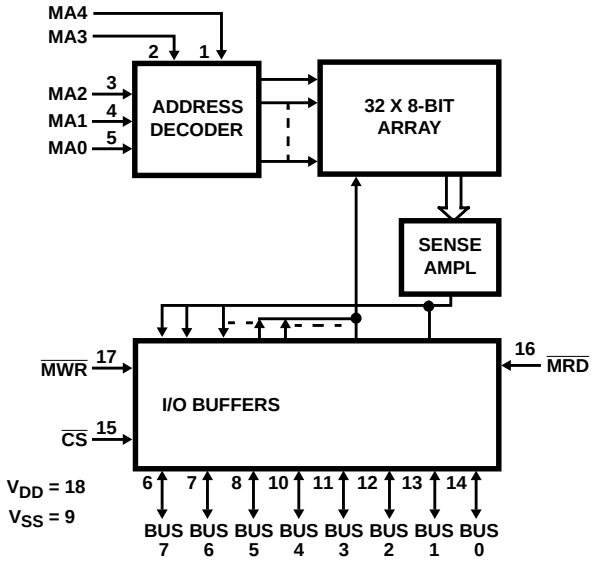


FIGURE 4. FUNCTIONAL DIAGRAM

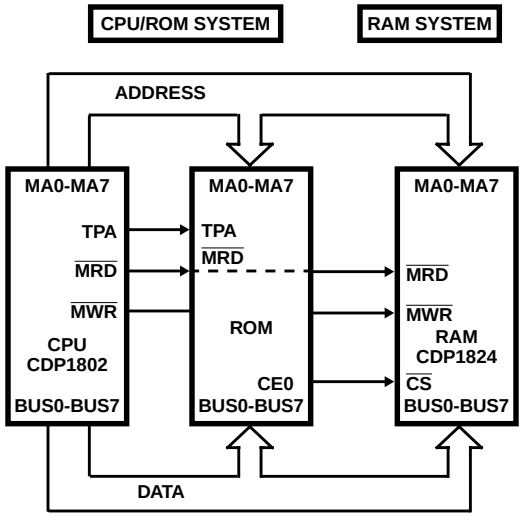


FIGURE 5. CDP1824 (128 X 8) MINIMUM SYSTEM (128 X 8)

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029