HCS125MS

Radiation Hardened
Quad Buffer, Three-State

September 1995

Features

- **3 Micron Radiation Hardened SOS CMOS**
- **Total Dose 200K RAD (Si)**
- **SEP Effective LET No Upsets: >100 MEV-cm^2/mg**
- **Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)**
- **Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s**
- **Dose Rate Upset >10^{10} RAD (Si)/s, 20ns Pulse**
- **Latch-Up Free Under Any Conditions**
- **Military Temperature Range: -55°C to +125°C**
- **Significant Power Reduction Compared to LSTTL ICs**
- **DC Operating Voltage Range: 4.5V to 5.5V**
- **Input Logic Levels**
  - **VIL = 30% of VCC Max**
  - **VIH = 70% of VCC Min**
- **Input Current Levels Ii ≤ 5µA at VOL, VOH**

Description

The Intersil HCS125MS is a Radiation Hardened quad three-state buffer, each having its own output enable input. A high level on the enable input puts the output in a high impedance state.

The HCS125MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

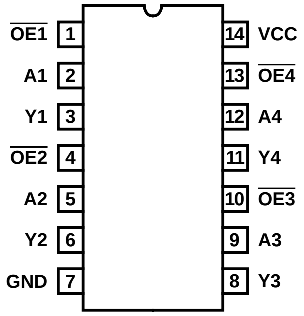
The HCS125MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Ordering Information

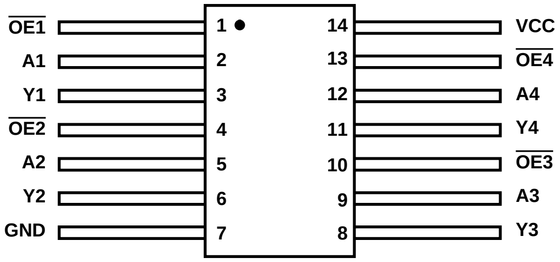
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS125DMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead SBDIP
HCS125KMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead Ceramic Flatpack
HCS125D/ Sample	+25°C	Sample	14 Lead SBDIP
HCS125K/ Sample	+25°C	Sample	14 Lead Ceramic Flatpack
HCS125HMSR	+25°C	Die	Die

Pinouts

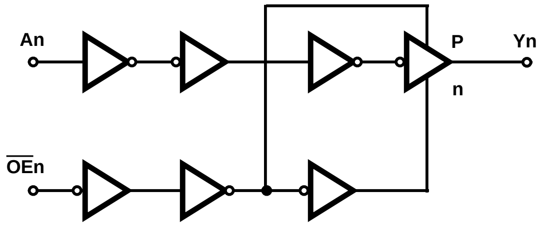
14 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T14, LEAD FINISH C
TOP VIEW



14 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP3-F14, LEAD FINISH C
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT
An	$\overline{\text{OEn}}$	Yn
H	L	H
L	L	L
X	H	Z

L = Low, H = High, X = Don't Care, Z = High Impedance

Absolute Maximum Ratings

Supply Voltage . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±35mA
Storage Temperature Range (TSTG) . . . . -65^{o}C to +150^{o}C
Lead Temperature (Soldering 10sec) . . . . +265^{o}C
Junction Temperature (TJ) . . . . +175^{o}C
ESD Classification . . . . Class 1
(All Voltage Reference to the VSS Terminal)

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package.	74^{o}C/W	24^{o}C/W
Ceramic Flatpack Package	116^{o}C/W	30^{o}C/W

Maximum Package Power Dissipation at +125^{o}C Ambient
SBDIP Package. 0.68W
Ceramic Flatpack Package 0.43W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:

SBDIP Package. . . . . 13.5mW/^{o}C
Ceramic Flatpack Package . . . . 8.6mW/^{o}C
Gate Count . . . . 20 Gates

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage Range . . . . +4.5V to +5.5V
Input Rise and Fall Time at 4.5V VCC (tr, tf) . . . . 100ns/V Max.
Operating Temperature Range. . . . . -55^{o}C to +125^{o}C
Input High Voltage. . . . . VCC to 70% of VCC
Input Low Voltage . . . . .0V to 30% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25^{o}C	-	40	µA
			2, 3	+125^{o}C, -55^{o}C	-	750	µA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V, (Note 2)	1	+25^{o}C	-7.2	-	mA
			2, 3	+125^{o}C, -55^{o}C	-6.0	-	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V, (Note 2)	1	+25^{o}C	7.2	-	mA
			2, 3	+125^{o}C, -55^{o}C	6.0	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25^{o}C	-	±0.5	µA
			2, 3	+125^{o}C, -55^{o}C	-	±5.0	µA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25^{o}C	-	±1.0	µA
			2, 3	+125^{o}C, -55^{o}C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 3)	7, 8A, 8B	+25^{o}C, +125^{o}C, -55^{o}C	-	-	V

NOTES:

1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Input to Y	TPHL TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25^{o}C	2	21	ns
			10, 11	+125^{o}C, -55^{o}C	2	25	ns
Enable Delay $\overline{OE}$ toY	TPZL TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25^{o}C	2	25	ns
			10, 11	+125^{o}C, -55^{o}C	2	30	ns
Disable Delay $\overline{OE}$ toY	TPLZ TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25^{o}C	2	25	ns
			10, 11	+125^{o}C, -55^{o}C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25^{o}C	-	60	pF
			1	+125^{o}C, -55^{o}C	-	90	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25^{o}C	-	10	pF
			1	+125^{o}C, -55^{o}C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25^{o}C	1	20	pF
			1	+125^{o}C, -55^{o}C	1	20	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25^{o}C	1	15	ns
			1	+125^{o}C, -55^{o}C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25^{o}C	-	0.75	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0	+25^{o}C	-6.0	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25^{o}C	6.0	-	mA

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 2)	+25°C	-	-	V
Propagation Delay Input to Y	TPHL TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	25	ns
Enable Delay $\overline{OE}$ to Y	TPZL TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	30	ns
Disable Delay $\overline{OE}$ to Y	TPLZ TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	+12µA
IOL/IOH	5	−15% of 0 Hour
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% go/no-go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC II BURN-IN (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

1. Each pin except VCC and GND will have a series resistor of 10K ± 5%.
2. Each pin except VCC and GND will have a series resistor of 1K ± 5%.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - ‘MS’

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

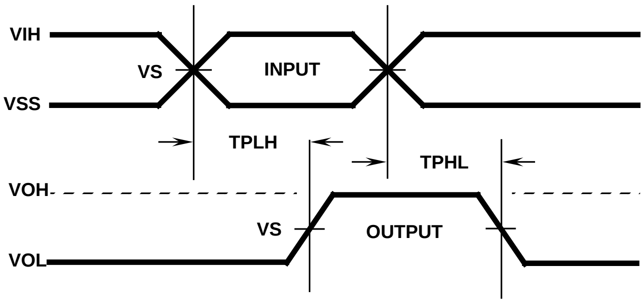
Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

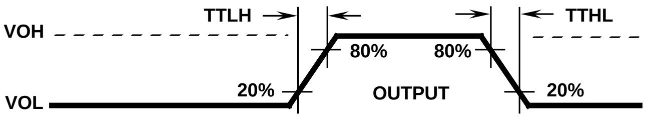
NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Propagation Delay Timing Diagram



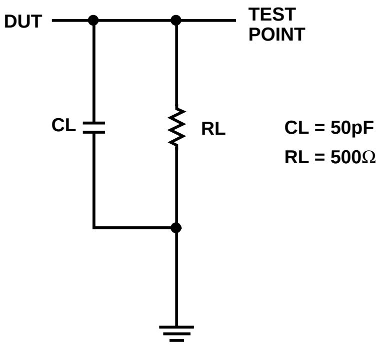
Transition Timing Diagram



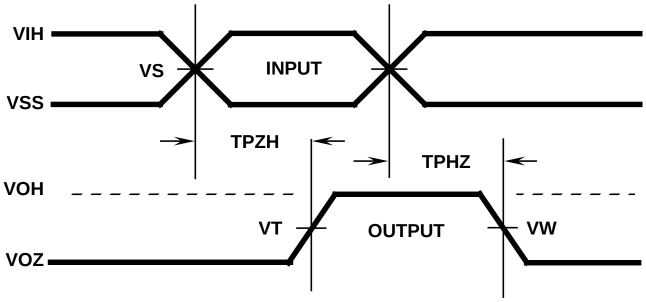
VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Propagation Delay Load Circuit



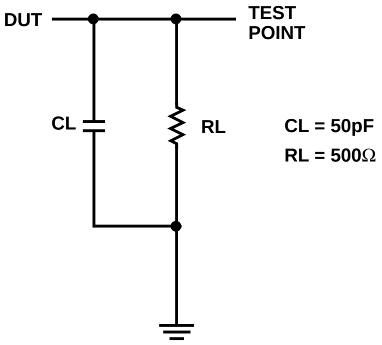
Three-State High Timing Diagrams



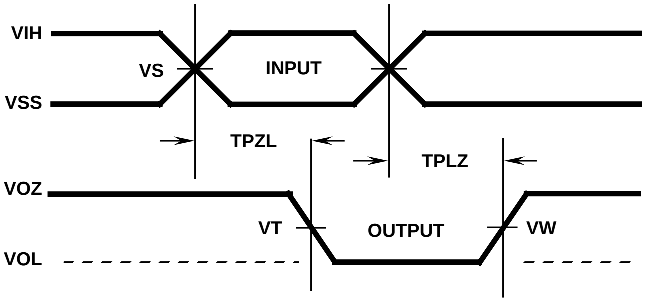
THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Three-State High Load Circuit



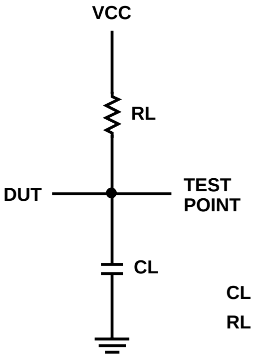
Three-State Low Timing Diagrams



THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Three-State Low Load Circuit



CL = 50pF
RL = 500Ω

Die Characteristics

DIE DIMENSIONS:

92 x 91(mils)
2.34 x 2.31 (mm)

METALLIZATION:

Type: AlSi
Thickness: 11kÅ ±1kÅ

GLASSIVATION:

Type: SiO_2
Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5$ A/cm^2

BOND PAD SIZE:

4 x 4 (mils)
100 x 100 (µm)

Metallization Mask Layout

HCS125MS