HCS241MS

Radiation Hardened Inverting Octal Three-State Buffer/Line Driver

September 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Dose Rate Upset >10^{10} RAD (Si)/Sec. 20ns Pulse
- Latch Up Free Under Any Conditions
- Military Temperature Range: -55^{o}C to +125^{o}C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% VCC Max
  - VIH = 70% VCC Min
- Input Compatibility Levels Ii ≤ 5μA at VOL, VOH

Description

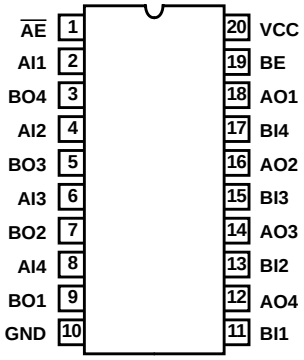
The Intersil HCS241MS is a Radiation Hardened inverting octal three-state buffer/line driver with two output enables, one active low, and one active high.

The HCS241MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

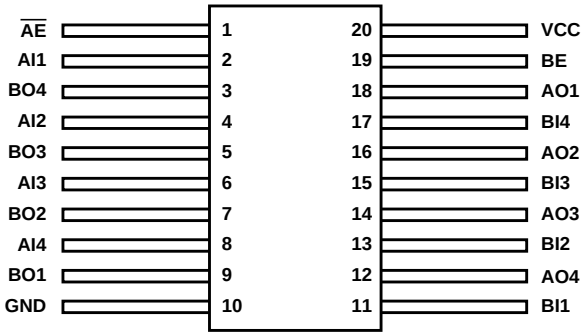
The HCS241MS is supplied in a 20 lead ceramic flatpack (K suffix) or a SBDIP package (D suffix).

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T20, LEAD FINISH C
TOP VIEW



20 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F20, LEAD FINISH C
TOP VIEW

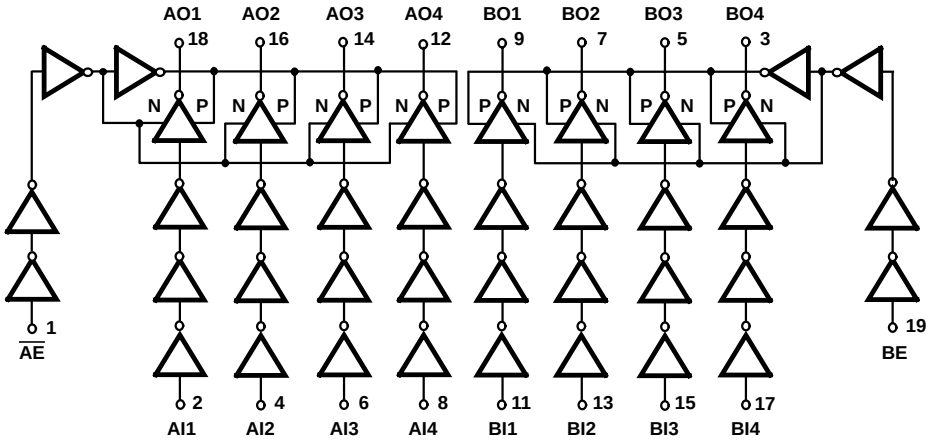


Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS241DMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	20 Lead SBDIP
HCS241KMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	20 Lead Ceramic Flatpack
HCS241D/Sample	+25^{o}C	Sample	20 Lead SBDIP
HCS241K/Sample	+25^{o}C	Sample	20 Lead Ceramic Flatpack
HCS241HMSR	+25^{o}C	Die	Die

Spec Number **518838**
File Number **3122.1**

Functional Diagram



TRUTH TABLE

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{AE}$	AIn	AOn	BE	BIn	BOn
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±35mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10 sec) . . . . . $+265^oC$
Junction Temperature (TJ) . . . . . $+175^oC$
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	$72^oC/W$	$24^oC/W$
Ceramic Flatpack Package	$107^oC/W$	$28^oC/W$

Maximum Package Power Dissipation at $+125^oC$ Ambient
SBDIP Package. 0.69W
Ceramic Flatpack Package 0.47W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package. . . . . $13.9mW/^oC$
Ceramic Flatpack Package . . . . . $9.3mW/^oC$
Gate Count . . . . . 40 Gates

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 100ns/V Max
Operating Temperature Range (T_A) . . . . . -55^oC to $+125^oC$
Input Low Voltage (VIL). . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . VCC to 70% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	40	µA
			2, 3	$+125^oC$, -55^oC	-	750	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0 (Note 2)	1	$+25^oC$	7.2	-	mA
			2, 3	$+125^oC$, -55^oC	6.0	-	
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0 (Note 2)	1	$+25^oC$	-7.2	-	mA
			2, 3	$+125^oC$, -55^oC	-6.0	-	
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC-0.1	-	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.35V, IOH = -50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V VIN = VCC or GND	1	$+25^oC$	-	±0.5	µA
			2, 3	$+125^oC$, -55^oC	-	±5.0	
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	$+25^oC$	-	±1.0	µA
			2, 3	$+125^oC$, -55^oC	-	±50	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V (Note 3)	7, 8A, 8B	$+25^oC$, $+125^oC$, -55^oC	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Force/Measure function may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	25	
Propagation Delay	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	25	
Propagation Delay	TPZL1 TPZL2	VCC = 4.5V, VIH = 4.5V, VIL = 0	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	
Propagation Delay	TPLZ1 TPLZ2	VCC = 4.5V, VIH = 4.5V, VIL = 0	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	
Propagation Delay	TPZH1 TPZH2	VCC = 4.5V, VIH = 4.5V, VIL = 0	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	24	
Propagation Delay	TPHZ1 TPHZ2	VCC = 4.5V, VIH = 4.5V, VIL = 0	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	

NOTES:

1. All voltage referenced to GND.
2. Measurements made with CL = 50pF, RL = 500Ω, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	36	pF
			1	+125°C, -55°C	-	59	pF
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	20	pF
			1	+125°C, -55°C	-	20	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VIN = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	6	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-6	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA		-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA		VCC-0.1	-	V
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±50	µA
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Noise Immunity Functional	FN	VCC = 4.5V, VIL = 3.15V, VIH = 1.35V, (Note 2)	+25°C	-	-	-
Propagation Delay	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	25	ns
	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	25	ns
	TPZL1 TPZL2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	30	ns
	TPLZ1 TPLZ2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	30	ns
	TPZH1 TPZH2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	24	ns
	TPHZ1 TPHZ2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	+12µA
IOL/IOH	5	-15% of 0 Hour
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 1)					
-	1, 10	3, 5, 7, 9, 12, 14, 16, 18	19, 20	2, 4, 6, 8, 11, 13, 15, 17	-

NOTES:

1. Each pin except VCC and GND will have a series resistor of 10KΩ ± 5%.
2. Each pin except VCC and GND will have a series resistor of 680Ω ± 5%

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20

NOTE: Each pin except VCC and GND will have a series resistor of 47KΩ ± 5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125^{o}C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

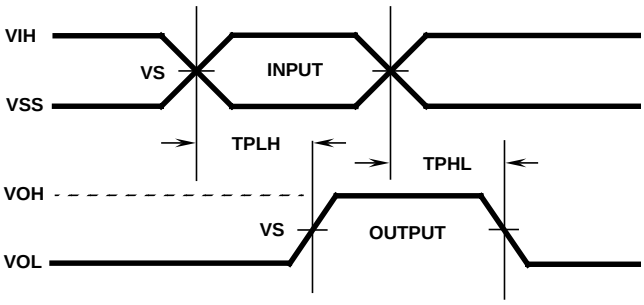
Sales Office Headquarters

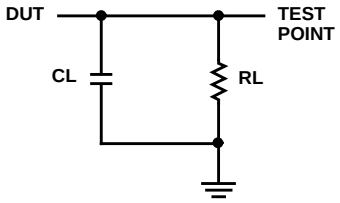
NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Propagation Delay Timing Diagram and Load Circuit

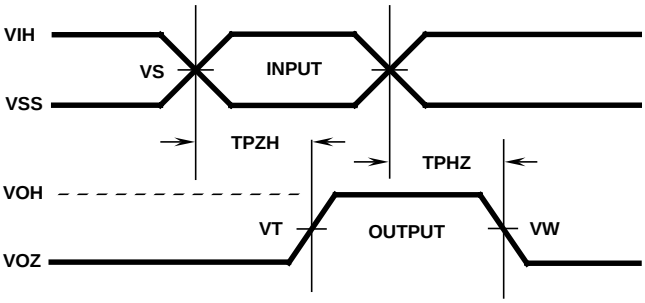


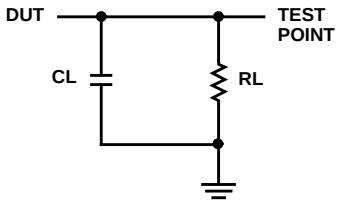


AC VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	4.50	V
VIL	0.0	V
VS	2.25	V
GND	0.00	V

Three-State High Timing Diagram and Load Circuit

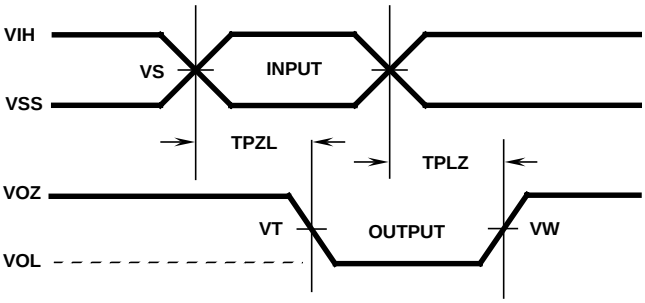


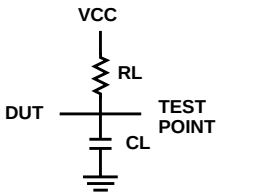


THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0.00	V

Three-State Low Timing Diagram and Load Circuit





THREE-STATE LOW VOLTAGE LEVELS

1	8	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0.00	V

Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness:13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
< 2.0 x 10^5A/cm^2

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS241MS