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# X1243

## 16K (2K x 8), 2-Wire RTC

April 28, 2005 FN8249.0

## Real Time Clock/Calendar/Alarm with EEPROM

### Features

- 2 alarms—interrupt output
  - Settable on the second, 10s of seconds, minute, 10s of minutes, hour, day, month, or day of the week
  - Repeat alarm for time base generation
- 2-wire interface interoperable with $I^2C$
  - 400kHz data transfer rate
- Secondary power supply input with internal switch-over circuitry
- 2Kbytes of EEPROM
  - 64-byte page write mode
  - 3-bit Block Lock™ protection
- Low power CMOS
  - <1µA operating current
  - <3mA active current during program
  - <400µA active current during data read
- Single byte write capability
- Typical nonvolatile write cycle time: 5ms
- High reliability
- Small package options
  - 8-lead SOIC package, 8-lead TSSOP package

### Description

The X1243 is a Real Time Clock with clock/calendar circuits and two alarms. The dual port clock and alarm registers allow the clock to operate, without loss of accuracy, even during read and write operations.

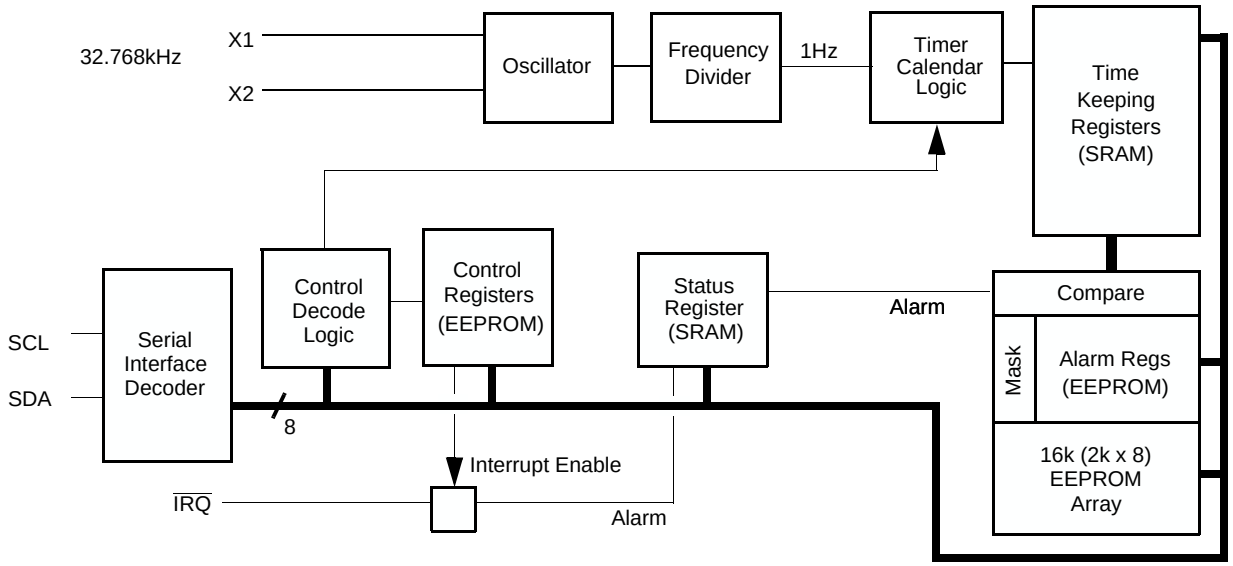
The clock/calendar provides functionality that is con-trollable and readable through a set of registers. The clock, using a low cost 32.768kHz crystal input, accu-rately tracks the time in seconds, minutes, hours, date, day, month and years. It has leap year correction and automatic adjustment for months with less than 31 days.

An alarm match of the RTC sets an interrupt ag and activates an interrupt pin. An alternative alarm function provides a pulsed interrupt for long time constant time-bases.

The device offers a backup power input pin. This $V_{BACK}$ pin allows the device to be backed up by a non-rechargeable battery. The RTC is fully operational from 1.8 to 5.5 volts.

The X1243 provides a 2Kbyte EEPROM array, giving a safe, secure memory for critical user and conguration data. This memory is unaffected by complete failure of the main and backup supplies.

### Block Diagram



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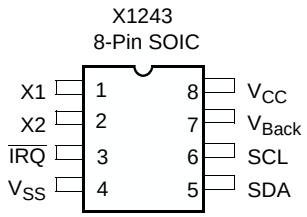
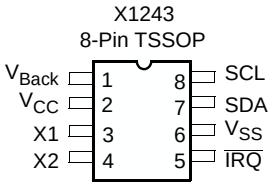
## Pin Configuration




## Pin Descriptions

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated).

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs.The input buffer is always active (not gated).

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz 2-wire inter-face speeds.

### $V_{BACK}$

This input provides a backup supply voltage to the device. $V_{BACK}$ supplies power to the device in the event the $V_{CC}$ supply fails.

## Interrupt Output—IRQ

This is an interrupt signal output. This signal noties a host processor that alarm has occurred and requests action. It is an open drain active LOW output.

### X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplier that can be con-gured for use as an on-chip oscillator. A 32.768kHz quartz crystal is used. Recommended crystal is a Citizen CFS-206. The crystal supplies a timebase for a clock/ oscillator. The internal clock can be driven by an external signal on X1, with X2 left unconnected.

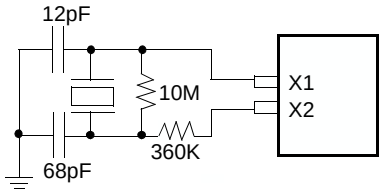



**FIGURE 1. RECOMMENDED CRYSTAL CONNECTION**

## Power Control Operation

The Power control circuit accepts a $V_{CC}$ and a $V_{BACK}$ input. The power control circuit will switch to $V_{BACK}$ when $V_{CC} < V_{BACK} – 0.2V$. It will switch back to $V_{CC}$ when $V_{CC}$ exceeds $V_{BACK}$.

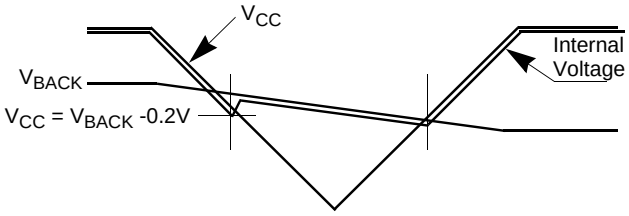



**FIGURE 2. POWER CONTROL**

## Real Time Clock Operation

The Real Time Clock (RTC) uses an external, 32.768kHz quartz crystal to maintain an accurate internal repre-sentation of the year, month, day, date, hour, minute, and seconds. The RTC has leap-year correction and a century byte. The clock will also correct for months hav-ing fewer than 31 days and will have a bit that controls 24-hour or AM/PM format. When the X1243 powers up after the loss of both $V_{CC}$ and $V_{BACK}$, the clock will not increment until at least one byte is written to the clock register.

### Reading the Real Time Clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the Real Time Clock. The RTC Registers can then be read in a Sequential Read Mode. Since the clock runs continuously and a read takes a nite amount of time, there is the possibility that the clock could change dur-ing the course of a read operation. In this device, the time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

### Writing to the Real Time Clock

The time and date may be set by writing to the RTC registers. To avoid changing the current time by an uncompleted write operation, the current time value is loaded into a separate buffer at the falling edge of the clock on the ACK bit before the RTC data input bytes, the clock continues to run. The new serial input data replaces the values in the buffer. This new RTC value is loaded back into the RTC Register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation the RTC will reect the newly loaded data beginning with the rst “one second” clock cycle after the stop bit. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any nonvolatile write sequences. A single byte may be written to the RTC without affect-ing the other bytes.

## Clock/Control Registers (CCR)

The Control/Clock Registers are located in an area log-ically separated from the array and are only accessible following a slave byte of “1101111x” and reads or writes to addresses [0000h:003Fh].

### CCR Access

The contents of the CCR can be modied by performing a byte or a page write operation directly to any address in the CCR. Prior to writing to the CCR (except the status register), however, the WEL and RWEL bits must be set using a two step process (See section “Writing to the Clock/Control Registers.”)

The CCR is divided into 5 sections.These are:

1. Alarm 0 (8 bytes)
2. Alarm 1 (8 bytes)
3. Control (2 bytes)
4. Real Time Clock (8 bytes)
5. Status (1 byte)

Sections 1) through 3) are nonvolatile and Sections 4) and 5) are volatile. Each register is read and written through buffers. The nonvolatile portion (or the counter portion of the RTC) is updated only if RWEL is set and only after a valid write operation and stop bit. A sequential read or page write operation provides access to the contents of only one section of the CCR per operation. Access to another section requires a new operation. Continued reads or writes, once reaching the end of a section, will wrap around to the start of the section. A read or page write can begin at any address in the CCR.

Section 5) is a volatile register. It is not necessary to set the RWEL bit prior to writing the status register. Section 5) supports a single byte read or write only. Continued reads or writes from this section terminates the operation.

The state of the CCR can be read by performing a ran-dom read at any address in the CCR at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. The read instruction latches all Clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read of the CCR will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read of the CCR, the address remains at the previous address +1 so the user can execute a current address read of the CCR and continue reading the next Register.

## Alarm Registers

There are two alarm registers whose contents mimic the contents of the RTC register, but add enable bits and exclude the 24-hour time selection bit. The enable bits specify which registers to use in the comparison between the Alarm and Real Time Registers. For example:

- The user can set the X1242 to alarm every Wednes-day at 8:00AM by setting the EDWn, the EHRn and EMNn enable bits to ‘0’ and setting the DWAn, HRAn and MNAn Alarm registers to 8:00AM Wednesday.
- A daily alarm for 9:30PM results when the EHRn and EMNn enable bits are set to ‘0’ and the HRAn and MNAn registers set 9:30PM.
- Setting the EMOn bit in combination with other enable bits and a specic alarm time, the user can establish an alarm that triggers at the same time once a year.

When there is a match, an alarm ag is set. The occur-rence of an alarm can be determined by polling the AL0 and AL1 bits, or by setting the AL0E and AL1E bits to ‘1’ and monitoring the IRQ output. The AL0E and AL1E bits enable the circuit that triggers the output IRQ pin when an alarm occurs. Writing a ‘0’ to one of the bits disables the output IRQ for that alarm condition, The alarm enable bits are located in the MSB of the but the alarm condition can still be checked by polling particular register. When all enable bits are set to ‘0’, the alarm ag. there are no alarms.

**TABLE 1. CLOCK/CONTROL MEMORY MAP**

| ADDR. | TYPE | REG NAME | BIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 OPTIONAL | RANGE | FACTORY SETTINGS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 003F | Status | SR | BAT | AL1 | AL0 | 0 | 0 | RWEL | WEL | RTCF | | 01h |
| 0037 | RTC (SRAM) | Y2K | 0 | 0 | Y2K21 | Y2K20 | Y2K13 | 0 | 0 | Y2K10 | 19/20 | 20h |
| 0036 | | DW | 0 | 0 | 0 | 0 | 0 | DY2 | DY1 | DY0 | 0-6 | 00h |
| 0035 | | YR | Y23 | Y22 | Y21 | Y20 | Y13 | Y12 | Y11 | Y10 | 0-99 | 00h |
| 0034 | | MO | 0 | 0 | 0 | G20 | G13 | G12 | G11 | G10 | 1-12 | 00h |
| 0033 | | DT | 0 | 0 | D21 | D20 | D13 | D12 | D11 | D10 | 1-31 | 00h |
| 0032 | | HR | T24 | 0 | H21 | H20 | H13 | H12 | H11 | H10 | 0-23 | 00h |
| 0031 | | MN | 0 | M22 | M21 | M20 | M13 | M12 | M11 | M10 | 0-59 | 00h |
| 0030 | | SC | 0 | S22 | S21 | S20 | S13 | S12 | S11 | S10 | 0-59 | 00h |
| 0011 | Control (EEPROM) | INT | IM | AL1E | AL0E | 0 | 0 | 0 | 0 | 0 | | 00h |
| 0010 | | BL | BP2 | BP1 | BP0 | 0 | 0 | 0 | 0 | 0 | | 00h |
| 000F | Alarm1 (EEPROM) | | unused | | | | | | | | | |
| 000E | | DWA1 | EDW1 | 0 | 0 | 0 | 0 | DY2 | DY1 | DY0 | 0-6 | 00h |
| 000D | | YRA1 | Unused - Default = RTC Year value | | | | | | | | | |
| 000C | | MOA1 | EMO1 | 0 | 0 | A1G20 | A1G13 | A1G12 | A1G11 | A1G10 | 1-12 | 00h |
| 000B | | DTA1 | EDT1 | 0 | A1D21 | A1D20 | A1D13 | A1D12 | A1D11 | A1D10 | 1-31 | 00h |
| 000A | | HRA1 | EHR1 | 0 | A1H21 | A1H20 | A1H13 | A1H12 | A1H11 | A1H10 | 0-23 | 00h |
| 0009 | | MNA1 | EMN1 | A1M22 | A1M21 | A1M20 | A1M13 | A1M12 | A1M11 | A1M10 | 0-59 | 00h |
| 0008 | | SCA1 | ESC1 | A1S22 | A1S21 | A1S20 | A1S13 | A1S12 | A1S11 | A1S10 | 0-59 | 00h |
| 0007 | Alarm0 (EEPROM) | | unused | | | | | | | | | |
| 0006 | | DWA1 | EDW0 | 0 | 0 | 0 | 0 | DY2 | DY1 | DY0 | 0-6 | 00h |
| 0005 | | YRA0 | Unused - Default = RTC Year value | | | | | | | | | |
| 0004 | | MOA0 | EMO0 | 0 | 0 | A0G20 | A0G13 | A0G12 | A0G11 | A0G10 | 1-12 | 00h |
| 0003 | | DTA0 | EDT0 | 0 | A0D21 | A0D20 | A0D13 | A0D12 | A0D11 | A0D10 | 1-31 | 00h |
| 0002 | | HRA0 | EHR0 | 0 | A0H21 | A0H20 | A0H13 | A0H12 | A0H11 | A0H10 | 0-23 | 00h |
| 0001 | | MNA0 | EMN0 | A0M22 | A0M21 | A0M20 | A0M13 | A0M12 | A0M11 | A0M10 | 0-59 | 00h |
| 0000 | | SCA0 | ESC0 | A0S22 | A0S21 | A0S20 | A0S13 | A0S12 | A0S11 | A0S10 | 0-59 | 00h |

## Real Time Clock Registers

### Year 2000 (Y2K)

The X1243 has a century byte that “rolls over” from 19 to 20 when the years byte changes from 99 to 00. The Y2K byte can contain only the values of 19 or 20.

### Day of the Week Register (DW)

This register provides a Day of the Week status and uses three bits DY2 to DY0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-... The assignment of a numerical value to a specic day of the week is arbitrary and may be decided by the system software designer. The Clock Default values dene 0 = Sunday.

### Clock/Calendar Registers (YR, MO, DT, HR, MN, SC)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 00 to 59, HR (Hour) is 1 to 12 with an AM or PM indicator (H21 bit) or 0 to 23 (with T24 = 1), DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (year) is 0 to 99.

### 24-Hour Time

If the T24 bit of the HR register is 1, the RTC will use a 24-hour format. If the T24 bit is 0, the RTC will use 12-hour format and bit H21 will function as an AM/PM indicator with a ‘1’ representing PM. The clock defaults to Standard Time with H21 = 0.

### Leap Years

Leap years add the day February 29 and are dened as those years that are divisible by 4.Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The X1243 does not correct for the leap year in the year 2100.

## Status Register (SR)

The Status Register is located in the RTC area at address 003FH. This is a volatile register only and is used to control the WEL and RWEL write enable latches, read an optional Low Voltage Sense bit, and read the two alarm bits. This register is logically sepa-rated from both the array and the Clock/Control Regis-ters (CCR).

**TABLE 2. STATUS REGISTER (SR)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 003Fh | BAT | AL1 | AL0 | 0 | 0 | RWEL | WEL | RTCF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

### BAT: Battery Supply—Volatile

This bit set to “1” indicates that the device is operating from $V_{BACK}$, not $V_{CC}$. It is a read only bit and is set/ reset by hardware.

### AL1, AL0: Alarm Bits (Volatile)

These bits announce if either alarm 1 or alarm 2 match the real time clock. If there is a match, the respective bit is set to ‘1’. The falling edge of the last data bit in a SR Read operation resets the ags.

NOTE: Only the AL bits that are set when an SR read starts will be reset. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

### RWEL: Register Write Enable Latch (Volatile)

This bit is a volatile latch that powers up in the LOW (disabled) state. The RWEL bit must be set to “1” prior to any writes to the Clock/Control Registers. Writes to RWEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition. A write to the CCR requires both the RWEL and WEL bits to be set in a specic sequence.

### WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the CCR and mem-ory array during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to the CCR or any array address will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the Sta-tus Register. Once set, WEL remains set until either reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the Status Register) or until the part powers up again. Writes to WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

### RTCF: Real Time Clock Fail Bit (Volatile)

This bit is set to a ‘1’ after a total power failure. This is a read only bit that is set by hardware when the device powers up after having lost all power to the device. The bit is set regardless of whether $V_{CC}$ or $V_{BACK}$ is applied rst. The loss of one or the other supplies does not result in setting the RTCF bit. The rst valid write to the RTC (writing one byte is sufcient) resets the RTCF bit to ‘0’.

### Unused Bits

These devices do not use bits 3 or 4, but must have a zero in these bit positions. The Data Byte output during a SR read will contain zeros in these bit locations.

## Control Registers

### Block Protect Bits—BP2, BP1, BP0 (Nonvolatile)

The Block Protect Bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block pro-tect bits will prevent write operations to one of eight segments of the array. The partitions are described in Table 3.

**TABLE 3. BLOCK PROTECT BITS**

| BP2 | BP1 | BP0 | PROTECTED ADDRESSES X1243 | ARRAY LOCK |
|---|---|---|---|---|
| 0 | 0 | 0 | None | None |
| 0 | 0 | 1 | 600h - 7FFh | Upper 1/4 |
| 0 | 1 | 0 | 400h - 7FFh | Upper 1/2 |
| 0 | 1 | 1 | 000h - 7FFh | Full Array |
| 1 | 0 | 0 | 000h - 03Fh | First Page |
| 1 | 0 | 1 | 000h - 07Fh | First 2 pgs |
| 1 | 1 | 0 | 000h - 0FFh | First 4 pgs |
| 1 | 1 | 1 | 000h - 1FFh | First 8 pgs |

### Interrupt Control Bits (AL1E, AL0E)

There are two Interrupt Control bits, Alarm 1 Interrupt Enable (AL1E) and Alarm 0 Interrupt Enable (AL0E) to specically enable or disable the alarm interrupt signal output. The interrupt output is enabled when either bit is set to ‘1’. Two volatile bits (AL1 and AL0), associated with these alarms, indicate if an alarm has happened. These bits are set on an alarm condition regardless of whether the alarm interrupts are enabled. The AL1 and AL0 bits are reset by the falling edge of the 8th clock of a read of the register containing the bits.

In an alternative mode (called pulsed interrupt mode), controlled by an interrupt mode (IM) bit, the alarm 0 setting provides an output pulse on IRQ each time the alarm matches the RTC. In this case the AL0 bit is not used. Alarm 1 works as before (i.e. the AL1 bit is set when an alarm occurs), but it is necessary to poll the sta-tus register to determine whether a match has occurred. This read operation is necessary to reset the AL1 ag.

### Normal Mode (IM Bit = 0)

A match of the RTC and the contents of the alarm 0 registers automatically sets the AL0 bit. If the AL0E bit is also set, the output IRQ signal goes active (LOW). If the AL0E bit is not set, the AL0 bit is set, but the IRQ signal remains unchanged.

A match of the RTC and the contents of the alarm 1 registers automatically sets the AL1 bit. If the AL1E bit is also set, the output IRQ signal goes active (LOW). If the AL1E bit is not set, the AL1 bit is set, but the IRQ signal remains unchanged.

Reading the status register, containing the AL0 and AL1 bits, resets the bits. The bits do not reset until the falling edge of the 8th output clock of the status register containing the Alarm bits. When the bits reset, the output IRQ signal returns to the inactive state.

### Pulsed Interrupt Mode (IM Bit = 1)

In this mode, the alarm interrupt enable bits (AL0E and AL1E) are not used. Alarm 1 operates as before, so a match of the RTC and Alarm 1 sets the AL1 bit. Since the interrupt enable bits have no function, it is neces-sary for the host processor to poll the AL1 bit to deter-mine if an alarm has occurred.

Alarm 0 provides an output response. In this case, when the RTC matches the Alarm 0 registers, the output IRQ pulses one time. This pulse can be used to control some outside circuit or event, without the need for a local processor. The duration of the pulse is 1024 cycles of the 32.748kHz oscillator. All alarm 0 enable options are available, so this becomes a very exible long term repeat trigger.

## Writing To The Clock/Control Registers

Changing any of the nonvolatile bits of the clock/control register requires the following steps:

- Write a 02H to the Status Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation pre-ceeded by a start and ended with a stop).
- Write a 06H to the Status Register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop).
- Write one to 8 bytes to the Clock/Control Registers with the desired clock, alarm, or control data. This sequence starts with a start bit, requires a slave byte of “11011110” and an address within the CCR and is terminated by a stop bit. A write to the CCR changes EEPROM values so these initiate a nonvolatile write cycle and will take up to 10ms to complete. Writes to undened areas have no effect. The RWEL bit is reset by the completion of a nonvolatile write write cycle, so the sequence must be repeated to again initiate another change to the CCR contents. If the sequence is not completed for any reason (by send-ing an incorrect number of bits or sending a start instead of a stop, for example) the RWEL bit is not reset and the device remains in an active mode.
- Writing all zeros to the status register resets both the WEL and RWEL bits.
- A read operation occurring between any of the previ-ous operations will not interrupt the register write operation.
- The RWEL and WEL bits can be reset by writing a 0 to the Status Register.

## Serial Communication

### Interface Conventions

The device supports a bidirectional bus oriented proto-col. The protocol denes any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

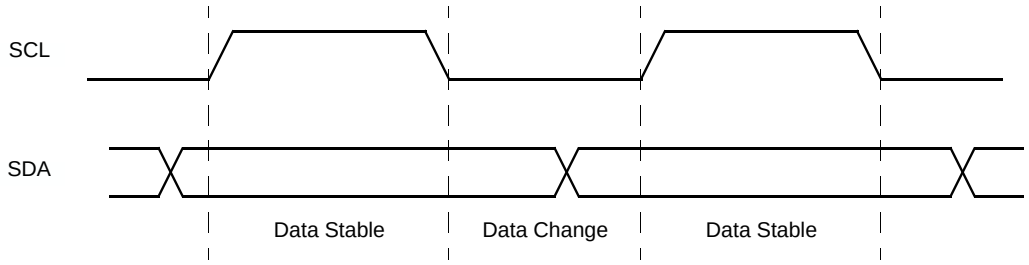



**FIGURE 3. VALID DATA CHANGES ON THE SDA BUS**

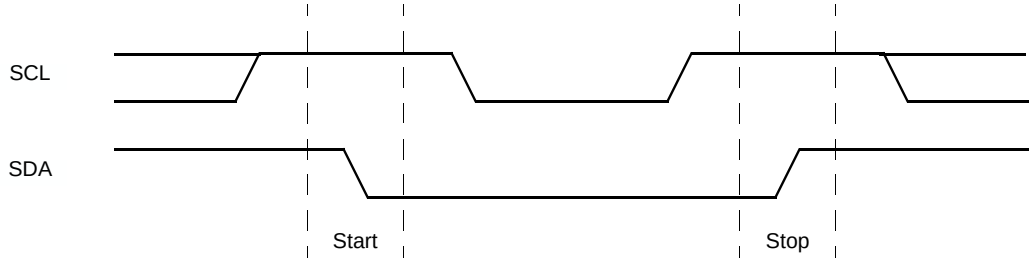



**FIGURE 4. VALID START AND STOP CONDITIONS**

### *Clock and Data*

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 3.

### *Start Condition*

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and

SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 4.

### *Stop Condition*

All communications must be terminated by a stop con-dition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus Refer to Figure 4.

### *Acknowledge*

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 5.

The device will respond with an acknowledge after rec-ognition of a start condition and if the correct Device Identier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for:

- The Slave Address Byte when the Device Identier and/or Select bits are incorrect
- All Data Bytes of a write when the WEL in the Write Protect Register is LOW
- The 2nd Data Byte of a Register Write Operation (when only 1 data byte is allowed)

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

## *Write Operations*

### *Byte Write*

For a byte write operation (Refer to Figure 13), the device requires the Slave Address Byte and the Word Address Bytes. This gives the master access to any one of the words in the array or CCR. (**Note:** Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in preceding operations to enable the write operation. See “Writing to the Clock/ Control Registers” on page 6.) Upon receipt of each address byte, the X1243 responds with an acknowl-edge. After receiving both address bytes the X1243 awaits the eight bits of data. After receiving the 8 data bits, the X1243 again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The X1243 then begins an internal write cycle of the data to the nonvolatile memory. Dur-ing the internal write cycle, the device inputs are dis-abled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 6.

A write to a protected block of memory is ignored, but will still receive an acknowledge. At the end of the write command, the X1243 will not initiate an internal write cycle, and will continue to ACK commands.

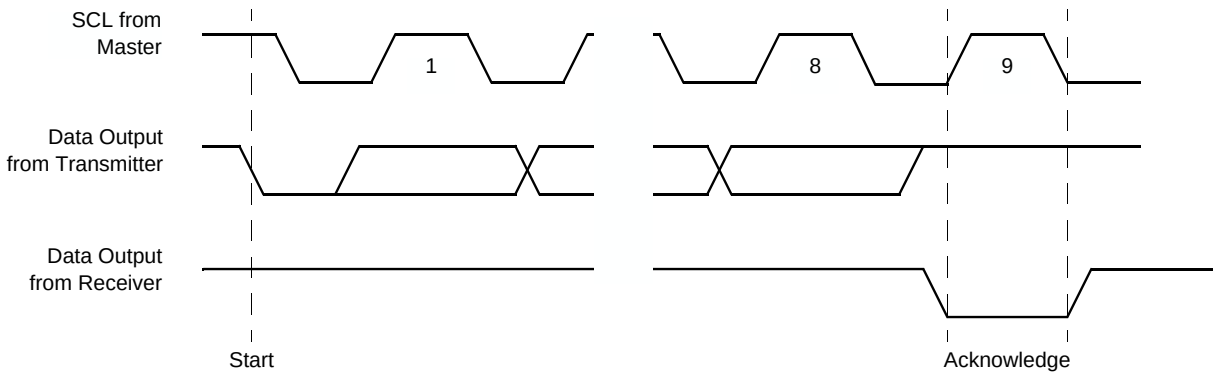



**FIGURE 5. ACKNOWLEDGE RESPONSE FROM RECEIVER**

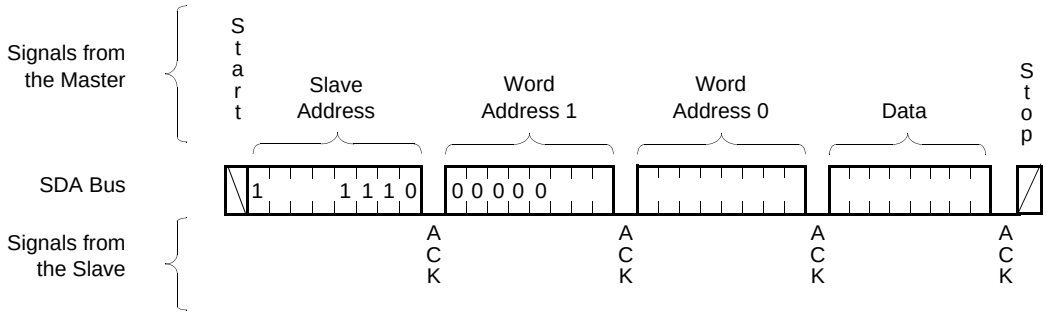



**FIGURE 6. BYTE WRITE SEQUENCE**

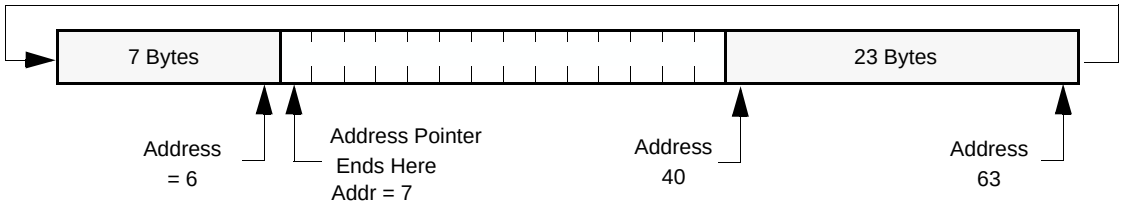



**FIGURE 7. WRITING 30 BYTES TO A 64-BYTE PAGE STARTING AT ADDRESS 40.**

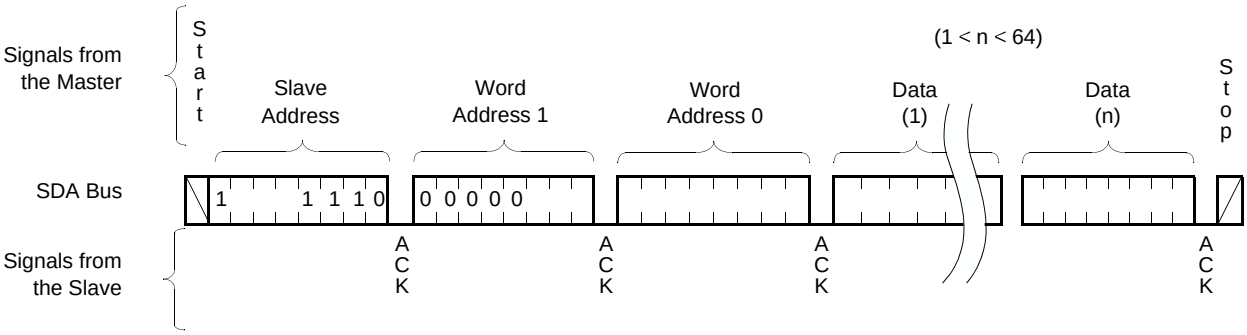



**FIGURE 8. PAGE WRITE SEQUENCE**

### Page Write

The X1243 has a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the rst data byte is transferred, the master can transmit up to 63 more bytes to the memory array and up to 7 more bytes to the clock/control registers.

(**Note:** Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two pre-ceding operations to enable the write operation. See “Writing to the Clock/Control Registers” on page 6.)

After the receipt of each byte, the X1243 responds with an acknowledge, and the address is internally incre-mented by one. When the counter reaches the end of the page, it “rolls over” and goes back to the rst address on the same page. This means that the mas-ter can write 64-bytes to a memory array page or 8-bytes to a CCR section starting at any location on that page. If the master begins writing at location 40 of the memory and loads 30 bytes, then the rst 23-bytes are written to addresses 40 through 63, and the last 7-bytes are written to columns 0 through 6. Afterwards, the address counter would point to location 7 on the page that was just written. If the master supplies more than the maximum bytes in a page, then the previously loaded data is over written by the new data, one byte at a time.

The master terminates the Data Byte loading by issu-ing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write oper-ation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 8 for the address, acknowledge, and data transfer sequence.

### Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it’s associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be affected.

### Acknowledge Polling

The disabling of the inputs during nonvolatile write cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master’s byte load operation, the device initiates the internal nonvolatile write cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the nonvolatile write cycle then no ACK will be returned. If the device has com-pleted the write operation, an ACK will be returned and the host can then proceed with the read or write opera-tion. Refer to the ow chart in Table 9.

## Read Operations

There are three basic read operations: Current Address Read, Random Read, and Sequential Read.

### Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incre-mented by one. Therefore, if the last read was to address n, the next read operation would access data from address n + 1. On power up, the sixteen bit address is initialized to 0h. In this way, a current address read can be initiated immediately after the power on reset to download the contents of memory starting at the rst location.

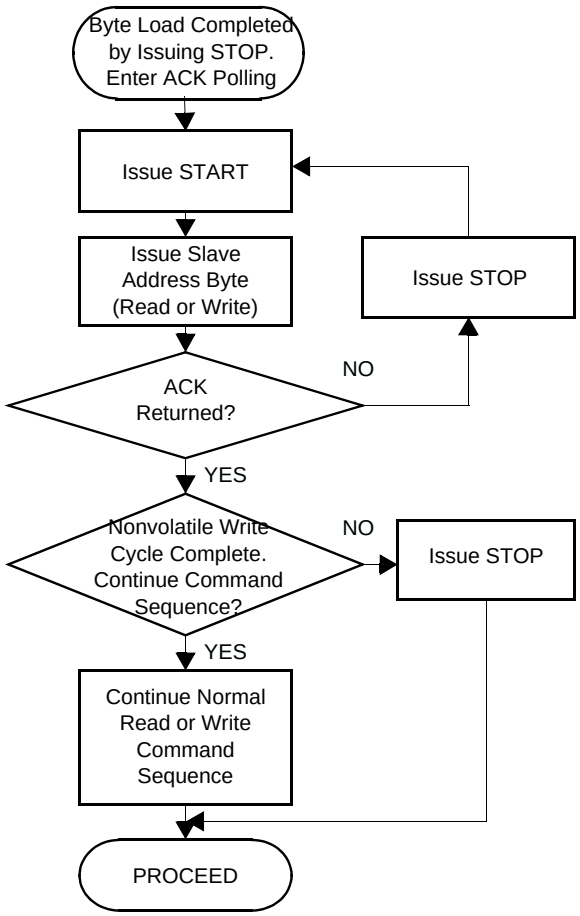



**FIGURE 9. ACKNOWLEDGE POLLING SEQUENCE**

Upon receipt of the Slave Address Byte with the R/W bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The mas-ter terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 10 for the address, acknowledge, and data transfer sequence.

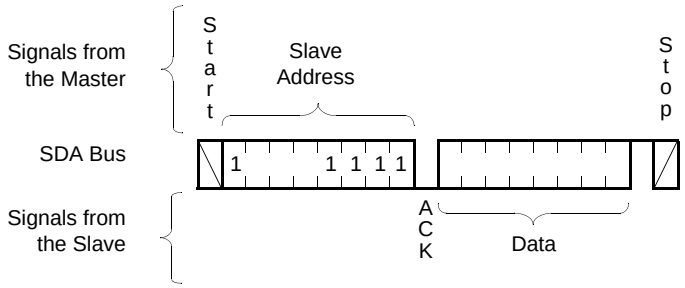



**FIGURE 10. CURRENT ADDRESS READ SEQUENCE**

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condi-tion during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

### *Random Read*

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/W bit set to one, the master must rst perform a “dummy” write operation.

The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/W bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 11 for the address, acknowledge, and data transfer sequence.

In a similar operation, called “Set Current Address,” the device sets the address if a stop is issued instead of the second start shown in Figure 11. The X1243 then goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Cur-rent Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

### *Sequential Read*

Sequential reads can be initiated as either a current address read or random address read. The rst Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicat-ing it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to the start of the address space and the device continues to output data for each acknowledge received. Refer to Figure 12 for the acknowledge and data transfer sequence.

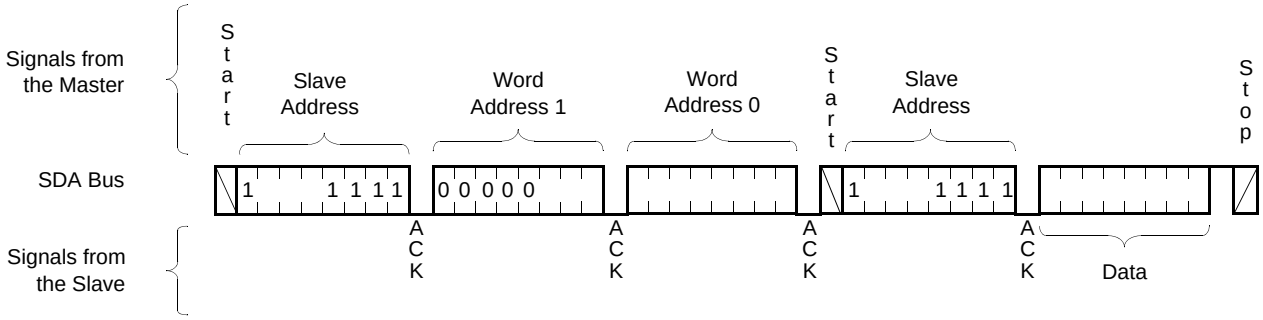



**FIGURE 11.** RANDOM ADDRESS READ

## Device Addressing

Following a start condition, the master must output a Slave Address Byte. The rst four bits of the Slave Address Byte specify access to the EEPROM array or to the CCR. Slave bits ‘1010’ access the EEPROM array. Slave bits ‘1101’ access the CCR.

Bit 3 through Bit 1 of the slave byte specify the device select bits.These are set to ‘111’.

The last bit of the Slave Address Byte denes the oper-ation to be performed. When this R/W bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 12.

After loading the entire Slave Address Byte from the SDA bus, the device compares the device identier and device select bits with ‘1010111’ or ‘1101111’. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a two byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power up the internal address counter is set to address 0h, so a current address read of the EEPROM array starts at address 0. When required, as part of a random read, the master device must supply the 2 Word Address Bytes.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. That is if the random read is from the array the slave byte must be ‘1010111x’ in both instances. Similarly, for a random read of the Clock/ Control Registers, the slave byte must be ‘1101111x’ in both places.

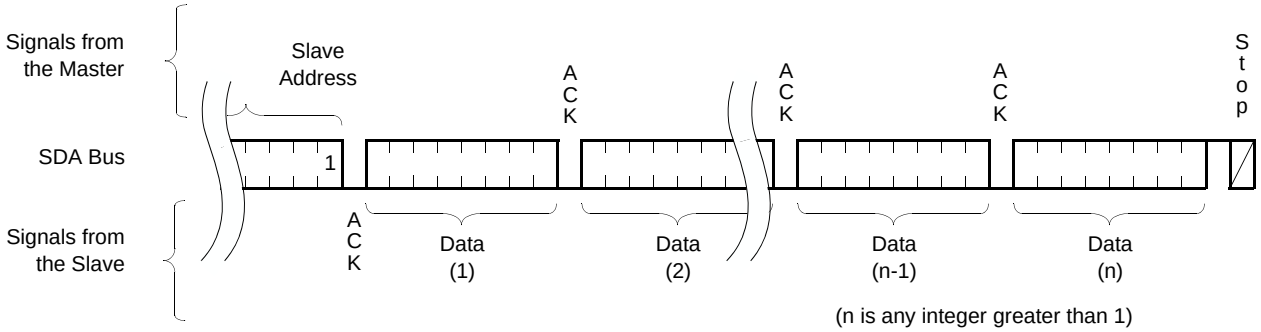



**FIGURE 12.** SEQUENTIAL READ SEQUENCE

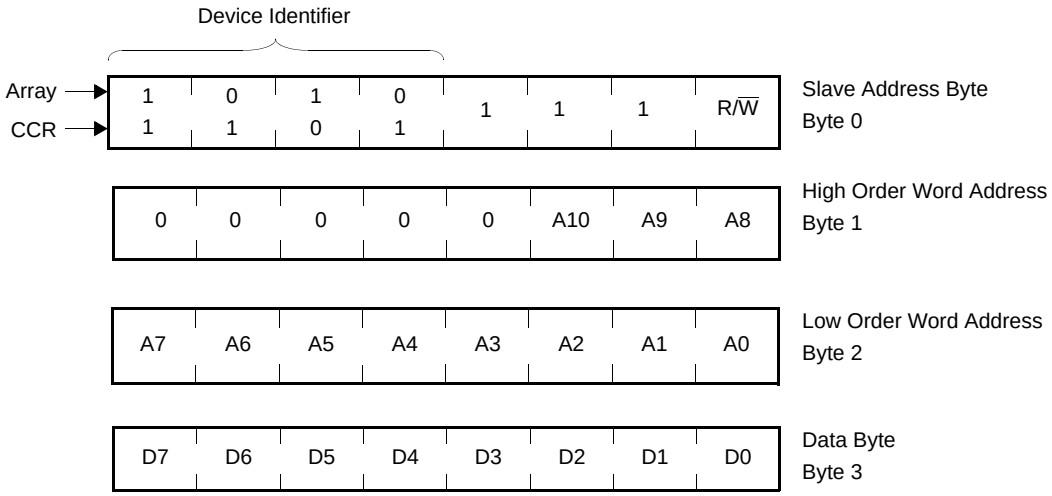



**FIGURE 13.** SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES (64-BYTE PAGES**)**

## ABSOLUTE MAXIMUM RATINGS COMMENT

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any pin
with respect to ground . . . . . -1.0V to 7.0V
DC output current. . . . . .5mA
Lead temperature (soldering, 10 seconds) . . . . . .300°C

*CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specifcation is not implied*

## DC OPERATING CHARACTERISTICS Temperature (-40°C to +85°C, unless otherwise stated.)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Main Power Supply | | 2.7 | | 5.5 | V | |
| $V_{BACK}$ | Backup Power Supply | | 1.8 | | 5.5 | V | |
| $V_{CB}$ | Switch to Backup Supply | | $V_{BACK}$ - 0.2 | | $V_{BACK}$ - 0.1 | V | 2 |
| $V_{BC}$ | Switch to Main Supply | | $V_{BACK}$ | | $V_{BACK}$ + 0.1 | | 2 |
| $I_{CC1}$ | Supply Current | $V_{CC}$ = 2.7V | | | 1.2 | µA | 3, 5, 10 |
| | | $V_{CC}$ = 5.5V | | | 1.7 | µA | |
| $I_{CC2}$ | Supply Current (External | $V_{CC}$ = 2.7V | | 3.8 | 5 | | 2, 3, 5, 11 |
| | crystal network) | $V_{CC}$ = 5.5V | | 7.5 | 15 | µA | |
| $I_{CC3}$ | Program Supply Current | $V_{CC}$ = 2.7V | | | 1.5 | µA | 1, 3, 5, 10 |
| | (nonvolatile) | $V_{CC}$ = 5.5V | | | 3.0 | µA | |
| $I_{BACK1}$ | Timekeeping Current | $V_{BACK}$ = 1.8V | | | 1.0 | µA | 2, 4, 6, 10 |
| | | $V_{BACK}$ = 5.5V | | | 1.5 | µA | |
| $I_{BACK2}$ | Timekeeping Current | $V_{BACK}$= 1.8V | | 1.6 | 3 | µA | 2, 4, 6, 11 |
| | (External crystal network) | $V_{BACK}$= 5.5V | | 7.5 | 15 | µA | |
| $I_{LI}$ | Input Leakage Current | | | | 10 | µA | 7 |
| $I_{LO}$ | Output Leakage Current | | | | 10 | µA | 7 |
| $V_{IL}$ | Input LOW Voltage | | -0.5 | | $V_{CC}$ x 0.3 or $V_{BACK}$ x 0.3 | V | 2, 9 |
| $V_{IH}$ | Input HIGH Voltage | | $V_{CC}$ x 0.7 or $V_{BACK}$ x 0.7 | | $V_{CC}$ + 0.5 $V_{BACK}$ + 0.5 | V | 2, 9 |
| $V_{OL}$ | Output LOW Voltage | 2.7V | | | 0.4 | V | 8 |
| | | 5.5V | | | 0.4 | | |

NOTES:

1. The device enters the Program state 200ns after a stop ending a write operation and continues for tWC.
2. Periodically sampled and not 100% tested.
3. $V_{IL}$ = $V_{CC}$ x 0.1, $V_{IH}$ = $V_{CC}$ x 0.9, $f_{SCL}$ = 400kHz, SDA = Open
4. $V_{CC}$ = 0V.
5. $V_{BACK}$= 0V.
6. $V_{SDA}$ = $V_{SCL}$ = $V_{BACK}$, Others = GND or $V_{BACK}$
7. $V_{SDA}$ = GND to $V_{CC}$, $V_{CLK}$ = GND or $V_{CC}$
8. IOL = 3.0mA at 5V, 1.5mA at 1.8V
9. Threshold voltages based on the higher of $V_{CC}$ or $V_{BACK}$.
10. Driven by external 32.768kHz square wave oscillator on X1, X2 open.
11. Using recommended crystal and oscillator network applied to X1 and X2 (25°C).

## Capacitance ($T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5V)

| SYMBOL | PARAMETER | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|
| $C_{OUT}$(1) | Output Capacitance (SDA, IRQ) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$(1) | Input Capacitance (SCL) | 6 | pF | $V_{IN}$ = 0V |

NOTE: This parameter is periodically sampled and not 100% tested.

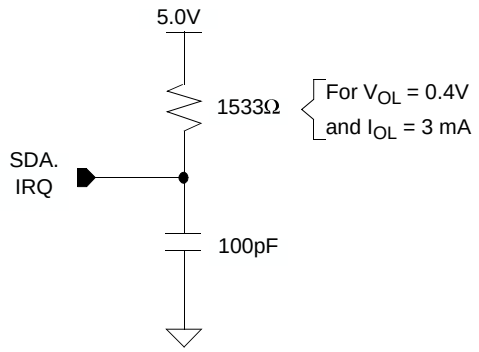
## AC Characteristics

### AC Test Conditions

| | |
|---|---|
| Input pulse levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing levels | $V_{CC}$ x 0.5 |
| Output load | Standard output load |

## Equivalent AC Output Load Circuit for $V_{CC}$ = 5V

### Standard Output Load for testing the device with $V_{CC}$ = 5.0V




## AC Specifications (TA = -40°C to +85°C, VCC = +2.7V to +5.5V, unless otherwise specied.)

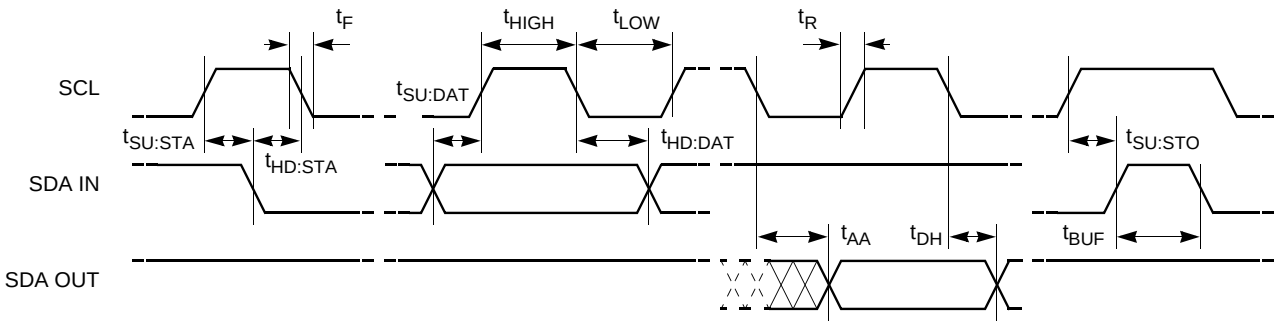
| SYMBOL | PARAMETER | 400kHz OPTION | | UNIT | |
|---|---|---|---|---|---|
| | | MIN | | | MAX |
| $f_{SCL}$ | SCL Clock Frequency | 0 | 400 | kHz | |
| $t_{IN}$(1) | Pulse width Suppression Time at inputs | 50 | | ns | |
| $t_{AA}$ | SCL LOW to SDA Data Out Valid | 0.1 | 0.9 | µs | |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start | 1.3 | | µs | |
| $t_{LOW}$ | Clock LOW Time | 1.3 | | µs | |
| $t_{HIGH}$ | Clock HIGH Time | 0.6 | | µs | |
| $t_{SU:STA}$ | Start Condition Setup Time | 0.6 | | µs | |
| $t_{HD:STA}$ | Start Condition Hold Time | 0.6 | | µs | |
| $t_{SU:DAT}$ | Data In Setup Time | 100 | | ns | |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | µs | |
| $t_{SU:STO}$ | Stop Condition Setup Time | 0.6 | | µs | |
| $t_{DH}$ | Data Output Hold Time | 50 | | ns | |
| $t_R$(1) | SDA and SCL Rise Time | 20 + .1Cb(2) | 300 | ns | |
| $t_F$(1) | SDA and SCL Fall Time | 20 + .1Cb(2) | 300 | ns | |
| Cb | Capacitive load for each bus line | | 400 | pF | |

NOTES:

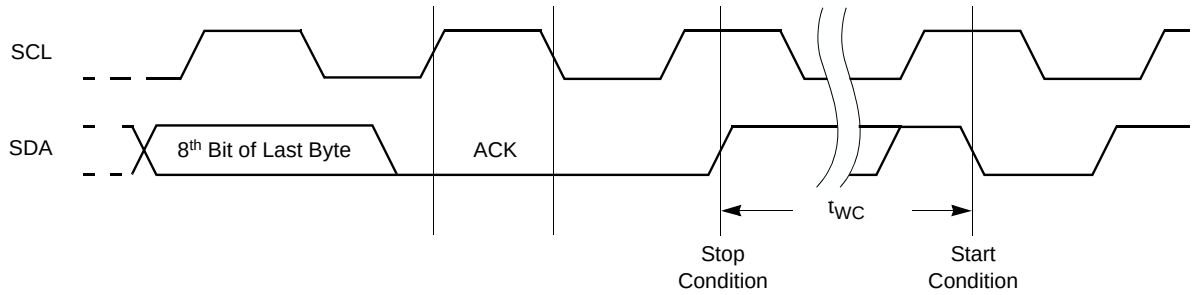
1. This parameter is periodically sampled and not 100% tested.
2. (Cb = total capacitance of one bus line in pF.

## Timing Diagrams

### Bus Timing




### Write Cycle Timing




### Power Up Timing

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $t_{PUR}$(1) | Time from Power Up to Read | | 1 | ms |
| $t_{PUW}$(1) | Time from Power Up to Write | | 5 | ms |

NOTE: Delays are measured from the time VCC is stable until the specied operation can be initiated. These parameters are periodically sampled and not 100% tested.

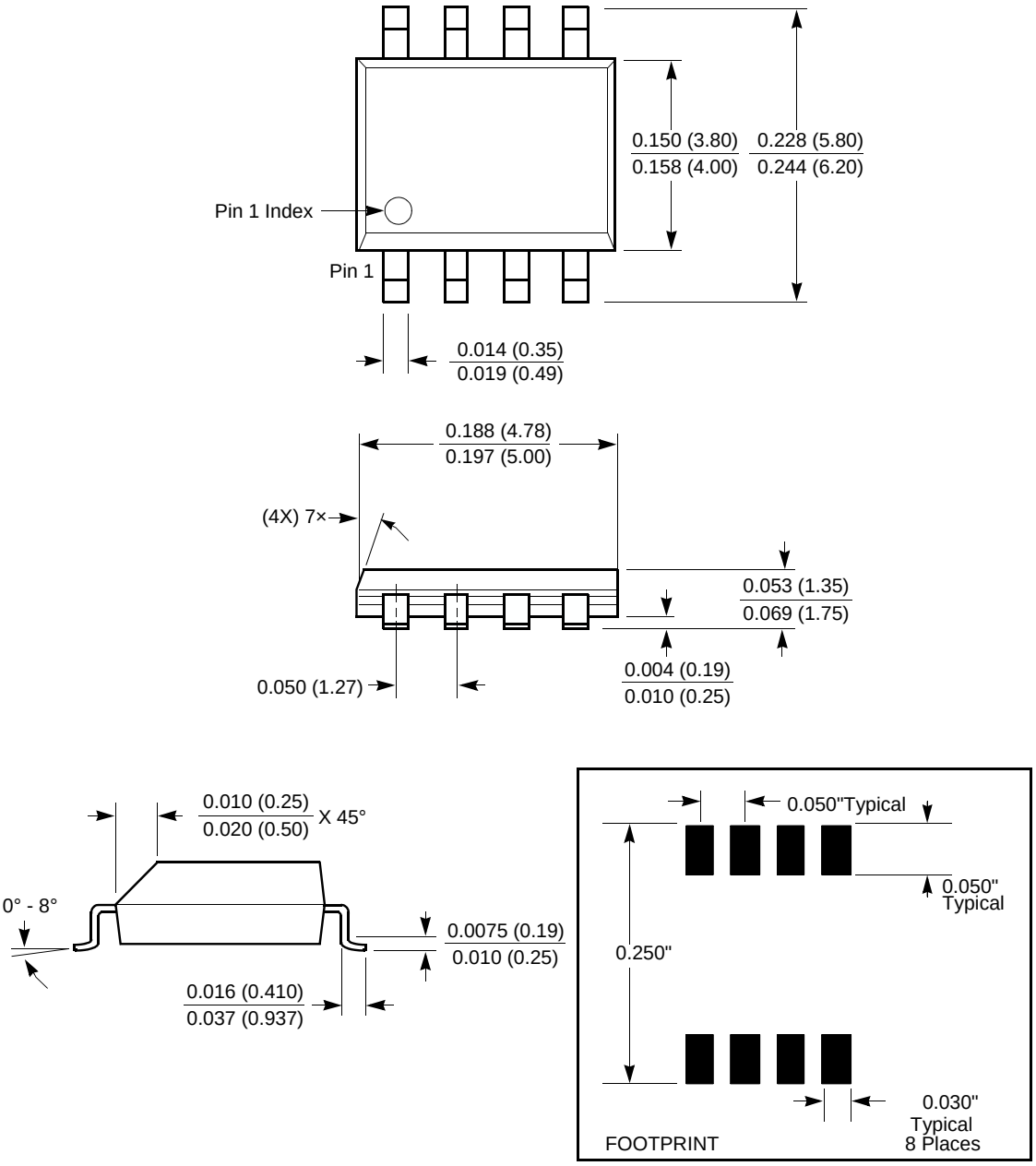
### Nonvolatile Write Cycle Timing

| SYMBOL | PARAMETER | MIN. | TYP.(1) | MAX. | UNIT |
|---|---|---|---|---|---|
| $t_{WC}$(1) | Write Cycle Time | | 5 | 10 | ms |

NOTE: tWC is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

## Packaging Information

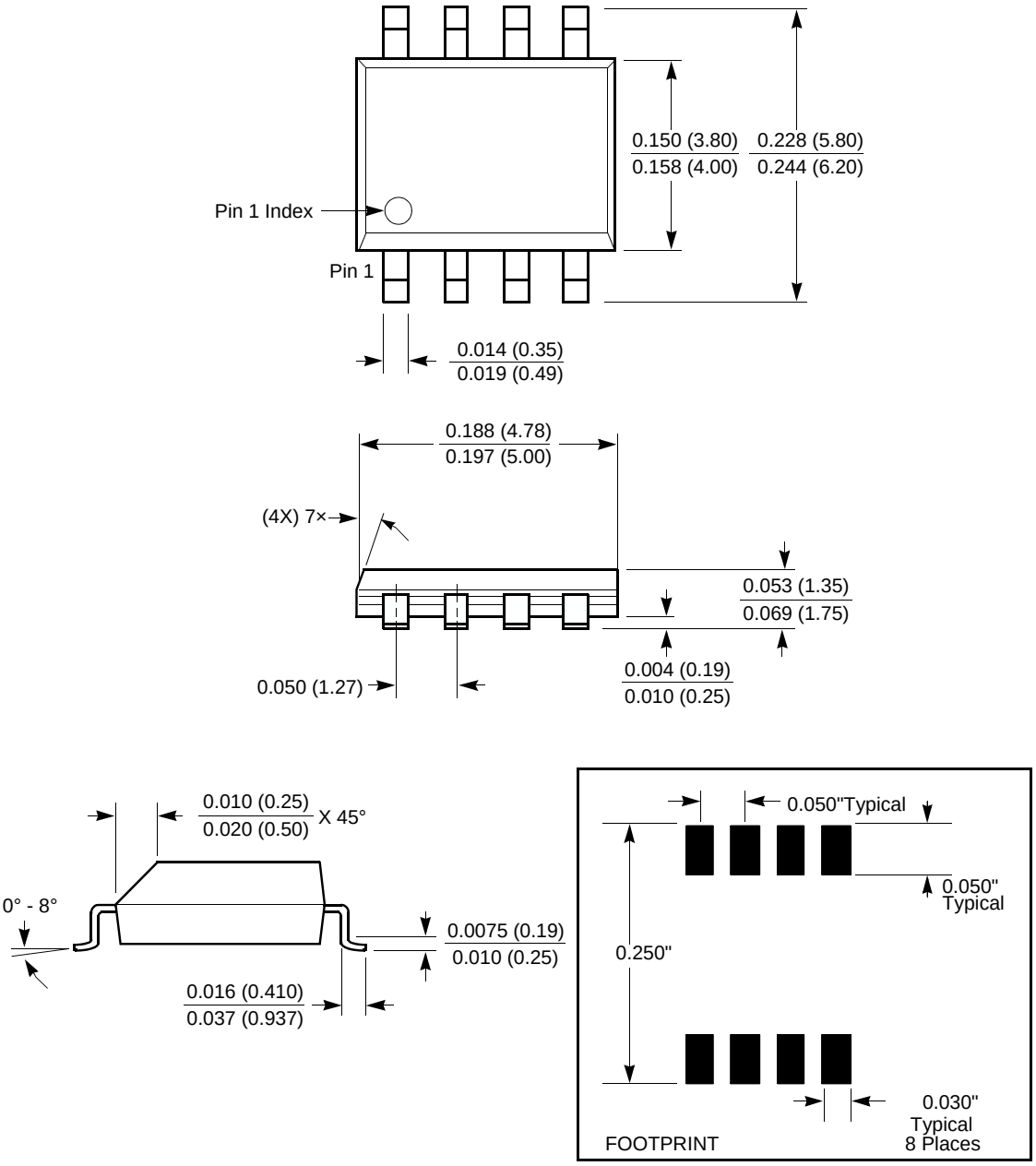
8-Lead Plastic, SOIC, Package Code S8




NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

## Packaging Information

8-Lead Plastic, SOIC, Package Code S8



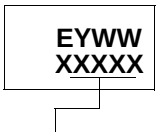

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

## Ordering Information

| VCC RANGE | PACKAGE | OPERATING TEMPERATURE RANGE | PART NUMBER 16KBIT EEPROM RESET (LOW) |
|---|---|---|---|
| 2.7-5.5V | 8L SOIC | 0°C–70°C | X1243S8 |
| | | -40°C–85°C | X1243S8I |
| | 8L TSSOP | 0°C–70°C | X1243V8 |

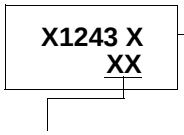
### Part Mark Information

**8-Lead TSSOP**




X1243 = 2.7 to 5.5V, 0 to +70×C
1243I = 2.7 to 5.5V, -40 to +85×C

**8-Lead SOIC**




Blank = 8-Lead SOIC

Blank = 2.7 to 5.5V, 0 to +70×C
I = 2.7 to 5.5V, -40 to +85×C

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