2-PHASE / DUAL SYNCHRONOUS PWM CONTROLLER WITH OSCILLATOR SYNCHRONIZATION AND PRE-BIAS STARTUP

FEATURES

- Dual Synchronous Controller with 180° Out of Phase Operation
- Configurable to 2-Independent Outputs or Current Share Single Output
- Voltage Mode Control
- Current Sharing Using Inductor's DCR
- Selectable Hiccup or Latched Current Limit using MOSFET's $R_{DS(on)}$ sensing
- Latched Over-Voltage Protection
- Pre-Bias Start Up
- Programmable Switching Frequency up to 500kHz
- Two Independent Soft-Starts/Shutdowns
- Precision Reference Voltage 0.8V
- Power Good Output
- External Frequency Synchronization
- Thermal Protection

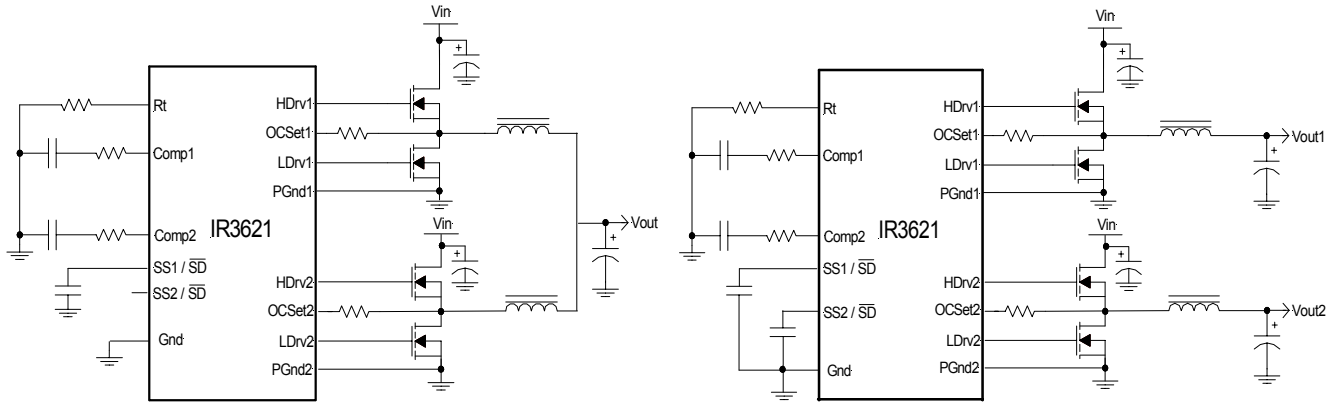
APPLICATIONS

- Embedded Networking & Telecom Systems
- Distributed Point-of-Load Power Architectures
- 2-Phase Power Supply
- Graphics Card
- DDR Memory Applications

DESCRIPTION

The IR3621 IC combines a dual synchronous buck controller and drivers, providing a cost-effective, high performance and flexible solution. The IR3621 operates in 2-Phase mode to produce either 2-independent output voltages or current share single output for high current application. The 180° out-of-phase operation allows the reduction of input and output capacitance.

Other key features include two independently programmable soft-start functions to allow system level sequencing of output voltages in various configurations. The pre-bias protection feature prevents the discharge of the output voltage and possible damage to the load during start-up when a pre-existing voltage is present at the output. Programmable switching frequency up to 500KHz per phase allows flexibility to tune the operation of the IC to meet system level requirements, and synchronization allows the simplification of system level filter design. Protection features such as selectable hiccup or latched current limit, and under voltage lock-out are provided to give required system level security in the event of a fault condition.



Current share, single output configuration

2-independent output voltage configuration

Figure 1 - Typical application of IR3621 in current share single output and 2-independent output voltage configuration

ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
M	IR3621M	32	73	------	Fig A
M	IR3621MTR	32	------	6000	
F	IR3621F	28	50	------	
F	IR3621FTR	28	------	2500	

ABSOLUTE MAXIMUM RATINGS

Vcc, V_{CL} Supply Voltage ..... -0.5V To 16V
VcH1 and VcH2 Supply Voltage ..... -0.5V To 25V
PGOOD..... -0.5V To 16V
Storage Temperature Range ..... -55°C To 150°C
Junction Temperature Range ..... -40°C To 150°C
ESD Classification ..... JEDEC, JESD22-A114

Caution: *Stresses above those listed in "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability*

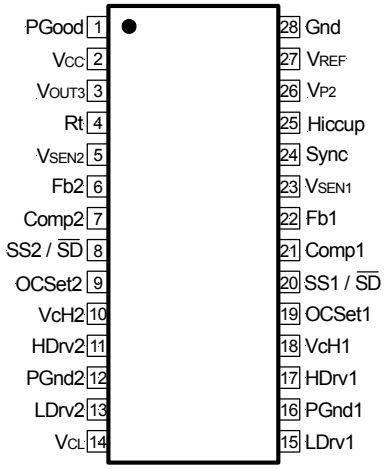
RECOMMENDED OPERATING CONDITIONS

Parameter	Definition	Min	Max	Units
Vcc	Supply Voltage	5.5	14.5	V
VcH1,2	Supply Voltage	10	20	V
Fs	Operating Frequency	200	500	kHz
Tj	Junction Temperature	-40	125	°C

PACKAGE INFORMATION

IR3621F

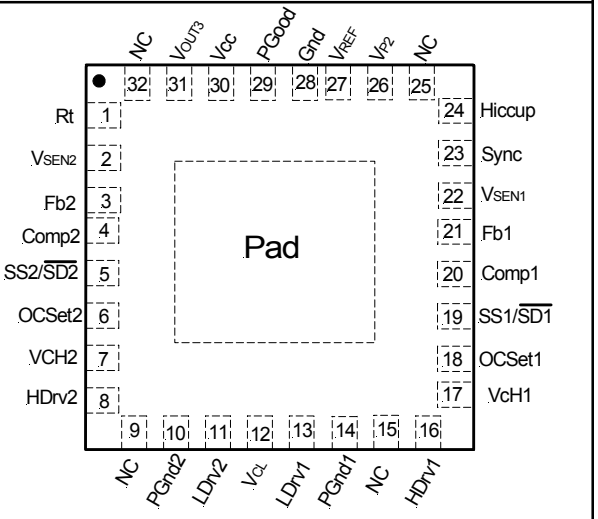
28-PIN TSSOP (F)



θ_{JA} = 75.5 °C/W
θ_{JC} =13.3 °C/W

IR3621M

32-Lead MLPQ 5mmx5mm (M)



θ_{JA} = 36.0 °C/W
θ_{JC} = 1.0 °C/W

Exposed pad on underside is connected to a copper pad through vias for 4-layer PCB board design.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=12V, VcH1=VcH2=V_{CL}=12V and 0°C<T_j<125°C.

PARAMETER	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNITS
Output Voltage Accuracy							
Feedback Voltage	V_{Fb1}, V_{Fb2}				0.80		V
Accuracy		MLPQ	Tj=25°C	-1		+1	%
			0°C <T_j< 125°C	-1.35		+1.35	%
			-40°C <T_j< 125°C	-2.5		+1.35	%
		TSSOP	Tj=25°C	-1.35		+1.35	%
			0°C <T_j< 125°C	-1.65		+1.65	%
			-40°C <T_j< 125°C	-3.0		+1.65	%
UVLO Section							
UVLO Threshold - Vcc	$UVLO_{VCC}$	Supply Ramping Up		4.7		5.3	V
UVLO Hysteresis - Vcc		Supply Ramp Up and Down			1		V
UVLO Threshold - VcH1,2	$UVLO_{VCH1,2}$	Supply Ramping Up		3.5		4.0	V
UVLO Hysteresis - VcH1,2		Supply Ramp Up and Down			0.75		V
Supply Current Section							
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=300kHz, C_L=1500pF			10	15	mA
VcH1 & VcH2 Dynamic Current	Dyn I_{CH}	Freq=300kHz, C_L=1500pF			15	25	mA
V_{CL} Dynamic Supply Current	Dyn I_{CL}	Freq=300kHz, C_L=1500pF			15	25	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V			10	15	mA
VcH1/VcH2 Static Current	I_{CHQ}	SS=0V			6	10	mA
V_{CL} Static Supply Current	I_{CLQ}	SS=0V			6	10	mA
Soft-Start / SD Section							
Charge Current	SS_{IB}	SS=0V		22	28	35	µA
Shutdown Threshold	SD					0.25	V
Power Good Section							
$V_{SENS1,2}$ Lower Trip Point	$PG_{FB1,2L}$	$V_{SENS1,2}$ Ramping Down		$0.8V_{REF}$	$0.9V_{REF}$	$0.95V_{REF}$	V
PGood Output Low Voltage	$PG_{(Voltage)}$	I_{SINK}=2mA			0.1	0.5	V
Error Amp Section							
Fb Voltage Input Bias Current	$I_{FB1,2}$	SS=3V			-0.1	-0.5	µA
Transconductance 1	g_{m1}			1400		2500	µmho
Transconductance 2	g_{m2}			1400		2500	µmho
Error Amp Source/Sink Current	$I_{(E/A)1,2}$			60	100	140	µA
Input Offset Voltage for E/A1,2	$V_{OS(ERR)}$	$Fb_{1,2}$ to V_{REF}		-4	0	+4	mV
VP2 Voltage Range	VP2	Note2		0.4		Vcc-2	V
Oscillator Section							
Frequency	Freq	$Rt_{(SET)}$ to 30.9K		255		345	kHz
Ramp Amplitude	V_{RAMP}	Note2			1.25		V
Min Duty Cycle	Dmin	Fb=1V				0	%
Min Pulse Width	Puls(ctrl)	F_{SW}=300kHz, Note2		150			ns
Max Duty Cycle	Dmax	Fb=0.6V, F_{SW}=200kHz		86.5			%
Synch Frequency Range	Sync(Fs)	20% above free running freq				1200	kHz
Synch Pulse Duration	Sync(puls)			200	300		ns
Synch High Level Threshold	Sync(H)			2			V
Synch Low Level Threshold	Sync(L)					0.6	V

Note1: Cold temperature performance is guaranteed via correlation using statistical quality control. Not 100% tested in production.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{OUT3} Internal Regulator						
Output Voltage			5.8	6.25	6.7	V
Output Current			44			mA
Protection Section						
OVP Trip Threshold	OVP	Output forced to 1.25V_{REF}	1.1V_{REF}	1.15V_{REF}	1.2V_{REF}	V
OVP Fault Prop Delay	OVP(delay)	Note2			5	µs
OCSET Current	I_{OCSet}		16	20	24	µA
Hiccup Duty Cycle		Hiccup pin pulled high, Note2		5		%
Hiccup High Level Threshold		Note2	2			V
Hiccup Low Level Threshold		Note2			0.8	V
Thermal Shutdown Trip Point		Note2		140		℃
Thermal Shutdown Hysteresis		Note2		20		℃
Output Drivers Section						
LO Drive Rise Time	$T_{r(LO)}$	C_L=1500pF,Figure 2		18	50	ns
HI Drive Rise Time	$T_{r(HI)}$	C_L=1500pF, Figure 2		18	50	ns
LO Drive Fall Time	$T_{f(LO)}$	C_L=1500pF,Figure 2		25	50	ns
Hi Drive Fall Time	$T_{f(HI)}$	C_L=1500pF,Figure 2		25	50	ns
Dead Band Time	T_{DB}	See Figure 2		50	100	ns

Note 2: Guaranteed by design but not tested for production.

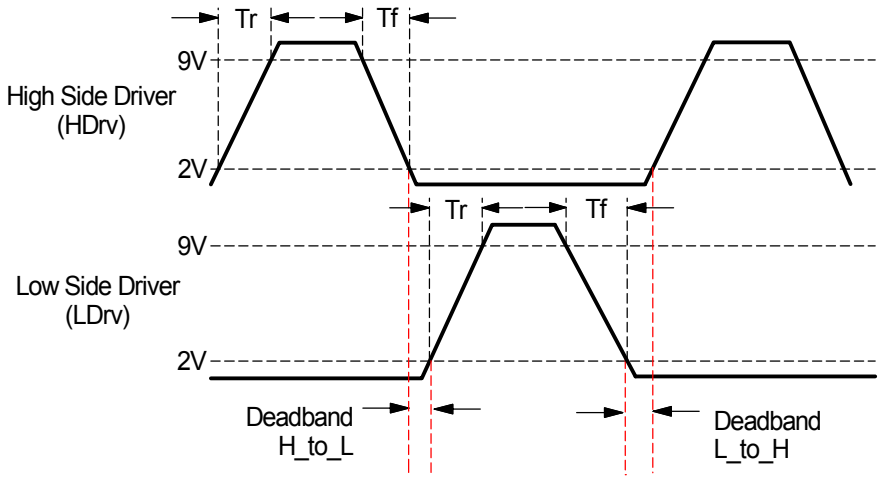


Figure 2 - Rise Time, Fall Time and Deadband for Driver Section

PIN DESCRIPTIONS

TSSOP	MLPQ	PIN SYMBOL	PIN DESCRIPTION
1	29	PGood	Power Good pin. Low when any of the outputs fall 10% below the set voltages.
2	30	Vcc	Supply voltage for the internal blocks of the IC. The Vcc slew rate should be <0.1V/us.
3	31	V_{OUT3}	Output of the internal LDO. Connect a 1.0uF capacitor from this pin to ground.
4	1	Rt	Connecting a resistor from this pin to ground sets the oscillator frequency.
5,23	2,22	V_{SEN2}, V_{SEN1}	Sense pins for OVP and PGood. For current share tie these pins together.
6,22	3,21	Fb2,Fb1	Inverting inputs to the error amplifiers. In current sharing mode, Fb1 is connected to a resistor divider to set the output voltage and Fb2 is connected to programming resistor to achieve current sharing. In independent 2-channel mode, these pins work as feedback inputs for each channel.
7,21	4,20	Comp2, Comp1	Compensation pins for the error amplifiers.
8 20	5 19	SS2 / SD SS1 / SD	These pins provide user programmable soft-start function for each outputs. Connect external capacitors from these pins to ground to set the start up time for each output. These outputs can be shutdown independently by pulling the respective pins below 0.3V. During shutdown both MOSFETs will be turned off. For current share mode SS2 must be floating.
9,19	6,18	OCSet2,OCSet1	A resistor from these pins to switching point will set current limit threshold.
10,18	7,17	VcH2, VcH1	Supply voltage for the high side output drivers. These are connected to voltages that must be typically 6V higher than their bus voltages. A 0.1μF high frequency capacitor must be connected from these pins to PGND to provide peak drive current capability.
11,17	8,16	HDrv2, HDrv1	Output drivers for the high side power MOSFETs. **Note3**
12,16	10,14	PGnd2, PGnd1	These pins serve as the separate grounds for MOSFET drivers and should be connected to the system's ground plane.
13,15	11,13	LDrv2, LDrv1	Output drivers for the synchronous power MOSFETs.
14	12	V_{CL}	Supply voltage for the low side output drivers.
24	23	Sync	The internal oscillator can be synchronized to an external clock via this pin.
25	24	Hiccup	When pulled High, it puts the device current limit into a hiccup mode. When pulled Low, the output latches off, after an overcurrent event.
26	26	V_{P2}	Non-inverting input to the second error amplifier. In the current sharing mode, it is connected to the programming resistor to achieve current sharing. In independent 2-channel mode it is connected to V_{REF} pin when Fb2 is connected to the resistor divider to set the output voltage.
27	27	V_{REF}	Reference Voltage. The drive capability of this pin is about 2μA.
28	28	Gnd	Analog ground for internal reference and control circuitry.
	9,15,25,32	N/C	No Connect

Note3: The negative voltage at these pins may cause instability for the gate drive circuits. To prevent this, a low forward voltage drop diode (Schottky) is required between these pins and power ground.

BLOCK DIAGRAM

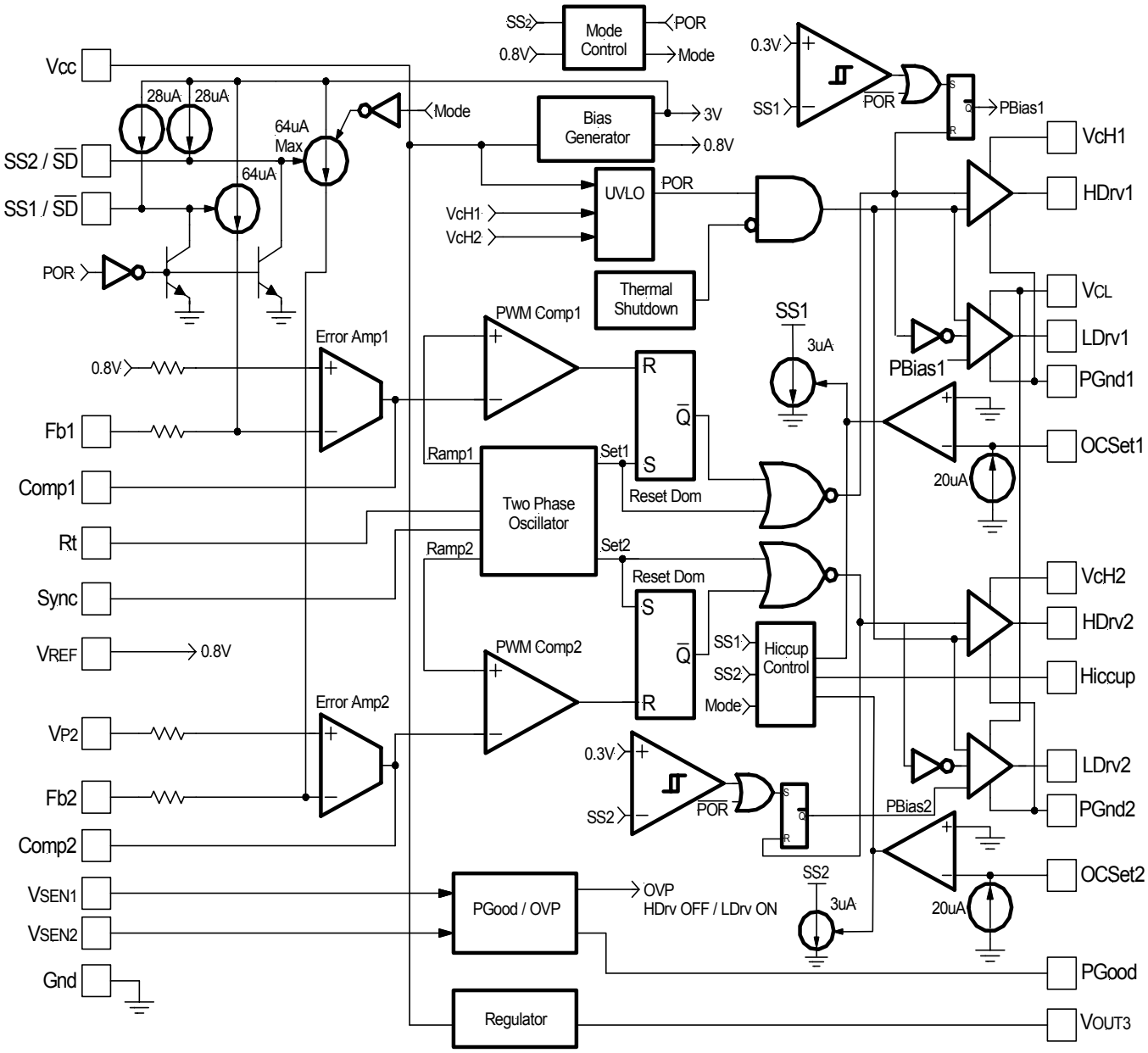


Figure 3 - IR3621Block Diagram

FUNCTIONAL DESCRIPTION

Introduction

The IR3621 is a versatile device for high performance buck converters. It consists of two synchronous buck controllers which can be operated either in two independent mode or in current share mode.

The timing of the IC is provided by an internal oscillator circuit which generates two out-of-phase clock that can be programmed up to 500kHz per phase.

Supply Voltage

Vcc is the supply voltage for internal controller. The operating range is from 5.5V to 14.5V. It also is fed to the internal LDO. When Vcc is below under-voltage threshold, all MOSFET drivers will be turned off.

Internal Regulator

The regulator powers directly from Vcc and generates a regulated voltage (Typ. 6.2V@40mA). The output is protected for short circuit. This voltage can be used for charge pump circuitry as shown in Figure12.

Input Supplies UnderVoltage LockOut

The IR3621 UVLO block monitors three input voltages (Vcc, VcH1 and VcH2) to ensure reliable start up. The MOSFET driver output turn off when any of the supply voltages drops below set thresholds. Normal operation resumes once the supply voltages rise above the set values.

Mode Selection

The SS2 pin is used for mode selection. In current share mode this pin should be floating and in dual output mode a soft start capacitor must be connected from this pin to ground to program the start time for the second output.

Independent Mode

In this mode the IR3621 provides control to two independent output power supplies with either common or different input voltages. The output voltage of each individual channel is set and controlled by the output of the error amplifier, which is the amplified error signal from the sensed output voltage and the reference voltage. The error amplifier output voltage is compared to the ramp signal thus generating fixed frequency pulses of variable duty-cycle, which are applied to the FET drivers, Figure19 shows a typical schematic for such application.

Currnt Share Mode

This feature allows to connect both outputs together to increase current handling capability of the converter to support a common load. The current sharing can be done either using external resistors or sensing the DCR of inductors (see Figure 4).

In this mode, one control loop acts as a master and sets the output voltage as a regular Voltage Mode Buck controller and the other control loop acts as a slave and monitors the current information for current sharing. The voltage drops across the current sense resistors (or DCR of inductors) are measured and their difference is amplified by the slave error amplifier and compared with the ramp signal to generate the PWM pulses to match the output current. In this mode the SS2 pin should be floating.

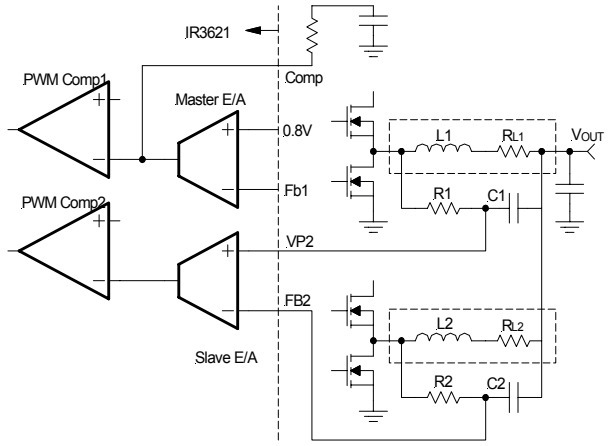


Figure 4 - Loss-less inductive current sensing and current sharing.

In the diagram, L1 and L2 are the output inductors. R_{L1} and R_{L2} are inherent inductor resistances. The resistor R1 and capacitor C1 are used to sense the average inductor current. The voltage across the capacitors C1 and C2 represent the average current flowing into resistance R_{L1} and R_{L2}. The time constant of the RC network should be equal or at most three times larger than the time constant L_1/R_{L1}.

$$R1 \times C1 = (1\sim3) \times \frac{L1}{R_{L1}} \qquad ---(1)$$

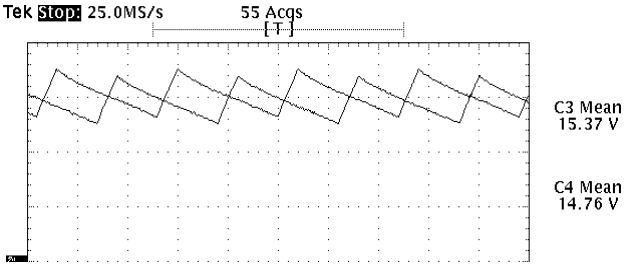


Figure 5 - 30A Current Sharing using Inductor sensing
(5A/Div)

Dual Soft-Start

The IR3621 has programmable soft-start to control the output voltage rise and limit the inrush current during start-up. It provides a separate Soft-Start function for each outputs. This will enable to sequence the outputs by controlling the rise time of each output through selection of different value soft-start capacitors. The soft-start pins will be connected together for applications where, both outputs are required to ramp-up at the same time.

To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1 and VcH2 rise above their threshold and generate the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. During power up, the converter output starts at zero and thus the voltage at Fb is about 0V. A current (64μA) injects into the Fb pin and generates a voltage about 1.6V (64μA × 25K) across the negative input of E/A and (see Figure6).
The magnitude of this current is inversely proportional to the voltage at soft-start pin. The 28μA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at negative input of E/A.

When the soft-start capacitor is around 1V, the current flowing into the Fb pin is approximately 32μA. The voltage at the positive input of the E/A is approximately:

$$32\mu A \times 25K = 0.8V$$

The E/A will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing. Because the voltage at pin of E/A is regulated to reference voltage 0.8V, the voltage at the Fb is:

$$V_{FB} = 0.8\text{-}(25K \times \text{Injected Current})$$

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 1.8V and the output voltage goes into steady state. Figure 7 shows the theoretical operational waveforms during soft-start.

Low Temperature Start-Up

The controller is capable of starting at -40°C ambient temperature.

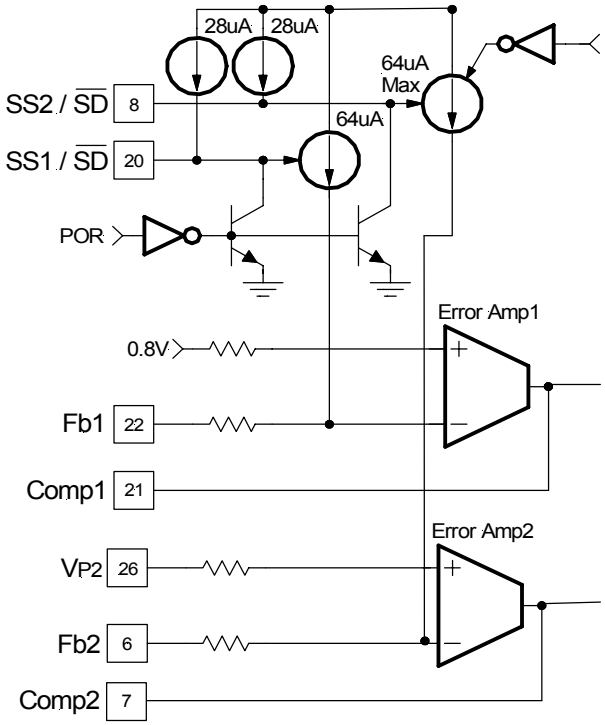


Figure 6 -Soft-start circuit for IR3621

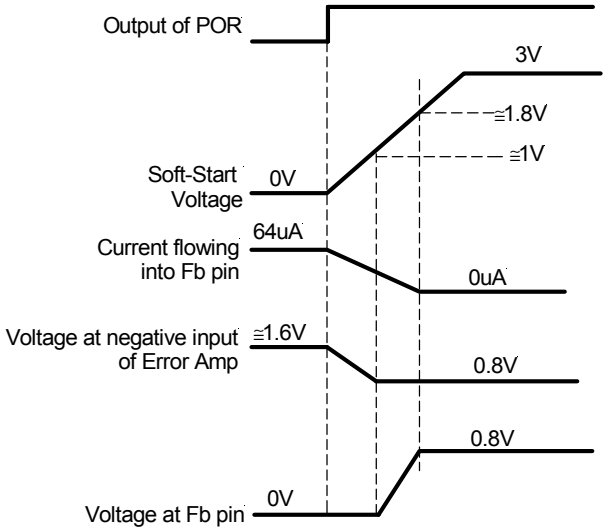


Figure 7 - Theoretical operational waveforms during soft-start.

The output start-up time is the time period when soft-start capacitor voltage increases from 1V to 1.8V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$28\mu A \times T_{START}/C_{SS} = 1.8V\text{-}1V$$

For a given start up time, the soft-start capacitor can be calculated by:

$$C_{SS} \cong 28\mu A \times T_{START}/0.8V$$

The soft-start is part of the Over Current Protection scheme, during the overload or short circuit condition the external soft start capacitors will be charged and discharged in certain slope rate to achieve the hiccup mode function.

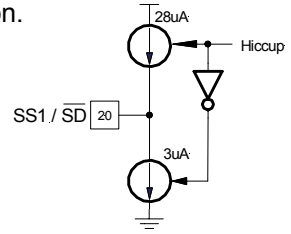


Figure 8 - 3uA current source for discharging soft start-capacitor during Hiccup mode

Out-of-Phase Operation

The IR3621 drives its two output stages 180° out-of-phase. In 2-phase configuration, the two inductor ripple currents cancel each other and result in a reduction of the output current ripple and yield a smaller output capacitor for the same ripple voltage requirement.

In single input voltage applications, the input ripple current reduces. This results in much smaller input capacitor's RMS current and reduces the input capacitor quantity.

Over-Current Protection

The IR3621 can provide two different schemes for Over-Current Protection (OCP). When the Hiccup pin is pulled high, the OCP will operate in hiccup mode. In this mode, during overload or short circuit, the outputs enter hiccup mode and stay in that mode until the overload or short circuit is removed. The converter will automatically re-cover.

When the Hiccup pin is pulled low, the OCP scheme will be changed to the latch up type, in this mode the converter will be turned off during Overcurrent or short circuit. The power needs to be recycled for normal operation.

Each phase has its own independent OCP circuitry.

The OCP is performed by sensing current through the $R_{DS(ON)}$ of low side MOSFET. As shown in Figure 9, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) which sets the current limit set point.

If using one soft start capacitor in dual configuration for a precise power up the OCP needs to be set to latch mode.

The internal current source develops a voltage across R_{SET}. When the low side switch is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times i_L \quad ---(2)$$

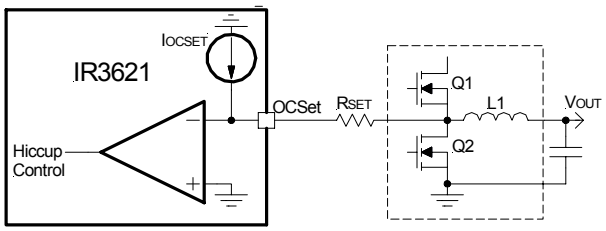


Figure 9 - Diagram of the over current sensing.

The critical inductor current can be calculated by setting:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times I_L = 0$$

$$I_{SET} = I_{L(CRITICAL)} = \frac{R_{SET} \times I_{OCSET}}{R_{DS(ON)}} \quad ---(3)$$

The value of R_{SET} should be checked in an actual circuit to ensure that the Over Current Protection circuit activates as expected. The IR3621 current limit is designed primarily as disaster preventing, "no blow up" circuit, and is not useful as a precision current regulator.

In two independent mode, the output of each channel is protected independently which means if one output is under overload or short circuit condition, the other output will remain functional. The OCP set limit can be programmed to different levels by using the external resistors. This is valid for both hiccup mode and latch up mode.

In 2-phase configuration, the OCP's output depends on any one channel, which means as soon as one channel goes to overload or short circuit condition the output will enter either hiccup or latch-up, dependes on status of Hiccup pin.

Pre-bias Startup

The IR3621 allows pre-bias startup without discharging the output capacitors. The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated.

Frequency Synchronization

The IR3621 is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge at an external clock. Per-channel switching frequency is set by external resistor (Rt). The free running oscillator frequency is twice the per-channel frequency. During synchronization, Rt is selected such that the free running frequency is 20% below the sync frequency. Synchronization capability is provided for both 2-output and 2-phase configurations. When unused, the Sync pin will remain floating and is noise immune.

Thermal Shutdown

Temperature sensing is provided inside IR3621. The trip threshold is typically set to 140°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops to normal range. There is a 20°C hysteresis in the shutdown threshold.

Power Good

The IR3621 provides a power good signal. The power good signal should be available after both outputs have reached regulation. This pin needs to be externally pulled high. High state indicates that outputs are in regulation.
Power good will be low if either one of the output voltages is 10% below the set value. There is only one power good for both outputs.

Over-Voltage Protection OVP

Over-voltage is sensed through separate V_{OUT} sense pins V_{SEN1} and V_{SEN2}. A separate OVP circuit is provided for each output. Upon over-voltage condition of either one of the outputs, the OVP forces a latched shutdown on both outputs. In this mode, the upper FET drivers turn off and the lower FET drivers turn on, thus crowbaring the outputs. Reset is performed by recycling Vcc.

Error Amplifier

The IR3621 is a voltage mode controller. The error amplifiers are of transconductance type. In independent mode, each amplifier closes the loop around its own output voltage. In current sharing mode, amplifier 1 becomes the master which regulates the common output voltage. Amplifier 2 performs the current sharing function. Both amplifiers are capable of operating with Type III compensation control scheme.

Operation Frequency Selection

The optimum operating frequency range for the IR3621 is 300kHz per phase, theoretically the IR3621 can be operated at higher switching frequency (e.g. 500kHz). However the power dissipation for IC, which is function of applied voltage, gate drivers load and switching frequency, will result in higher junction temperature of device. It may exceed absolute maximum rating of junction temperature, figure 18 (page 17) shows case temperature versus switching frequency with different capacitive loads for TSSOP package.
This should be considered when using IR3621 for such application. The below equation shows the relationship between the IC's maximum power dissipation and Junction temperature:

$$Pd = \frac{T_J - T_A}{\theta_{JA}}$$

Where:
Tj: Maximum Operating Junction Temperature
TA: Ambient Temperature
θ_{JA} = Thermal Impedance of package

The switching frequency is determined by an external resistor (Rt). The switching frequency is approximately inversely proportioned to resistance (see Fig 10).

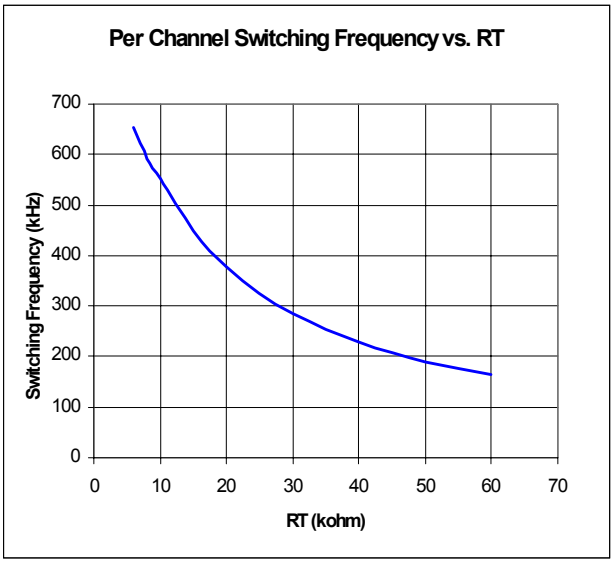


Figure 10- Switching Frequency versus External Resistor.

Shutdown

The outputs can be shutdown independently by pulling the respective soft-start pins below 0.3V. This can be easily done by using an external small signal transistor. During shutdown both MOSFETs will be turned off. During this mode the LDO will stay on. Normal operation will resume by cycling soft start pins.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for the IR3621, the schematic is Figure19 on page18.

V_{IN} = 12V
$V_{OUT(2.5V)}$ = 2.5V @ 10A
$V_{OUT(1.8V)}$ = 1.8V @ 10A
ΔV_{OUT} = Output voltage ripple ≅ 3% of V_{OUT}
F_S = 400kHz

Output Voltage Programming
Output voltage is programmed by the reference voltage and an external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is referenced to the voltage on the non-inverting pin of error amplifier. For this application, this pin (V_{P2}) is connected to the reference voltage (V_{REF}). The output voltage is defined by using the following equation:

$$V_{OUT} = V_{P2} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(4)$$

$V_{P2} = V_{REF} = 0.8V$

When an external resistor divider is connected to the output as shown in Figure 11.

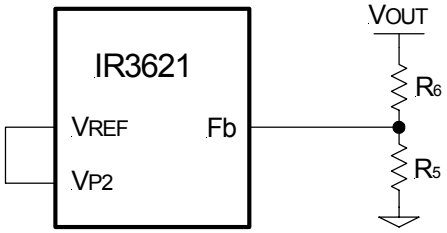


Figure 11 - Typical application of the IR3621 for programming the output voltage.

Equation (4) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_P} - 1\right)$$

Will result to:

$V_{OUT(2.5V)}$ = 2.5V
V_{REF} = 0.8V
R_9= 2.15K, R_5= 1K

$V_{OUT(1.8V)}$ = 1.8V
V_{REF} = 0.8
R_7= 1.24K, R_8 = 1K

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage can be set more accurately by using low value, precision resistors.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$Css \cong 28 \times t_{START} \quad (\mu F) \qquad ---(5)$$

Where t_{START} is the desired start-up time (ms)

For a start-up time of 4ms for both output, the soft-start capacitor will be 0.1μF. Connect two 0.1μFceramic capacitors from SS1 pin and SS2 pin to GND.

Supply VcH1 and VcH2
To drive the high side MOSFET, it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 12. This method is simple and inexpensive. The operation of the circuit is as follows: when the lower MOSFET is turned on, the capacitor (C1) charges up to V_{OUT3}, through the diode (D1). The bus voltage will be added to this voltage when upper MOSFET turns on in next cycle, and providing supply voltage (VcH1) through diode (D2). VcH1 is approximately:

$$VCH1 \cong V_{OUT3} + V_{BUS} - (V_{D1} + V_{D2})$$

Capacitor in the range of 0.1μF is generally adequate for most applications. The diode must be a fast recovery device to minimize the amount of charge fed back from the charge pump capacitor into V_{OUT3}. The diodes need to be able to block the full power rail voltage, which is seen when the high side MOSFET is switched on. For low voltage application, Schottky diodes can be used to minimize forward drop across the diodes at start up.

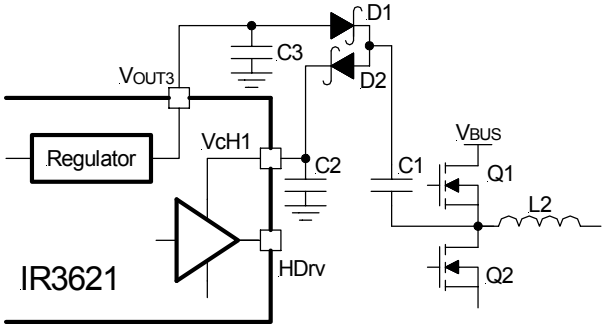


Figure 12 - Charge pump circuit.

Input Capacitor Selection

The 180^0 out of phase will reduce the RMS value of the ripple current seen by input capacitors. This reduces numbers of input capacitors. The input capacitors must be selected that can handle both the maximum ripple RMS at highest ambient temperature as well as the maximum input voltage. The RMS value of current ripple for duty cycles under 50% is expressed by:

$$I_{RMS}=\sqrt{(I_1^2D_1(1-D_1)+I_2^2D_2(1-D_2)-2I_1I_2D_1D_2)} \quad \text{--- (6)}$$

Where:
I_{RMS} is the RMS value of the input capacitor current
D_1 and D_2 are the duty cycle for each output
I_1 and I_2 are the current for each output
For this application the I_{RMS} =4.8A

For higher efficiency, low ESR capacitors are recommended.
Choose two Poscap from Sanyo 16TPB47M (16V, 47µF, 70mΩ) with a maximum allowable ripple current of 1.4A for inputs of each channel.

Inductor Selection

The inductor is selected based on operating frequency, transient performance and allowable output voltage ripple. Low inductor values result in faster response to step load (high $\Delta i/\Delta t$) and smaller size but will cause larger output ripple due to increased inductor ripple current. As a rule of thumb, select an inductor that produces a ripple current of 10-40% of full load DC.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \quad \text{---(7)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

For $\Delta i_{(2.5V)}$ = 45%($I_{O(2.5V)}$), then the output inductor will be:

L_4 = 1.1µH

For $\Delta i_{(1.8V)}$ = 35%($I_{O(1.8V)}$), then the output inductor will be:

L_3 = 1.1µH

Panasonic provides a range of inductors in different values and low profile for large currents.

Choose ETQP6F1R1BFA (1.1µH, 16A, 2.2mΩ) both for L_3 and L_4.

For 2-phase application, equation (7) can be used for calculating the inductors value. In such case the inductor ripple current is usually chosen to be between 10-40% of maximum phase current.

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship: (ESL, Equivalent Series Inductance is neglected)

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \quad \text{---(8)}$$

Where:
ΔV_O = Output Voltage Ripple
Δi = Inductor Ripple Current
ΔV_O = 3% of V_O will result to $ESR_{(2.5V)}$ =16.6mΩ and $ESR_{(1.8V)}$ =16mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC330M, 330µF, 6.3V has an ESR 40mΩ. Selecting three of these capacitors in parallel for 2.5V output, results to an ESR of ≅ 13.3mΩ which achieves our low ESR goal. And selecting three of these capacitors in parallel for 1.8V output, results in an ESR of ≅ 13.3mΩ which achieves our low ESR goal.
The capacitors value must be high enough to absorb the inductor's ripple current.

Power MOSFET Selection

The IR3621 uses four N-Channel MOSFETs. The selection criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The both control and synchronous MOSFETs must have a maximum operating voltage (V_{DSS}) that exceeds the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistors can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results in a shoot-through.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter, the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND}(\text{Upper Switch}) = I_{LOAD}^2 \times R_{DS(on)} \times D \times \vartheta$$

$$P_{COND}(\text{Lower Switch}) = I_{LOAD}^2 \times R_{DS(on)} \times (1 - D) \times \vartheta$$

$\vartheta = R_{DS(on)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7821 for control MOSFETs and IRF8113 for synchronous MOSFETs. These devices provide low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7821	IRF8113
V_{DSS} = 30V	V_{DSS} = 30V
$R_{DS(on)}$ = 9mΩ	$R_{DS(on)}$ = 6mΩ

The total conduction losses for each output will be:

$$P_{CON(TOTAL,\ 2.5V)} = P_{CON(UPPER)} + P_{CON(LOWER)}$$

$$P_{CON(TOTAL,\ 2.5V)} = 1.0W$$

$$P_{CON(TOTAL,\ 1.8V)} = P_{CON(UPPER)} + P_{CON(LOWER)}$$

$$P_{CON(TOTAL,\ 1.8V)} = 1.0W$$

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in a synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the switching losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(9)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

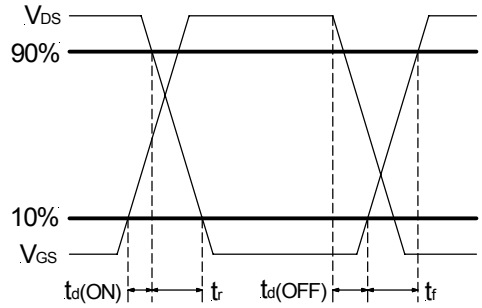


Figure 13 - Switching time waveforms.

From IRF7821 data sheet we obtain:
IRF7821
t_r = 2.7ns
t_f = 7.3ns

These values are taken under a certain condition test. For more details please refer to the IRF7821 data sheet.

By using equation (9), we can calculate the total switching losses.

$P_{SW(TOTAL,2.5V)}$ = 0.18W
$P_{SW(TOTAL,1.8V)}$ = 0.18W

Programming the Over-Current Limit
The over-current threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (3).

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worse case operation.

$R_{DS(on)} = 6m\Omega \times 1.5 = 9m\Omega$
$I_{SET} \cong I_{O(LIM)} = 10A \times 1.5 = 15A$
(50% over nominal output current)

This results to:
$R_{SET} = R_1 = R_6 = 6.75K\Omega$

This resistor must be placed close to the IC, place a small ceramic capacitor from this pin to ground for noise rejection purposes.

Feedback Compensation

The IR3621 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 14). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad ---(10)$$

Where: Lo is the output inductor
For 2-phase application, the effective output inductance should be used

Co is the total output capacitor

Figure 14 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

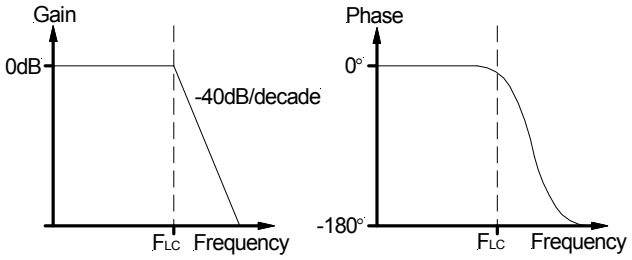


Figure14 - Gain and phase of LC filter

The IR3621's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.
The E/A can be compensated with or without the use of local feedback. When operated without local feedback, the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 15.

Note that this method requires the output capacitor to have enough ESR to satisfy stability requirements. In general, the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(10A)$$

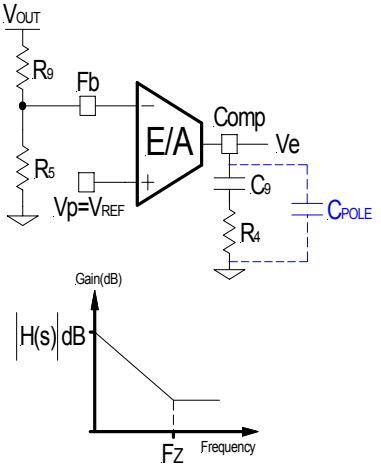


Figure 15 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_9 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(11)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s=j \times 2\pi \times F_O)| = g_m \times \frac{R_5}{R_9+R_5} \times R_4 \qquad ---(12)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(13)$$

|H(s)| is the gain at zero cross frequency.
First select the desired zero-crossover frequency (F_{O1}):

$$F_{O1} > F_{ESR} \text{ and } F_{O1} \leq (1/5 \sim 1/10) \times f_S$$

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{F_{O1} \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_9}{R_5} \times \frac{1}{g_m} \quad ---(14)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
F_{O1} = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_9 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For $V_{2.5V}$:

V_{IN} = 12V	F_{LC} = 5.06kHz
V_{OSC} = 1.25V	R_5 = 1K
F_{O1} = 40kHz	R_9 = 2.14K
F_{ESR} = 13.3KHz	g_m = 1400μmho

This results to R_4=4.8K
Choose R_4=5K

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \quad ---(15)$$

For:

Lo = 1.1μH	F_Z = 3.61kHz
Co = 990μF	R_4 = 5K

Using equations (13) and (15) to calculate C_9, we get:

$C_9 \cong$ 8.3nF; Choose C_9 =8.2nF

Same calcuation For $V_{1.8V}$ will result to: R_3 = 4.2K and C_8 = 10nF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditional stability for ceramic output capacitor with very low ESR or any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for a voltage-mode controller is shown in Figure 16.

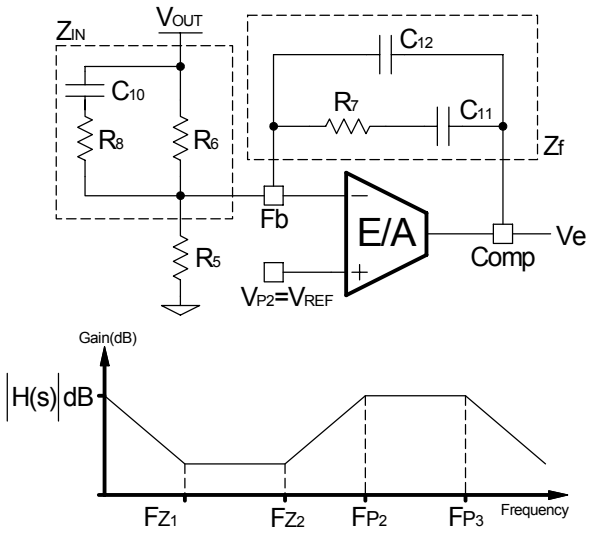


Figure 16- Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$g_m Z_f >> 1$ and $g_m Z_{IN} >> 1$ ---(16)

By replacing Z_{IN} and Z_f according to Figure 16, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \quad ---(17)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (16) regarding transconductance error amplifier.

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient response. The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Based on the frequency of the zero generated by ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation type and location of crossover frequency.

Compensator Type	Location of Zero Crossover Frequency (F_O)	Typical Output Capacitor
Type II (PI)	$F_{LC} < F_{ESR} < F_O < f_S/2$	Electrolytic, Tantalum
Type III (PID) Method A	$F_{LC} < F_O < F_{ESR} < f_S/2$	Tantalum, Ceramic
Type III (PID) Method B	$F_{LC} < F_O < f_S/2 < F_{ZO}$	Ceramic

Table - The compensation type and location of zero crossover frequency.

Details are dicussed in application Note AN-1043 which can be downloaded from the IR Web-Site.

Compensation for Slave Error Amplfier for 2-Phase Configuration

The slave error amplifier is a differential-input transconductance amplifier, in 2-phase configuration the main goal for the slave feed back loop is to control the inductor current to match the master's inductor current as well provides highest bandwidth and adequate phase margin for overall stability. The following analysis is valid for both using external current sense resistor and using DCR of inductors.

The transfer function of power stage is expressed by:

$$G(s) = \frac{I_{L2}(s)}{Ve(s)} = \frac{V_{IN}}{sL_2 \times V_{OSC}} \quad ---(18)$$

Where:
V_{IN} = Input Voltage
L_2 = Output Inductor
V_{OSC} = Oscillator Peak Voltage

As shown the transfer function is a function of inductor current.

The transfer function for the compensation network is given by equation (19), when using a series RC circuit as shown in Figure 17:

$$D(s) = \frac{Ve(s)}{R_{S2} \times I_{L2}(s)} = \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1 + sC_2R_2}{sC_2}\right) \quad ---(19)$$

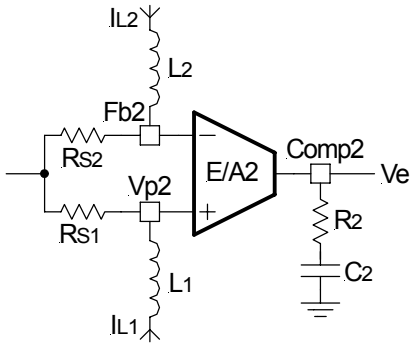


Figure 17 - The PI compensation network for slave channel.

The loop gain function is:

$$H(s)=[G(s) \times D(s) \times R_{S2}]$$

$$H(s)=R_{S2} \times \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1+sR_2C_2}{sC_2}\right) \times \left(\frac{V_{IN}}{sL_2 \times V_{OSC}}\right)$$

Select a zero crossover frequency for control loop (F_{O2}) 1.25 times larger than zero crossover frequency for voltage loop (F_{O1}):

$$F_{o2} \cong 1.25\% x F_{01}$$

$$H(Fo) = g_m \times R_{S1} \times R_2 \times \frac{V_{IN}}{2\pi \times Fo \times L_2 \times V_{OSC}} = 1 \quad ---(20)$$

From (20), R_2 can be express as:

$$R_2 = \frac{1}{g_m \times R_{S1}} \times \frac{2\pi \times F_{O2} \times L_2 \times V_{OSC}}{V_{IN}} \quad ---(21)$$

The power stage of current loop has a dominant pole (F_p) at frequency expressed by:

$$F_p = \frac{R_{eq}}{2\pi \times L_2}$$

Where R_{eq} is the total resistance of the power stage which includes the $R_{ds(on)}$ of the FET switches, the DCR of inductor and shunt resistance (if it used).

$$R_{eq} = R_{DS(on)} + R_L + R_s$$

Set the zero of compensator at 10 times the dominant pole frequency F_p, the compensator capacitor, C_2 can be calculated as:

$$F_z = 10 \times F_p \qquad C_2 = \frac{1}{2\pi x R_2 x F_z}$$

All design should be tested for stability to verify the calculated values.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start by placing the power components. Make all the connections in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching. Place input capacitor near to the drain of the high-side MOSFET.

The layout of driver section should be designed for a low resistance (a wide, short trace) and low inductance (a wide trace with ground return path directly beneath it), this directly affects the driver's performance.

To reduce the ESR, replace the one input capacitor with two parallel ones. The feedback part of the system should be kept away from the inductor and other noise sources and must be placed close to the IC. In multilayer PCBs, use one layer as power ground plane and have a separate control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current paths to a separate loops that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

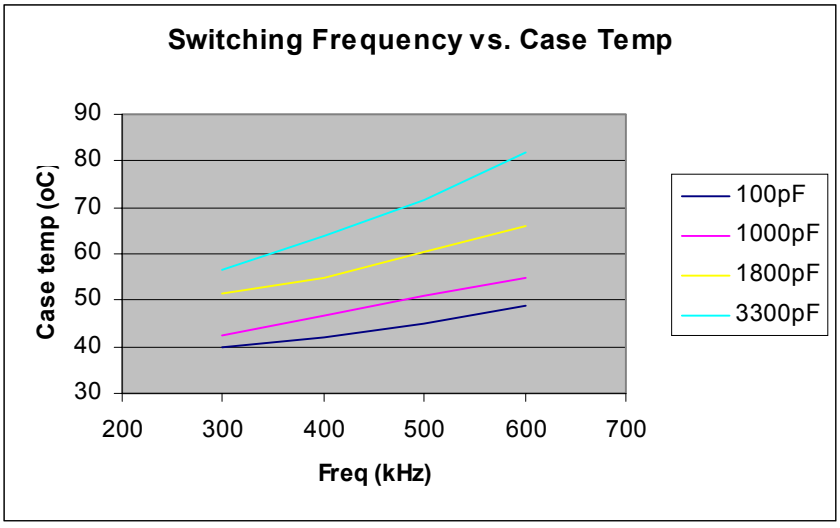


Figure18- Case Temperature (TSSOP package) versus Switching Frequency at Room Temperature
Test Condition: Vin=VcL=VcH1=VcH2=12V, Capacitors used as loads for output drivers.

TYPICAL APPLICATION

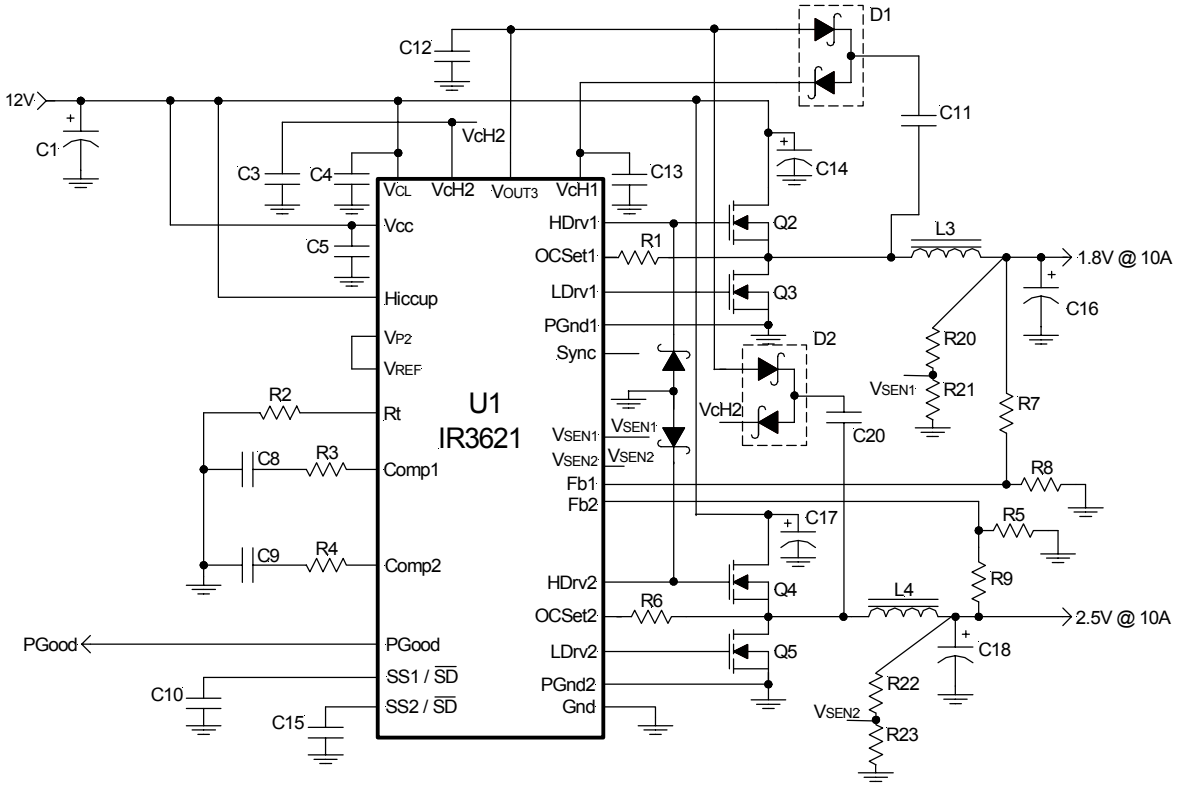


Figure 19 - Typical application of IR3621.
12V input and two independent outputs using type 2 compensation.

TYPICAL APPLICATION

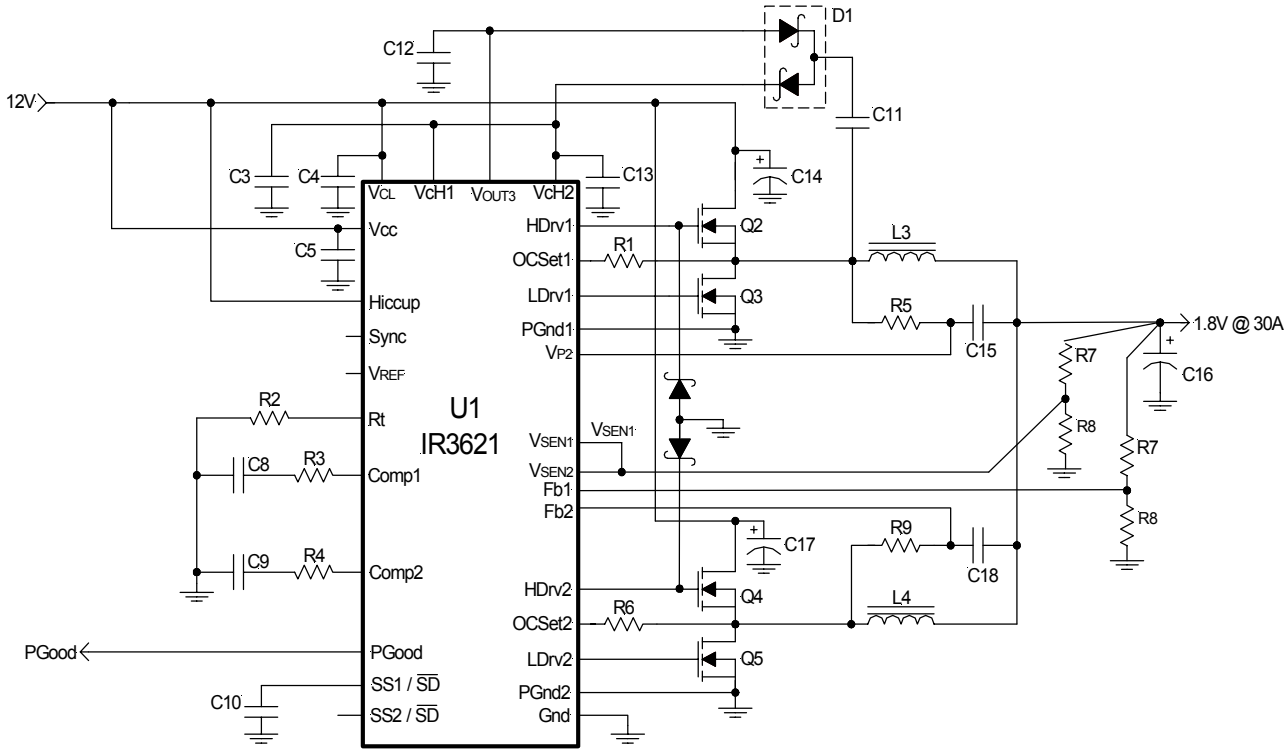
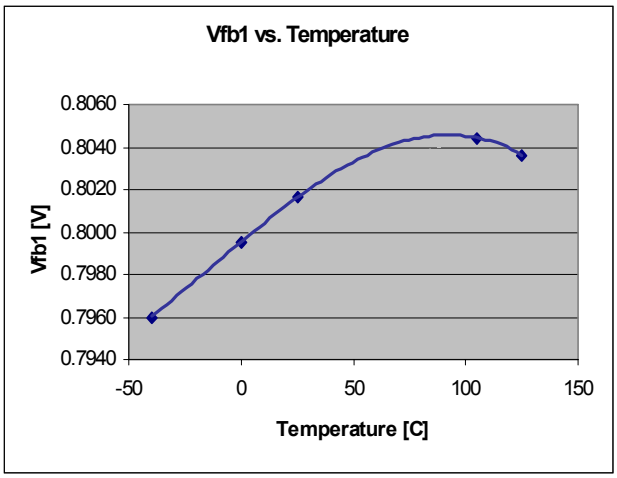
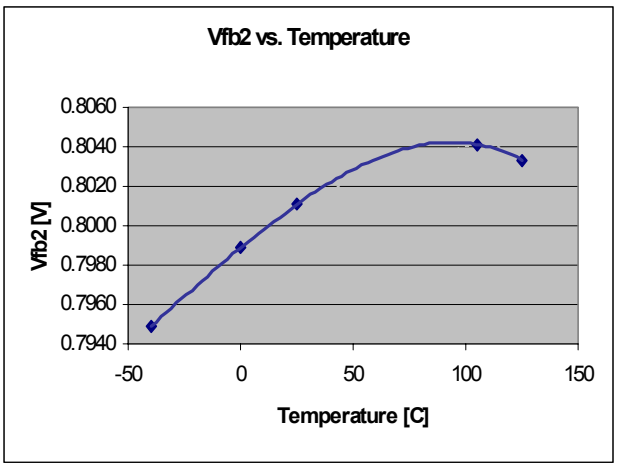
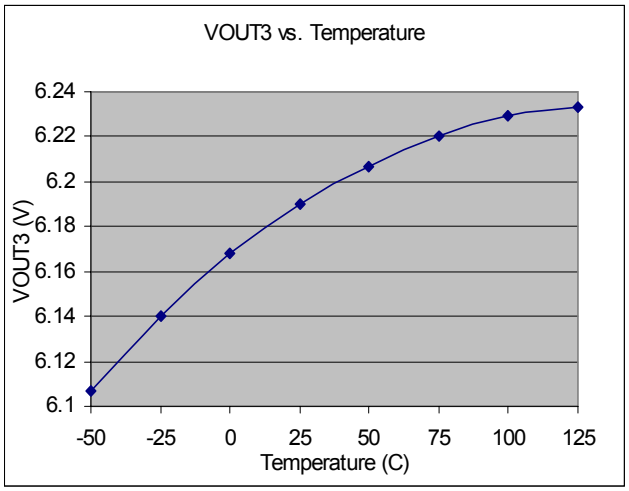


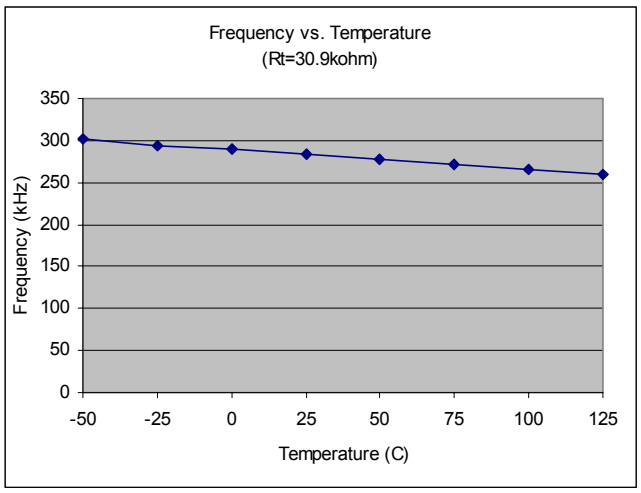
Figure 20 - 2-phase operation with inductor current sensing using type 2 compensation.
12V to 1.8V @ 30A output

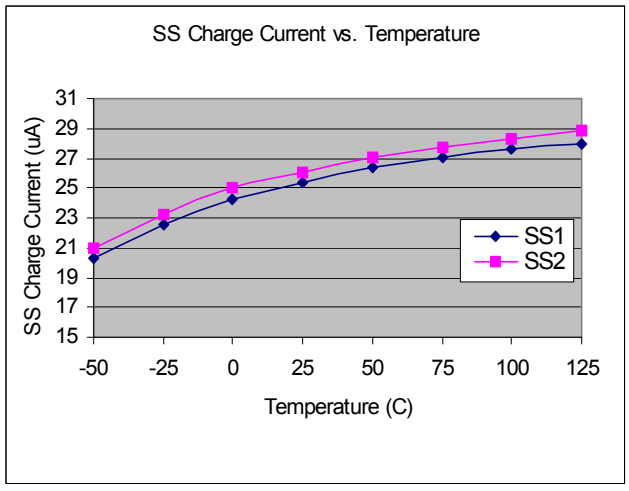
TYPICAL OPERATING CHARACTERISTICS

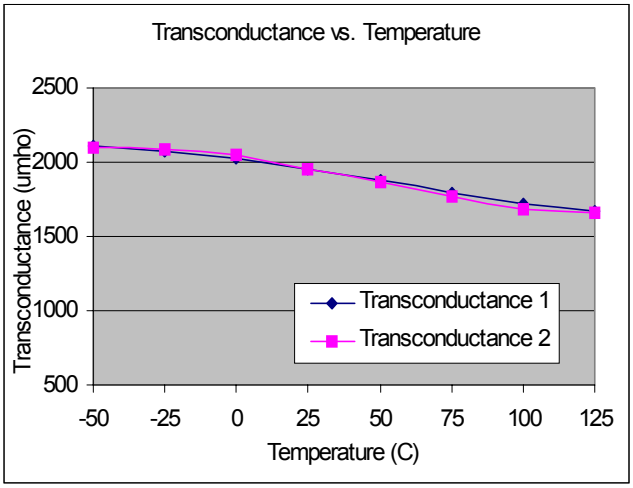




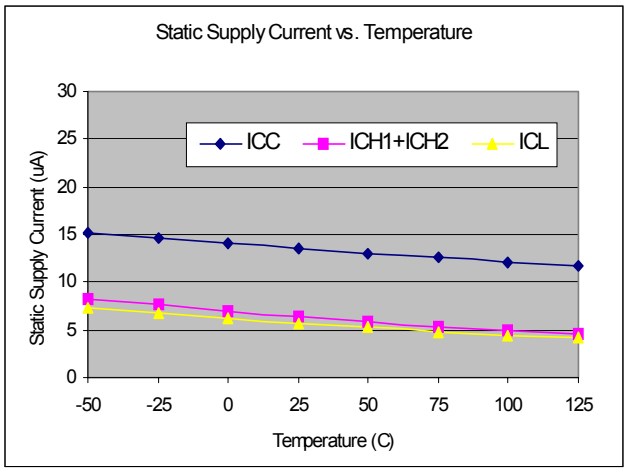


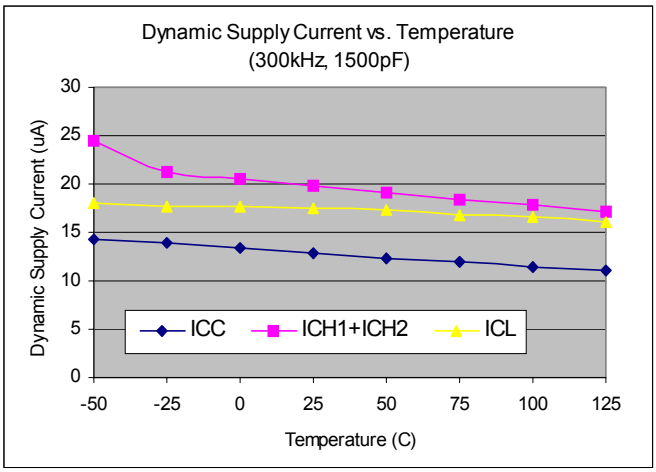


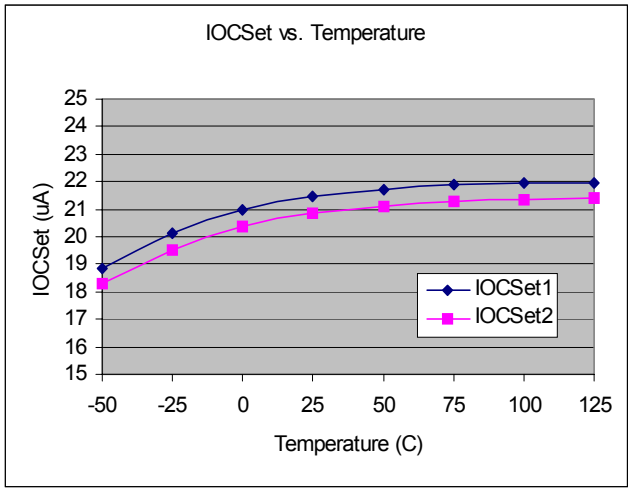


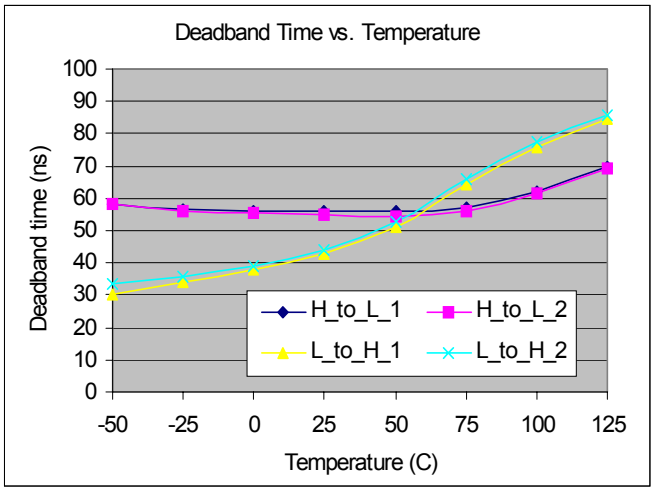


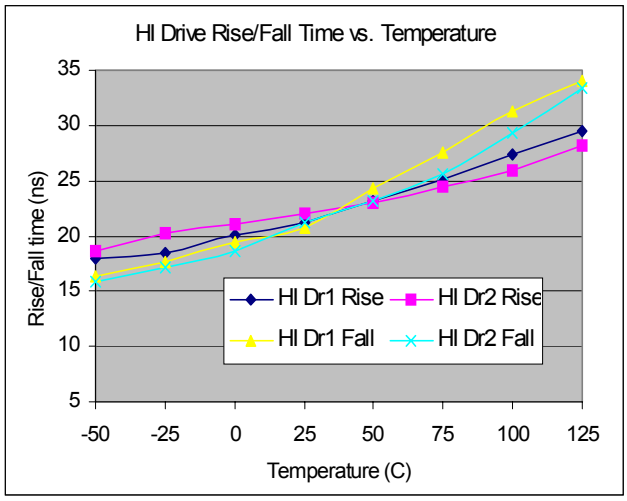
TYPICAL OPERATING CHARACTERISTICS

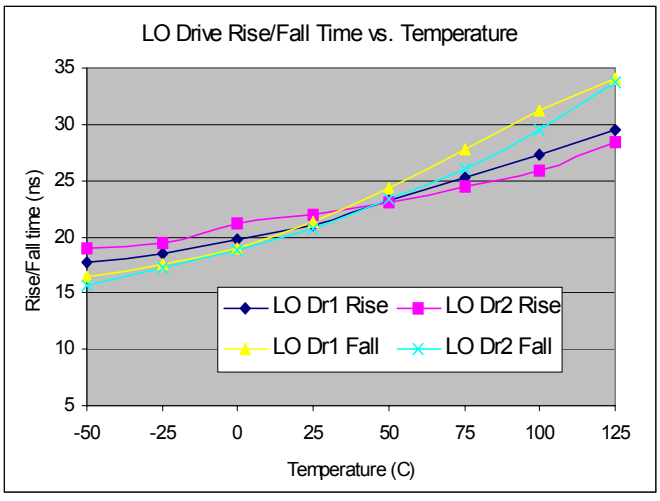












TYPICAL OPERATING WAVEFORMS

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400kHz, T_A=Room Temp, No Air Flow Unless otherwise specified.

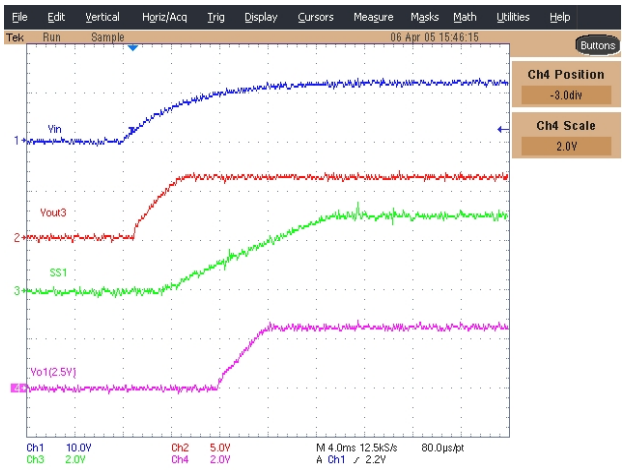


Figure 21 - Start up waveforms for 2.5V output
Ch1: Vin, Ch2: Vout3, Ch3: SS1, Ch4:Vo1 (2.5V)

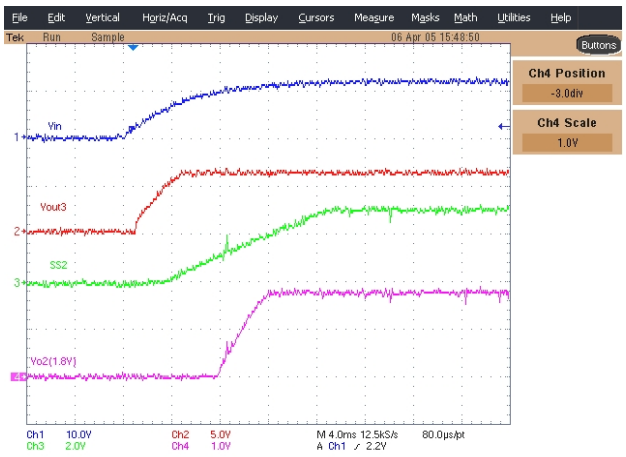


Figure 22 - Start up waveforms for 1.8V output
Ch1: Vin, Ch2: Vout3, Ch3: SS2, Ch4:Vo2 (1.8V)

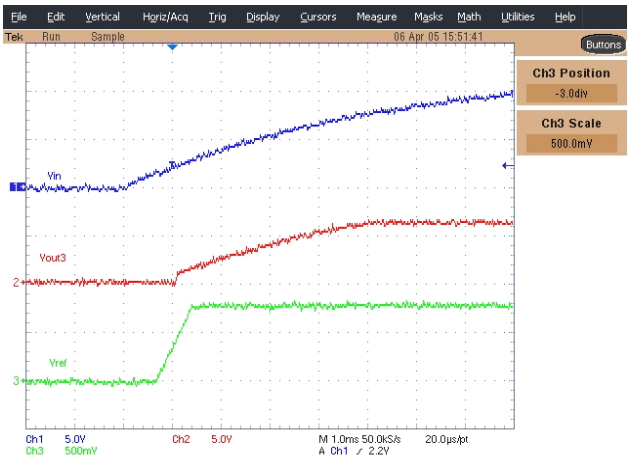


Figure 23 - Start up waveforms
Ch1: Vin, Ch2: Vout3, Ch3: Vref

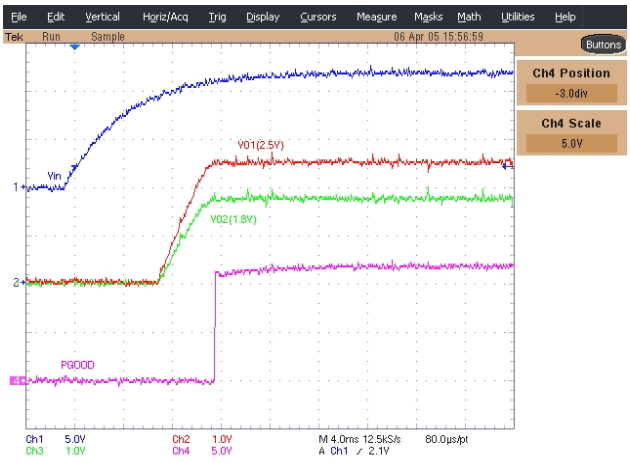


Figure 24 - Vo1, Vo2 and PGood
Ch1: Vin, Ch2: Vo1, Ch3: Vo2, Ch4: PGood

TYPICAL OPERATING WAVEFORMS

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400kHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

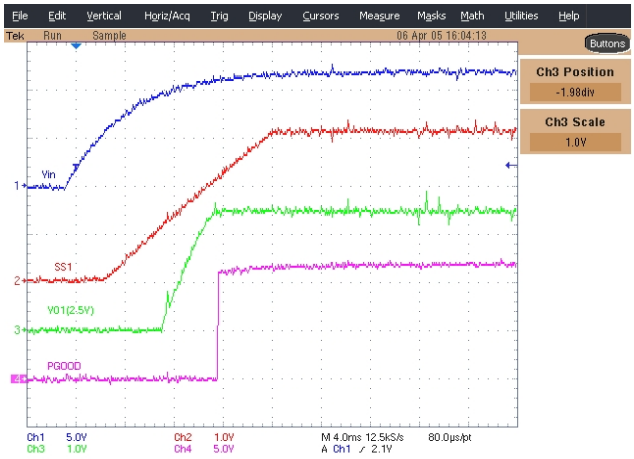


Figure 25 - 2.5V output
Ch1: Vin, Ch2: SS1, Ch3: Vo1, Ch4: PGood

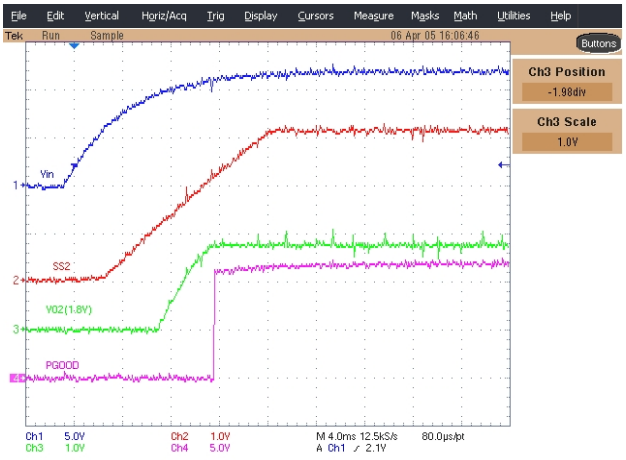


Figure 26 - 1.8V output
Ch1: Vin, Ch2: SS2, Ch3: Vo2, Ch4: PGood

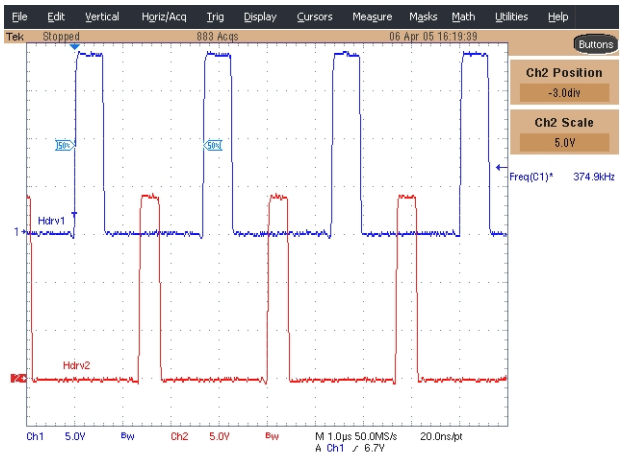


Figure 27 - Gate waveforms with 180° out of phase
Ch1: Hdrv1, Ch2: Hdrv2

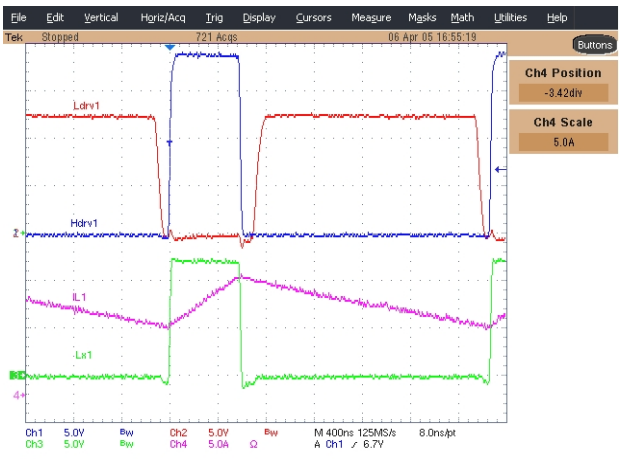


Figure 28 - 2.5V Waveforms
Ch1: Hdrv1, Ch2: Ldrv1, Ch3: Lx1, Ch4: Inductor Current

TYPICAL OPERATING WAVEFORMS

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400kHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

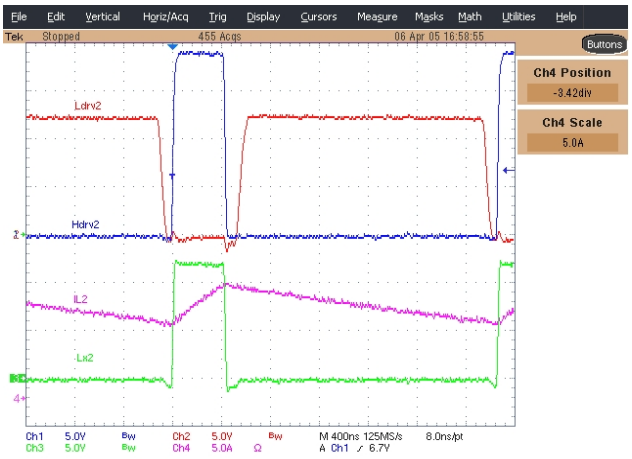


Figure 29 - 2.5V Waveforms
Ch1: Hdrv2, Ch2: Ldrv2, Ch3: Lx2, Ch4: Inductor Current

Figure 30 - 1.8V output shorted
Ch1: Vo1, Ch2: SS2, Ch3: Inductor Current

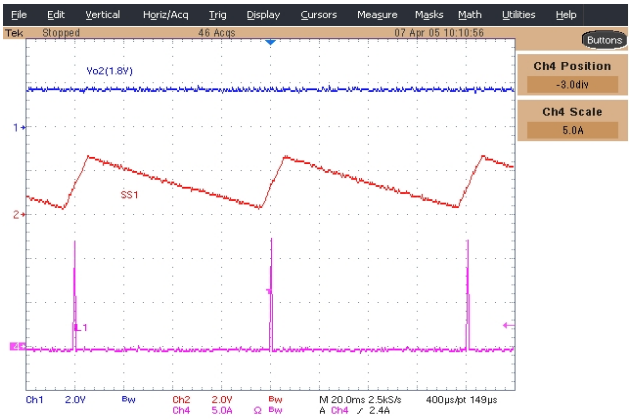


Figure 31 - 2.5V output shorted
Ch1: Vo2, Ch2: SS1, Ch3: Inductor Current

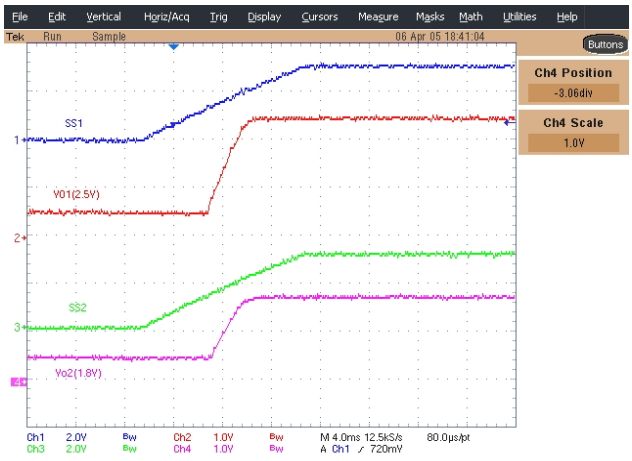


Figure 32 - Prebias Start up
Ch1: SS1, Ch2: Vo1, Ch3: SS2, Ch4:Vo2

TYPICAL OPERATING WAVEFORMS

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400kHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

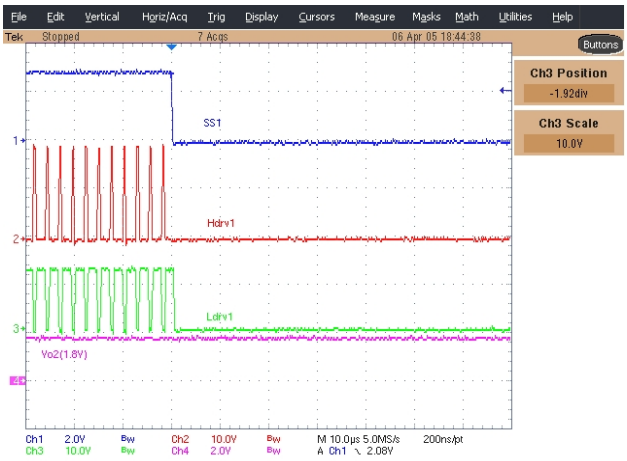


Figure 33 - SS1 pin shorted to Gnd
Ch1: SS1, Ch2: Hdrv1, Ch3: Ldrv1, Ch4:Vo2

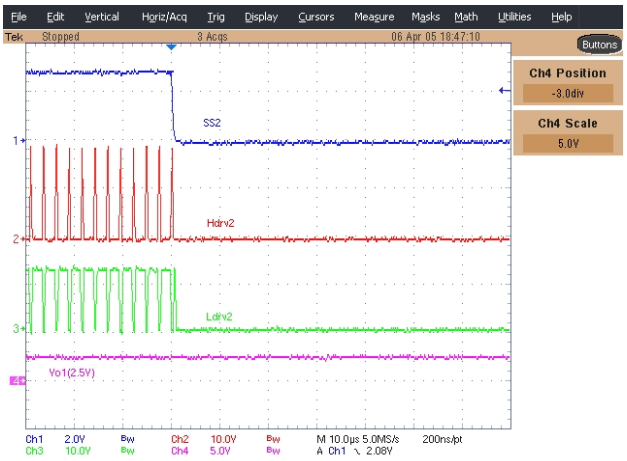


Figure 34 - SS2 pin shorted to Gnd
Ch1: SS2, Ch2: Hdrv2, Ch3: Ldrv2, Ch4:Vo1

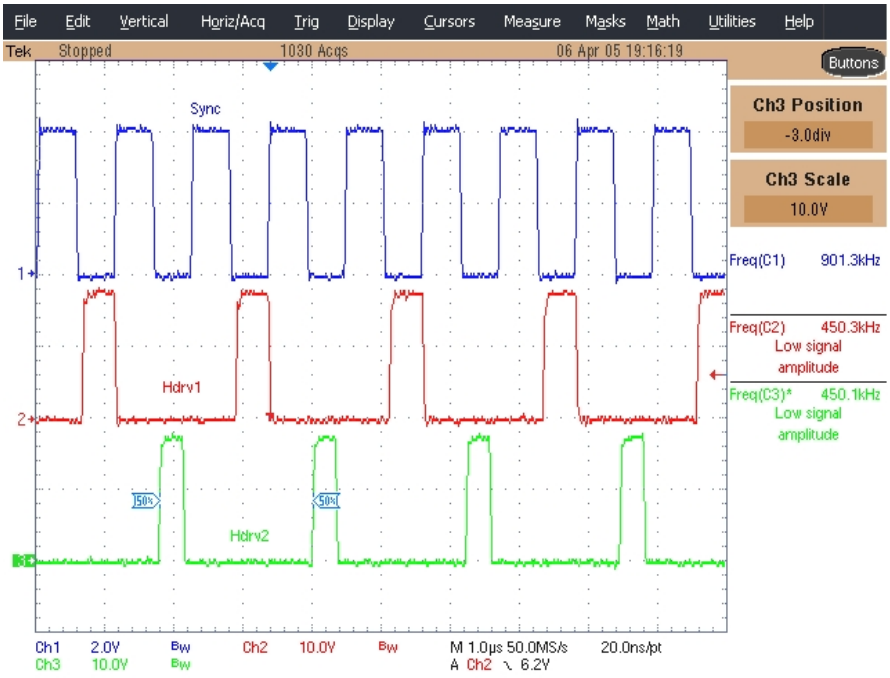


Figure 35 - External Synchronization
Ch1: External Clock, Ch2: Hdrv1, Ch3: Hdrv2

TYPICAL OPERATING WAVEFORMS

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400kHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

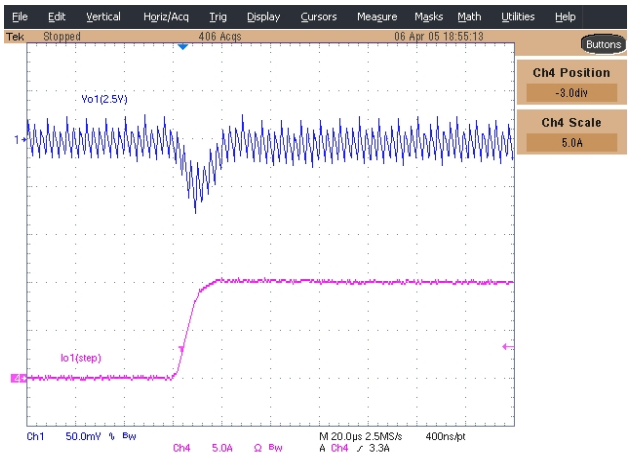


Figure 36 - Load Transient Respons for Vo1
(Io=0 to 10A)
Ch1: Vo1, Ch4:Io1

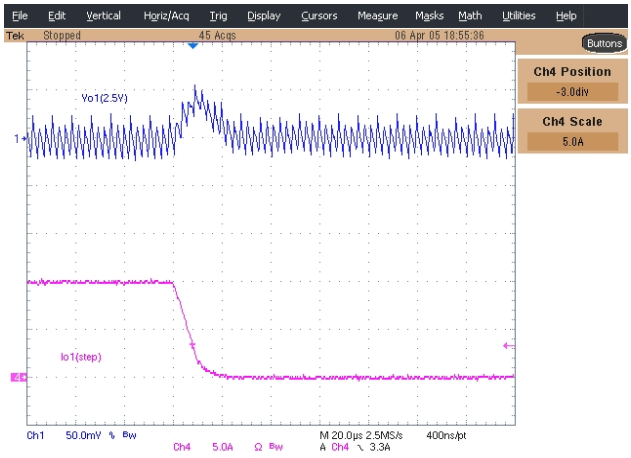


Figure 37 - Load Transient Respons for Vo1
(Io=10 to 0A)
Ch1: Vo1, Ch4: Io1

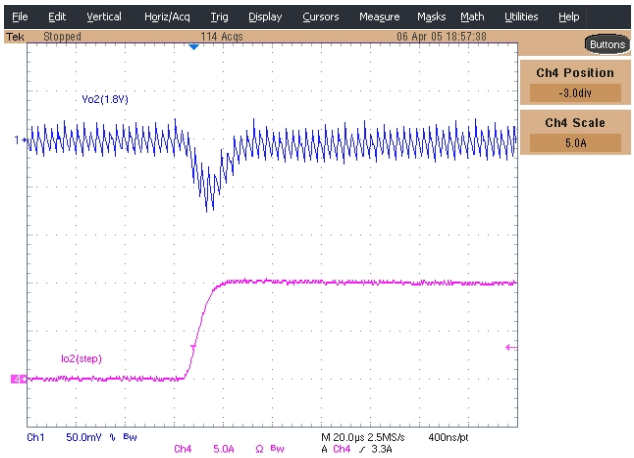


Figure 38 - Load Transient Respons for Vo2
(Io=0 to 10A)
Ch1: Vo2, Ch4: Io2

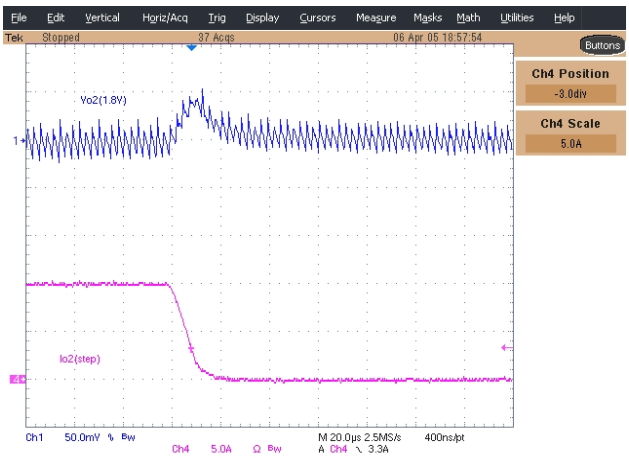


Figure 39 - Load Transient Respons for Vo2
(Io=10 to 0A)
Ch1: Vo2, Ch4: Io2

TYPICAL PERFORMANCE CURVES

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400kHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

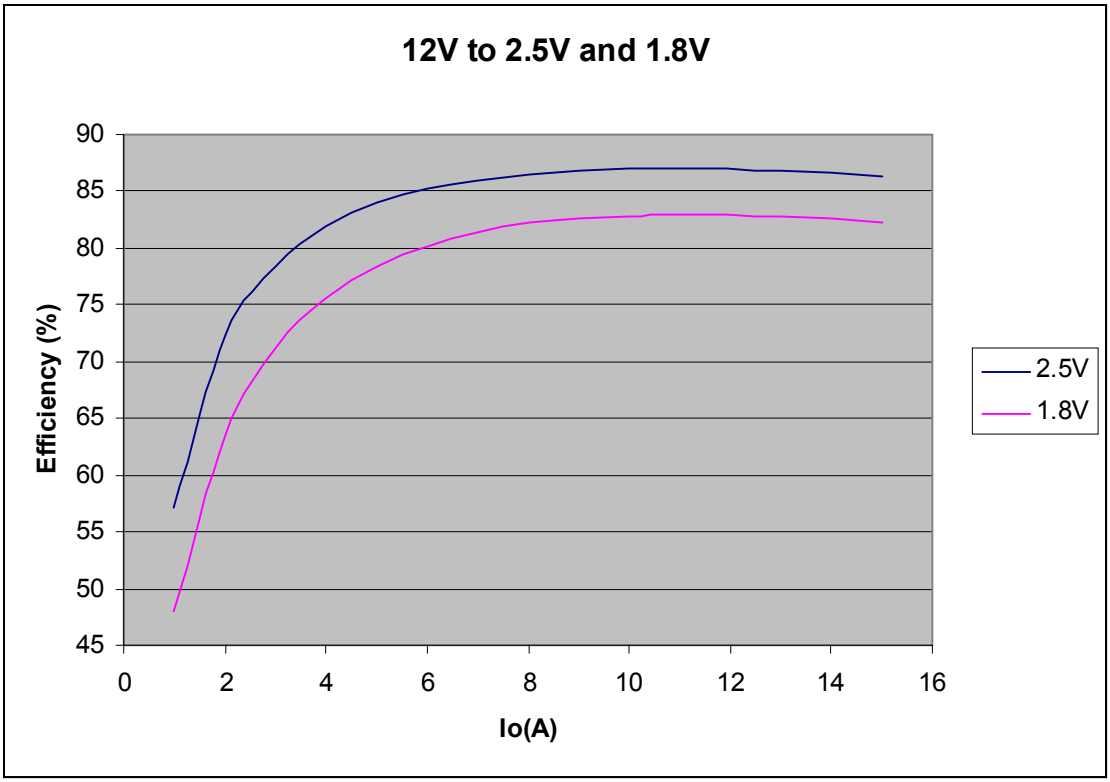
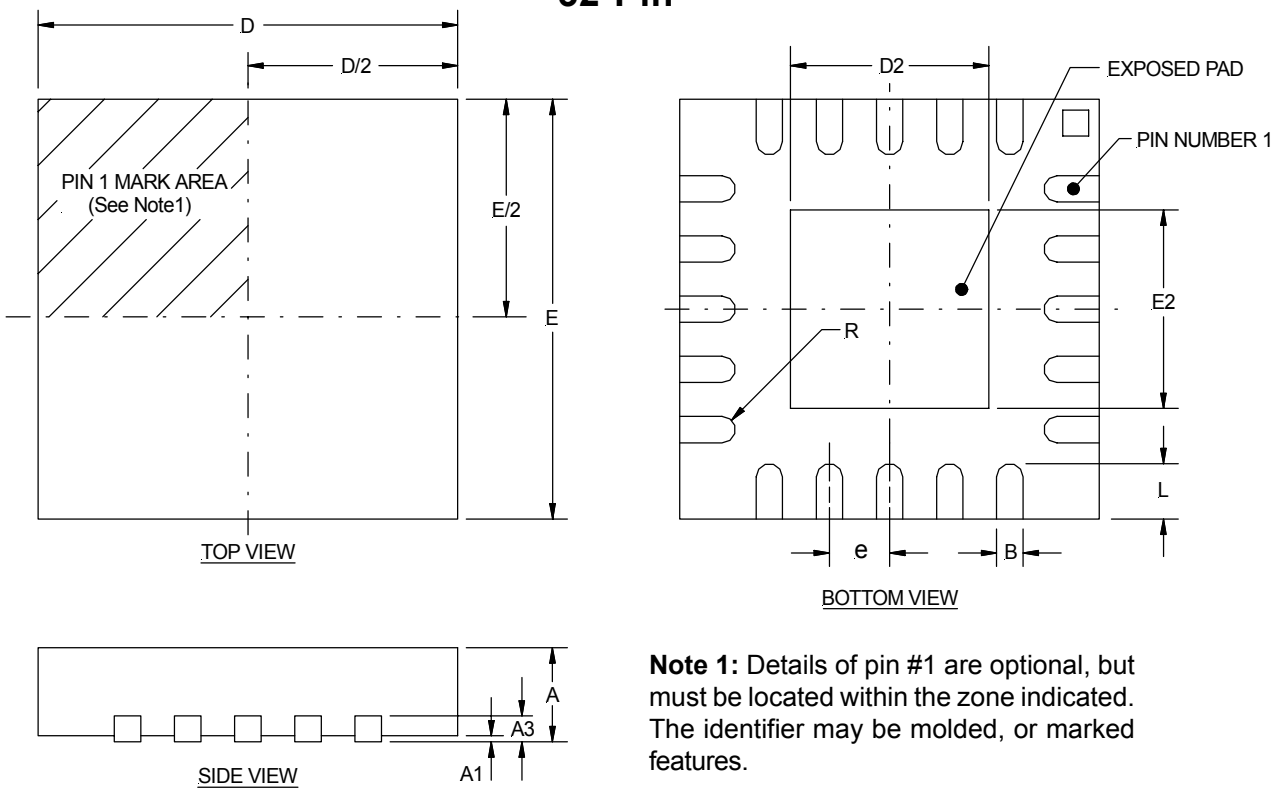


Figure 40 - Efficiency for 2.5V and 1.8V outputs at room temperature and no air flow. Efficiency was measured when the other output was operating at no load.

(IR3621M) MLPQ 5x5 Package
32-Pin

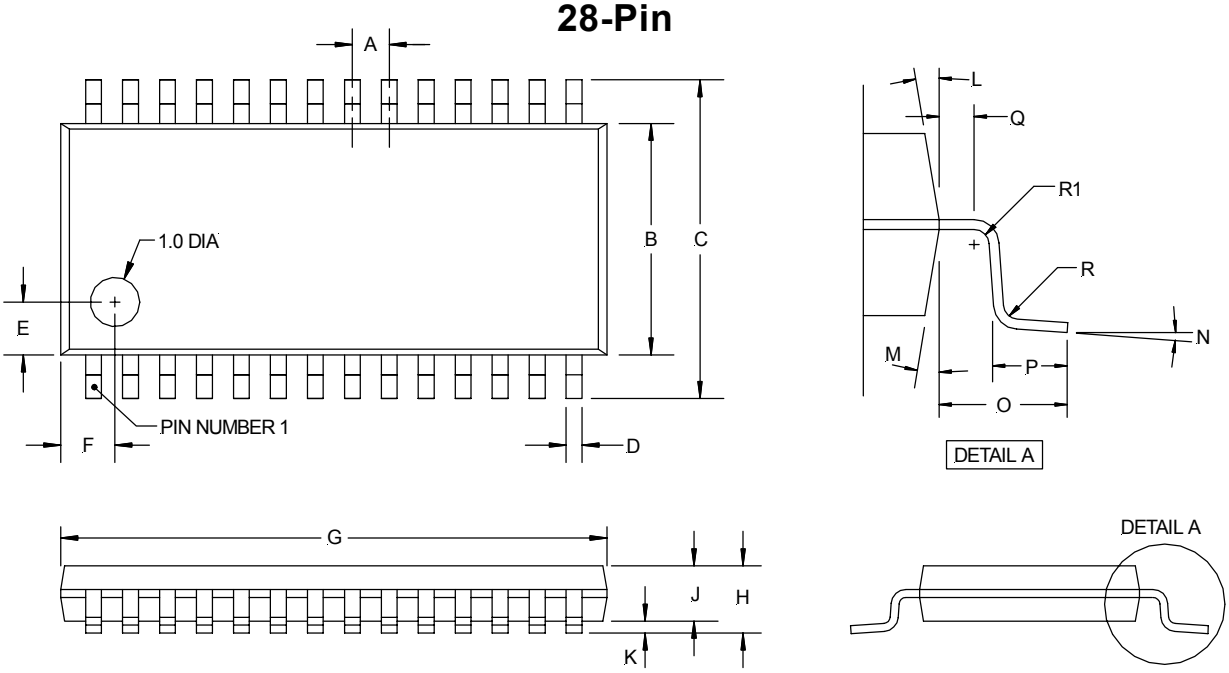


Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

SYMBOL	32-PIN 5x5		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		5.00 BSC	
D2	3.30	3.45	3.55
E		5.00 BSC	
E2	3.30	3.45	3.55
e		0.50 BSC	
L	0.30	0.40	0.50
R	0.09	---	---

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(IR3621F) TSSOP Package
28-Pin



SYMBOL	28-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	9.60	9.70	9.80
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

TAPE & REEL ORIENTATION

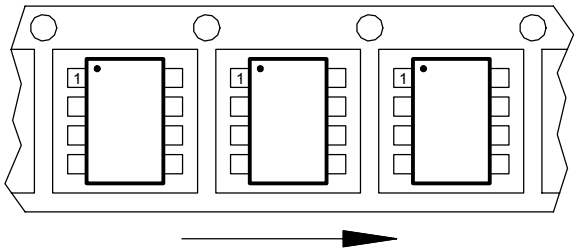


Figure A : Feed Direction

International
IOR Rectifier

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TAC Fax: (310) 252-7903

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Data and specifications subject to change without notice. 6/23/2005