

## 2,048-BIT SERIAL ELECTRICALLY ERASABLE PROM

MARCH 2001

### FEATURES

- State-of-the-art architecture
  - Non-volatile data storage
  - Low voltage operation:
    - 3.0V ( $V_{CC} = 2.7V$  to  $6.0V$ )
  - Full TTL compatible inputs and outputs
  - Auto increment for efficient data dump
- Low voltage read operation
  - Down to 2.7V
- Hardware and software write protection
  - Defaults to write-disabled state at power-up
  - Software instructions for write-enable/disable
- Advanced low voltage CMOS E<sup>2</sup>PROM technology
- Versatile, easy-to-use Interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming status indicator
  - Word and chip erasable
  - Stop SK anytime for power savings
- Durable and reliable
  - 10-year data retention after 100K write cycles
  - 100,000 write cycles
  - Unlimited read cycles

### OVERVIEW

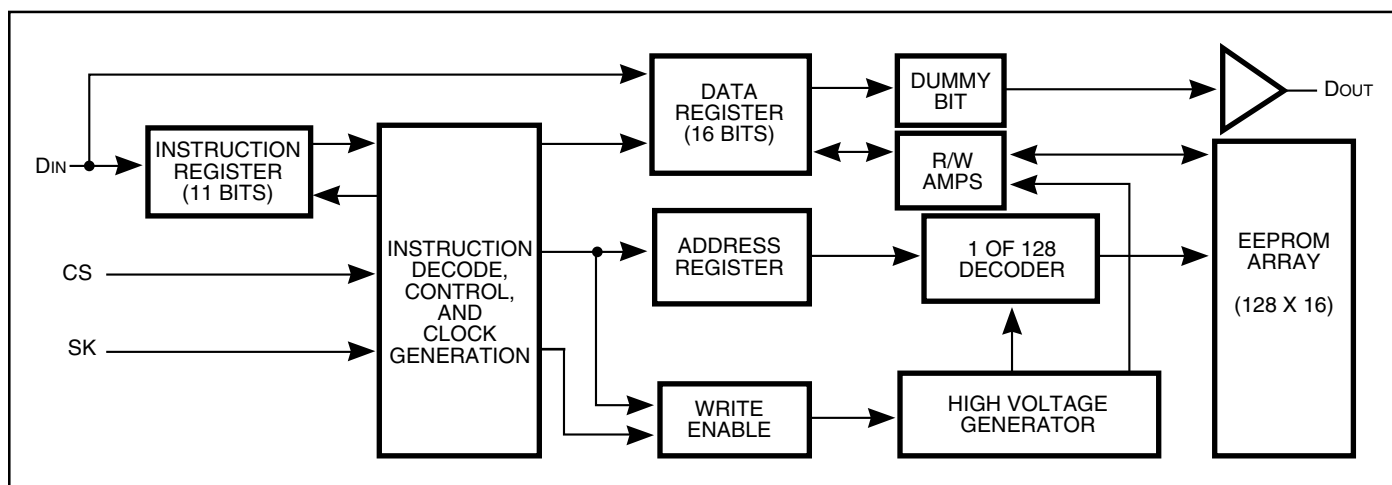
The IS93C56-3 is a low cost 2,048-bit, non-volatile, serial E<sup>2</sup>PROM. It is fabricated using *ISSI's* advanced CMOS E<sup>2</sup>PROM technology. The IS93C56-3 provides efficient non-volatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which includes read, write, and mode enable functions. The data out pin (D<sub>OUT</sub>) indicates the status of the device during in the self-timed non-volatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (D<sub>OUT</sub>) pin will indicate the READY/BUSY status of the chip.

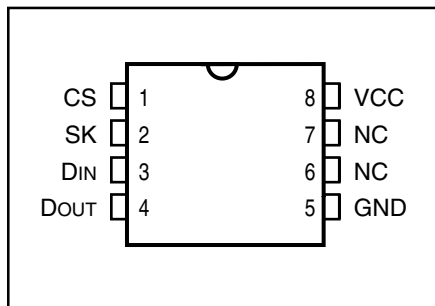
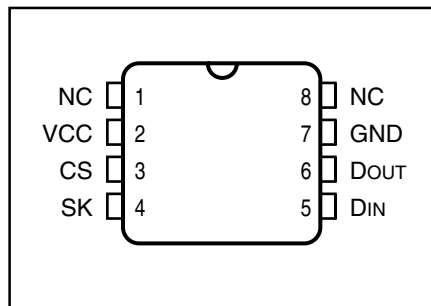
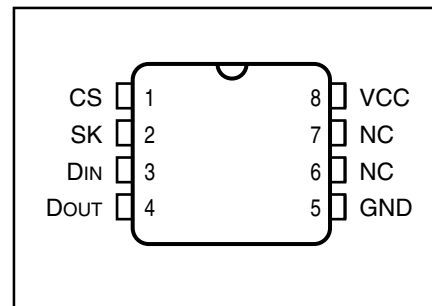
### APPLICATIONS

The IS93C56-3 is ideal for high-volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

### FUNCTIONAL BLOCK DIAGRAM



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**PIN CONFIGURATION****8-Pin DIP****PIN CONFIGURATION****8-Pin JEDEC Small Outline "G"****PIN CONFIGURATION****8-Pin JEDEC Small Outline "GR"****PIN DESCRIPTIONS**

CS	Chip Select
SK	Serial Data Clock
DIN	Serial Data Input
DOUT	Serial Data Output
NC	Not Connected
Vcc	Power
GND	Ground

**ENDURANCE AND DATA RETENTION**

The IS93C56-3 is designed for applications requiring up to 100,000 programming cycles (WRITE, WRALL, ERASE and ERAL). It provides 10 years of secure data retention, without power after the execution of 100,000 programming cycles.

**DEVICE OPERATION**

The IS93C56-3 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DIN pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the IS93C56-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

**Read (READ)**

The READ instruction is the only instruction that outputs serial data on the DOUT pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DOUT changes during the low-to-high transitions of SK (see Figure 3).

**Low Voltage Read**

The IS93C56-3 has been designed to ensure that data read operations are reliable in low voltage environments. The IS93C56-3 is guaranteed to provide accurate data during read operations with Vcc as low as 2.7V.

**Auto Increment Read Operations**

In the interest of memory transfer operation applications, the IS93C56-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

**Write Enable (WEN)**

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When Vcc is applied, this device

powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until Vcc is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

### Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been applied to D<sub>IN</sub>, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250 ns (5V operation) from the falling edge of CS (t<sub>CS</sub>), if CS is brought HIGH, D<sub>OUT</sub> will indicate the READY/ $\overline{\text{BUSY}}$  status of the chip: logical “0” means programming is still in progress; logical “1” means the selected register has been written, and the part is ready for another instruction (see Figure 5). (NOTE: The combination of CS HIGH, D<sub>IN</sub> HIGH and the rising edge of the SK clock, resets the READY/ $\overline{\text{BUSY}}$  flag. Therefore, it is important if you want to access the READY/ $\overline{\text{BUSY}}$  flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

### Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. While the

WRALL instruction is being loaded, the address field becomes a sequence of “Don’t Care” bits (see Figure 6). As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250 ns (t<sub>CS</sub>), the D<sub>OUT</sub> pin indicates the READY/ $\overline{\text{BUSY}}$  status of the chip (see Figure 6).

### Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

### Erase Register (ERASE)

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t<sub>CS</sub>, will cause D<sub>OUT</sub> to indicate the READY/ $\overline{\text{BUSY}}$  status of the chip: a logical “0” indicates programming is still in progress; a logical “1” indicates the erase cycle is complete and the part is ready for another instruction (see Figure 8).

### Erase All (ERALL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical “1” (see Figure 9).

## INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A6-A0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A6-A0)	D15-D0 <sup>(1)</sup>
WRALL (Write All Registers)	1	00	01XXXXXX	D15-D0 <sup>(1)</sup>
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	X(A6-A0)	
ERALL (Erase All Registers)	1	00	10XXXXXX	

**Note:** 1. If input data is not 16 bits exactly, the last 16 bits will be taken as input data (a word).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>GND</sub>	Voltage with Respect to GND	-0.3 to +6.5	V
T <sub>BIAS</sub>	Temperature Under Bias (IS93C56-3)	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias (IS93C56-3I)	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature	-65 to +125	°C

**Notes:**

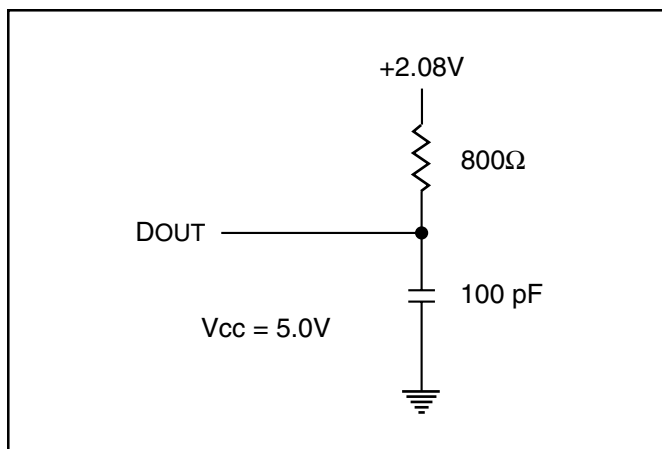
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	2.7V to 6.0V
Industrial	-40°C to +85°C	2.7V to 6.0V

**CAPACITANCE**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5	pF

**FIGURE 1. AC TEST CONDITIONS**

**DC ELECTRICAL CHARACTERISTICS**T<sub>A</sub> = 0°C to +70°C for IS93C56-3 and -40°C to +85°C for IS93C56-3I.

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	Min.	Max.	Unit
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 10 μA CMOS	2.7V to 3.3V	—	0.2	V
V <sub>OL1</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA TTL	4.5V to 5.5V	—	0.4	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -10 μA CMOS	2.7V to 3.3V	V <sub>CC</sub> - 0.2	—	V
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OH</sub> = -400 μA TTL	4.5V to 5.5V	2.4	—	V
V <sub>IH</sub>	Input HIGH Voltage		2.7V to 3.3V 4.5V to 5.5V	2.4 2	V <sub>CC</sub> V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage		2.7V to 3.3V 4.5V to 5.5V	-0.1 -0.1	0.6 0.8	V
I <sub>LI</sub>	Input Leakage	V <sub>IN</sub> = 0V to V <sub>CC</sub> (CS, SK, D <sub>IN</sub> )		1	1	μA
I <sub>LO</sub>	Output Leakage	V <sub>OUT</sub> = 0V to V <sub>CC</sub> , CS = 0V		1	1	μA

**POWER SUPPLY CHARACTERISTICS**T<sub>A</sub> = 0°C to +70°C for IS93C56-3 and -40°C to +85°C for IS93C56-3I.

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	IS93C56-3			IS93C56-3I			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	CS = V <sub>IH</sub> , SK = 500 KHz CMOS Input Levels	2.7V to 3.3V	—	0.5	2	—	0.5	2	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	CS = V <sub>IH</sub> , SK = 1 MHz CMOS Input Levels	4.5V to 5.5V	—	4	6	—	4	6	mA
I <sub>SB</sub>	Standby Current	CS = D <sub>IN</sub> = SK = 0V	2.7V to 3.3V 4.5V to 5.5V	—	2	10	—	2	10	μA

**AC ELECTRICAL CHARACTERISTICS**

TA = 0°C to +70°C for IS93C56-3 and -40°C to +85°C for IS93C56-3.

Symbol	Parameter	Test Conditions	Vcc	IS93C56-3		IS93C56-3I		Unit
				Min.	Max.	Min.	Max.	
fSK	SK Clock Frequency		2.7V to 6.0V	0	0.5	0	0.5	MHz
			4.5V to 6.0V	0	1	0	1	MHz
tSKH	SK HIGH Time		2.7V to 6.0V	500	—	500	—	ns
			4.5V to 6.0V	250	—	250	—	
tSKL	SK LOW Time		2.7V to 6.0V	1	—	1	—	µs
			4.5V to 6.0V	250	—	250	—	ns
tCS	Minimum CS LOW Time		2.7V to 6.0V	500	—	500	—	ns
			4.5V to 6.0V	250	—	250	—	
tCSS	CS Setup Time	Relative to SK	2.7V to 6.0V	100	—	100	—	ns
			4.5V to 6.0V	50	—	50	—	ns
tDIS	DIN Setup Time	Relative to SK	2.7V to 6.0V	200	—	200	—	ns
			4.5V to 6.0V	100	—	100	—	ns
tCSH	CS Hold Time	Relative to SK	2.7V to 6.0V	0	—	0	—	ns
			4.5V to 6.0V	0	—	0	—	
tDIH	DIN Hold Time	Relative to SK	2.7V to 6.0V	400	—	400	—	ns
			4.5V to 6.0V	100	—	100	—	
tPD1	Output Delay to "1"	AC Test	2.7V to 6.0V	—	500	—	500	ns
			4.5V to 6.0V	—	500	—	500	
tPD0	Output Delay to "0"	AC Test	2.7V to 6.0V	—	500	—	500	ns
			4.5V to 6.0V	—	500	—	500	
tSV	CS to Status Valid	AC Test, CL = 100 pF	2.7V to 6.0V	—	500	—	500	ns
			4.5V to 6.0V	—	500	—	500	
tDF	CS to DOUT in 3-state	CS = VIL	2.7V to 6.0V	—	200	—	200	ns
			4.5V to 6.0V	—	100	—	100	
tWP	Write Cycle Time		2.7V to 6.0V	—	10	—	10	ms
			4.5V to 6.0V	—	10	—	10	

AC WAVEFORMS

FIGURE 2. SYNCHRONOUS DATA TIMING

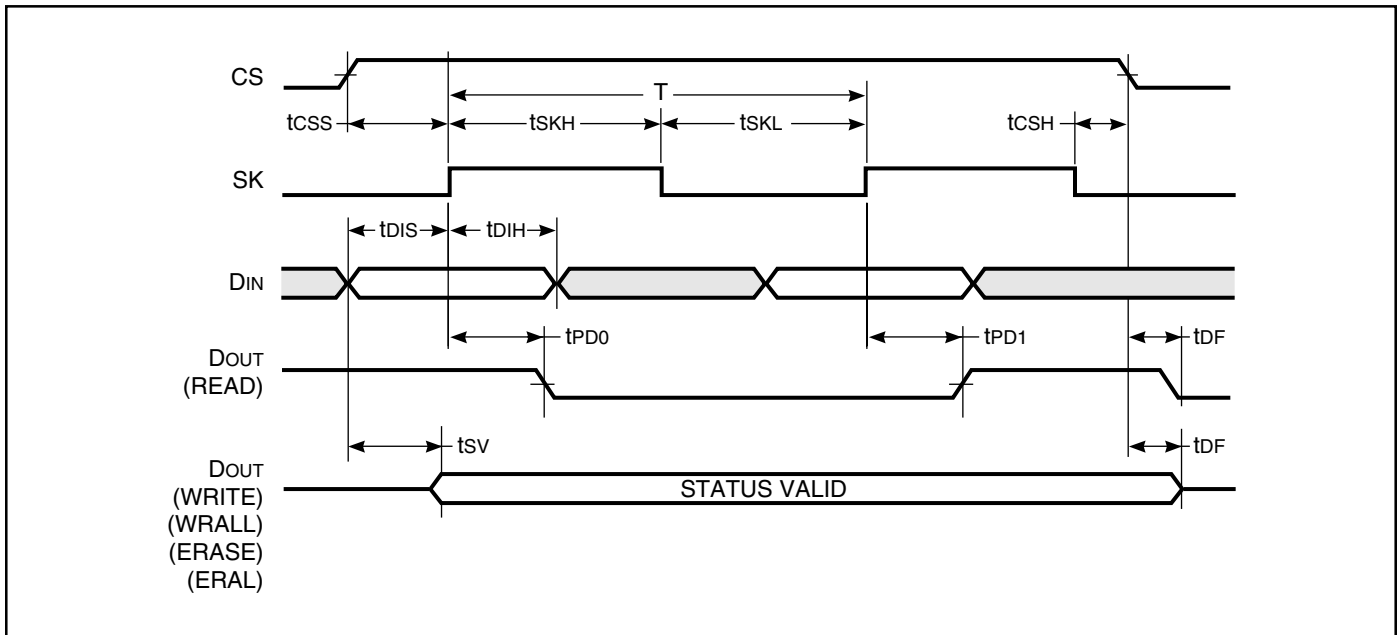


FIGURE 3. READ CYCLE TIMING

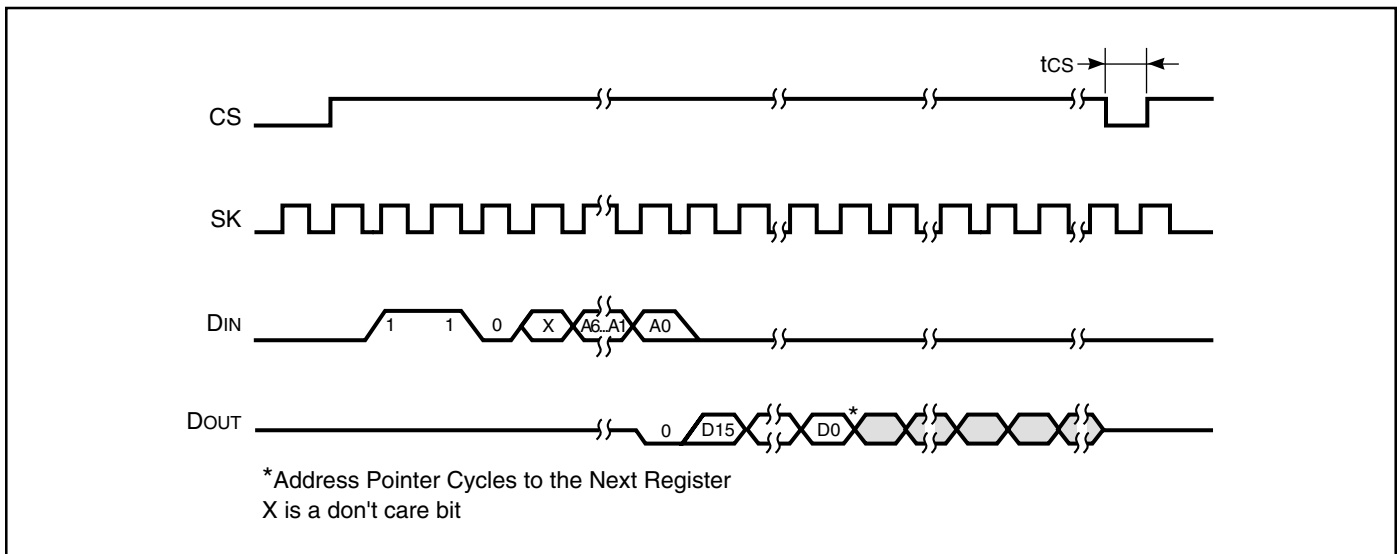


FIGURE 4. SYNCHRONOUS DATA TIMING

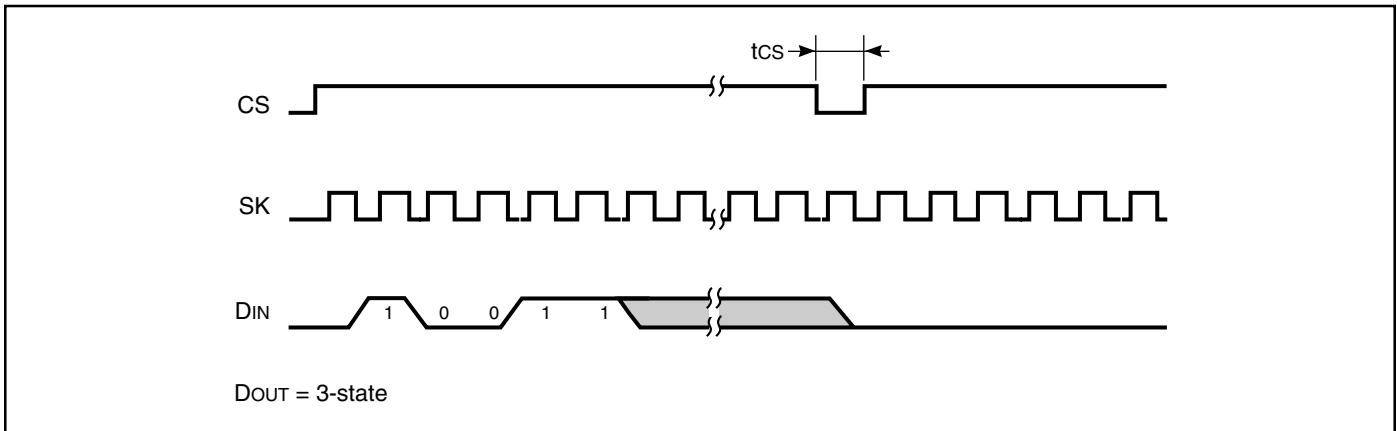


FIGURE 5. WRITE (WRITE) CYCLE TIMING

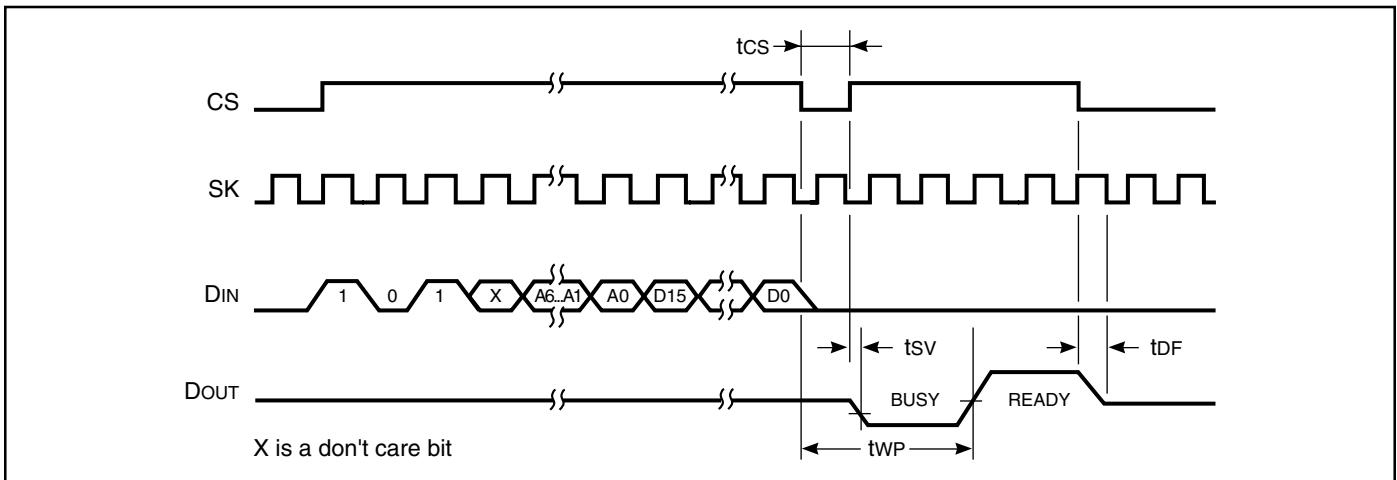
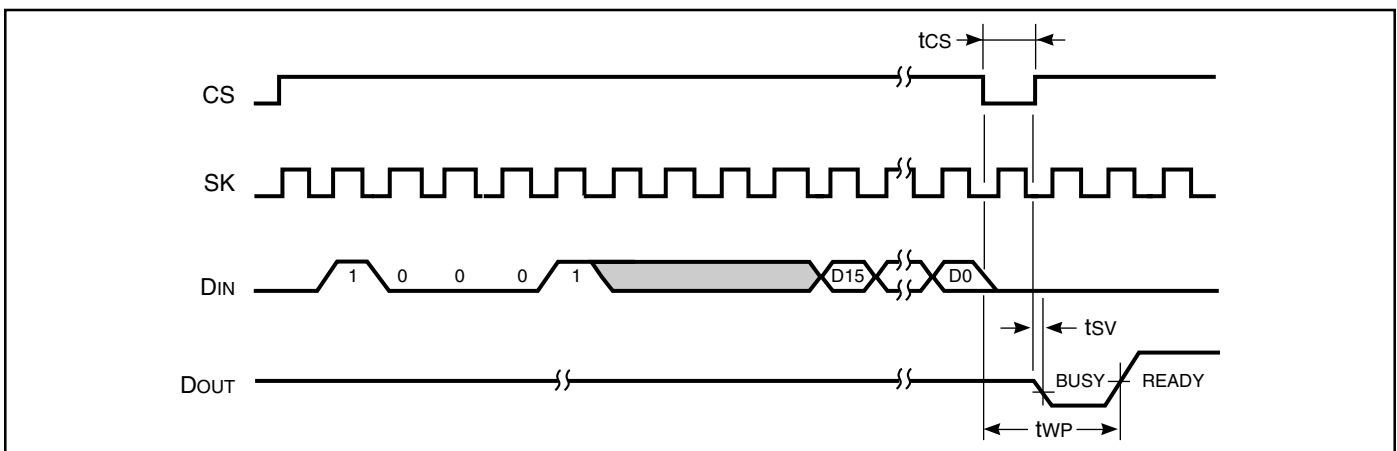
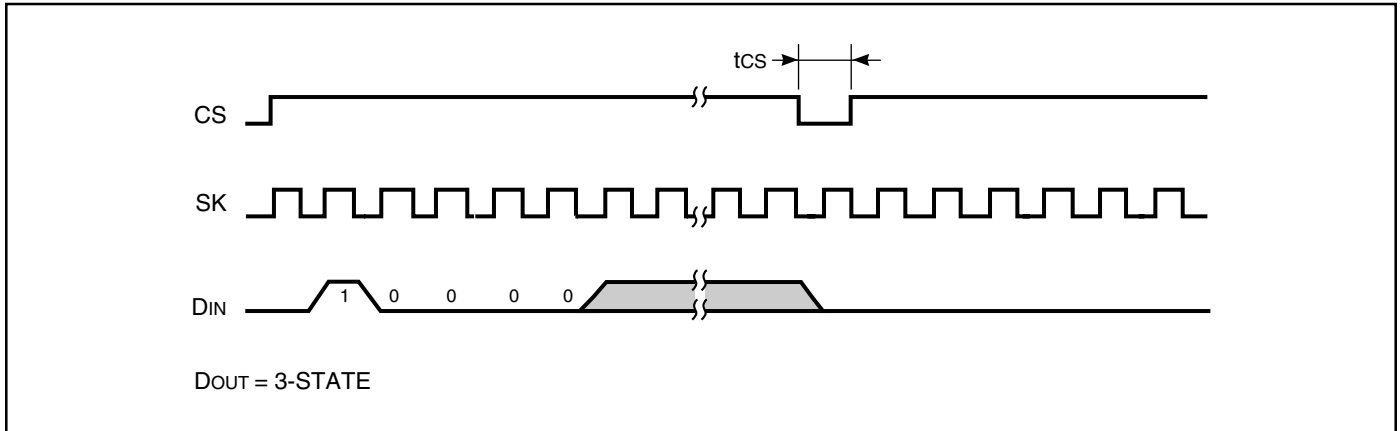


FIGURE 6. WRITE ALL (WRALL) TIMING

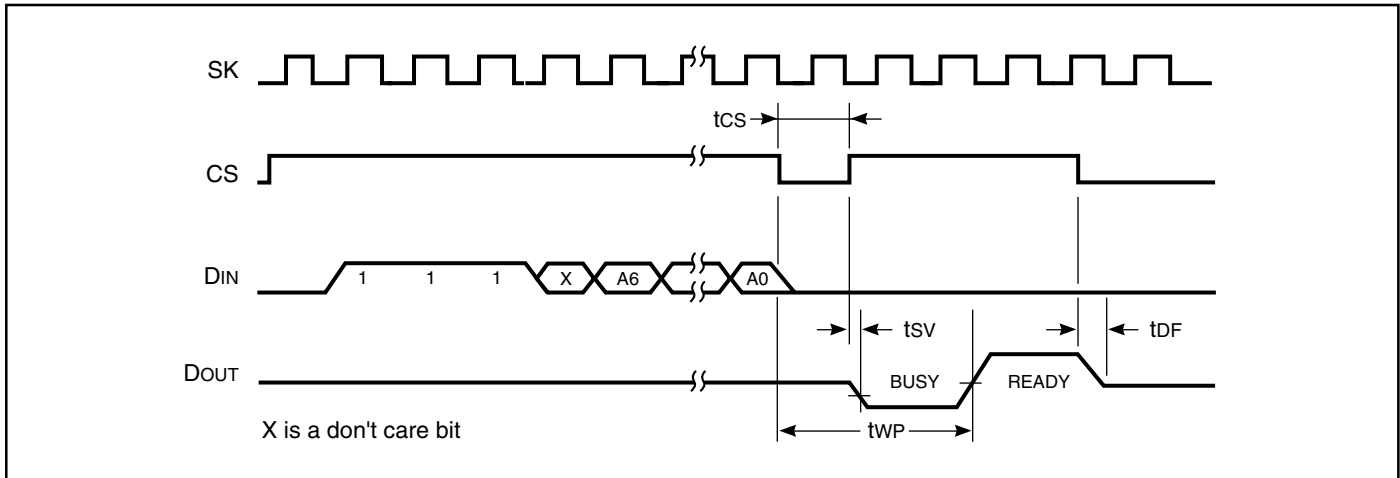




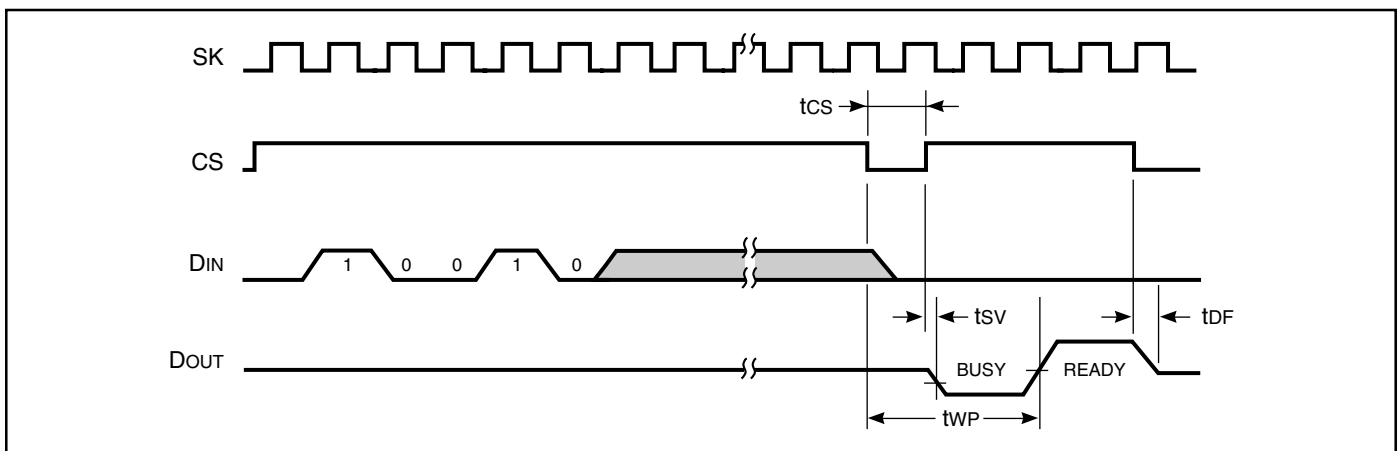
**FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING**



**FIGURE 8. ERASE (REGISTER ERASE) CYCLE TIMING**



**FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING**



**Note for Figures 8 and 9:**

After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in  $\overline{\text{BUSY}}$  status (DOUT indicates  $\overline{\text{BUSY}}$  status) then performs another instruction would cause device malfunction.

**ORDERING INFORMATION****Commercial Range: 0°C to +70°C**

Speed (MHz)	Order Part No.	Package
1	IS93C56-3P	300-mil Plastic DIP
1	IS93C56-3G	Small Outline (JEDEC)
1	IS93C56-3GR	Small Outline (JEDEC)

**ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

Speed (MHz)	Order Part No.	Package
1	IS93C56-3PI	300-mil Plastic DIP
1	IS93C56-3GI	Small Outline (JEDEC)
1	IS93C56-3GRI	Small Outline (JEDEC)

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