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A. HE8P160 Introduction

HE8P160 is a member of 8-bit Micro-controller OTP series product developed by Jess Technology Co., Ltd. This IC use OTP(One Time Programming) ROM, which can be wrote by the writer tool provided by Jess. It can provides fast verification, pilot-run product, and provide more versatile application request to user. HE8P160 is a super-set of seven IC body(HE80012S, HE80016S, HE80021S, HE83000, HE80012M, HE80016M, HE80021M, HE83115, HE83116, HE89A21, HE89R21)and internal build in 8 channel 12-bit ADC block. If user want to simulate any one of the seven IC body, The writer tool will automatically restrict the hardware resource, such as ROM - RAM size, it is very convenient to use.

This IC has build-in LCD driver which have many configuration and can use Mask Option to select the configuration, such as【128 pixel LCD driver + 16 Bit I/O Port】... 【64 pixel LCD driver + 32Bit I/O Port】. Build-in voltage regulator let LCD display stable when external battery voltage drop. The built-in OP operation amplifier can be used with (light, voice - temperature, humility) sensor and used as battery low detection. The 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism.
The instruction set of HE8P160 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B. HE8P160 Features

- Operation Voltage: 2.4V- 5.2V
- System Clock: DC ~ 8MHz @ 5.2V
  DC ~ 4MHz @ 2.4V
- Internal ROM: 64K Bytes (64K Program ROM)
- Internal RAM: 512 Bytes.
- Dual Clock System Normal (Fast) clock: 32.768K - 8MHz
  Slow clock: 32.768KHz
- Operation Mode: DUAL, FAST' SLOW' IDLE, SLEEP Mode.
- Build - in WDT (WATCH DOG TIMER) to prevent deadlock or abnormal condition..
- 16~32 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin. The I/O PRTD [3:0] each has 5mA sink capability.
- Build - in OP amplifier. This OP operating range between 0~(VDD-1) , that is different from previous OP comparator operating range between 0.8-VDD, the user should notice this. Please set the operation range on 0.8~(VDD-1) if user want to design a circuit working both on 8P160 and target IC.
- Build-in 125KHz, 8-channel 12-bit ADC block.
- Build-in voltage regulator which provide LCD stable operating voltage.
- 4 COM*32 SEG LCD driver which have A,B type. Voltage regulator circuit, please reference application circuit. The LCD highest voltage LV3 must less than 9.0 V.
- Contain a 7-bit Current-type D/A converter.
- Provide PWM output device。(Users can select with or without Rate Selection, connect with “ VDD + PWM ” or “ PWMP + PWMN ”)
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timer and one Time Base timer.
- Instruction set: 32 instructions, 4 addressing mode. 9-bit DATA POINTER for RAM and 16-bit TABLE POINTER for ROM.

C. Mask Option Comparison Table

When user use JESS writer (include application software & hardware) to write data to OTP, the user can select specific IC from software application, in the mean time, the JESS writer will set all the configuration automatically. The following table describe the configuration relative setting, if user want to use HE8P160 full function setting, please reference following setting.

NAME	Description	80012S 80016S 80021S	83000	80012M 80016M 80021M	83115	83116	89A21	89R21
MO_LDVINC	0: TP not changed at LDV 1: TP++ at LDV	User	1	1	1	1	1	1
MO_FOSCE	0: internal fast OSC 1: external fast OSC, use it now	1	User	User	User	User	User	User
MO_FXTAL	0: R/C osc. For fast clock 1: X'tal osc. For fast clock	User	User	User	User	User	User	User
MO_FRCI_S[2:0]	000: RFRC_I~=500K 001: RFRC_I~=1M 010: RFRC_I~=1.5M 011: RFRC_I~=2M 100: RFRC_I~=2.5M 101: RFRC_I~=3M 110: RFRC_I~=3.5M 111: RFRC_I~=4M	000: not exist	User	User	User	User	User	User
MO_SXTAL	0: R/C osc. For 32K clock 1: X'tal osc. For 32K clock	0: not exist	User	User	User	User	User	User
MO_FCK/SCKN	00: slow clock only 01: illeagal 10: dual clock 11: fast clock only	11	User	User	User	User	User	User
MO_WDTE	0: WDT disable 1: WDT enable	0	User	User	User	User	User	User
MO_CPP[7:4]	0: open-drain output 1: push-pull output	1	1	User	1	User	User	User
MO_CPP[3:0]	0: open-drain output 1: push-pull output	1	User	User	User	User	User	User
MO_DPP[7:0]	0: open-drain output 1: push-pull output	User	User	User	User	User	User	User
MO_14PP[7:0]	0: open-drain output 1: push-pull output	1	1	1	User	1	User	User
MO_15PP[7:0]	0: open-drain output 1: push-pull output	1	1	1	1	1	User	User
MO_LIO14[7:0]	0: IO pin 1: LCD pin	0	0	0	User	1	User	User
MO_LIO15[7:0]	0: IO pin 1: LCD pin	0	0	0	0	1	User	User
MO_DTMFSCK	0: DTMF clock source 3.58 MHz 1: DTMF clock source 32768 Hz	0	0	0	0	0	User	User
MO_LVRG	0: LCD regulator disable 1: LCD rgulator enable	0	0	0	0	0	0	User
MO_PRTC_ADC[7:0]	0: IO pin 1: ADC input	0	0	0	0	0	0	0
MO_PRTD_HIC[3:0]	0: 2mA IoL 1: 5mA IoL	0	0	0	0	0	0	0
MO_PROTECTN	0: OTP read protect 1: OTP not protect	User	User	User	User	User	User	User

MO_ROM[1:0]	00: ROM 4k byte 01: ROM 8k byte 10: ROM 16k byte 11: ROM 64k byte	11	00	11	11	11	10	10
MO_RAM[1:0]	00: RAM 64 byte 01: RAM 128 byte 10: RAM 256 byte 11: RAM 512 byte	01	00	01	10	10	11	11
MO_TC2	0: TC2 not exist 1: TC2 exist	0	1	1	1	1	1	1
MO_TB	0: TB not exist 1: TB exist	0	0	0	0	0	1	1
MO_PRT0C[1:0]	00: prt0C not exist 01: only prt0C[3:0] exist 10: only prt0C[7:4] exist 11: prt0C exist	00	01	11	01	11	11	11
MO_PRT14	0: prt14 not exist 1: prt14 exist	0	0	0	1	0	1	1
MO_PRT15	0: prt15 not exist 1: prt15 exist	0	0	0	0	0	1	1
MO_PRT14_SS	0: prt14[7:0]=SEG[19:12] 1: prt14[7:0]=SEG[23:16]	0	0	0	0	1	1	1
MO_LCD	0: LCD not exist 1: LCD exist	0	0	0	1	1	1	1
MO_PWM[1:0]	00: PWM not exist 01: PWM logic 10: PWM1 logic 11: PWM not exist	10	00	10	10	01	00	00
MO_PMD	0: PWMP/PWMN output 1: PWM/GND_PWM output	1	0	0	0	0	0	0
MO_VO	0: DAC not exist 1: DAC exist	1	0	1	1	1	0	0
MO_OPAMP	0: Opamp not exist 1: Opamp exist	0	1	1	1	1	0	0
MO_DTMF	0: DTMF not exist 1: DTMF exist	0	0	0	0	0	1	1

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D. Pin Description

Pin	Pin-Name	I/O	Function	Description
52, 51	**FXI,** **FXO**	B, O	External fast clock pin. Connection to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask Option setting ： MO_FCK / SCKN = 00: Slow clock only 0l: Illegal 10: Dual Clock 11: Fast Clock only MO_FOSCE = 0：Internal fast osc. 1：External fast osc. MO_FXTAL = 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL = 0：RC for 32.768 Hz clock =1 : X'tal for 32.768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL , SLOW , IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
55, 54	**SXI,** **SXO**	I, O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER 1, Time-Base and other internal blocks.	
50	**RSTP_N**	I	System Reset	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides , MO_WDTE can set Watch Dog Timer: MO_WDTE = 0：Disable Watch Dog Timer = 1：Enable Watch Dog Timer
53	**TSTP_P**	I	Test Pin , active high.	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
82,83, 1..6	**PRTC[7:0]** **/ADC[7:0];**	B	Port C bi-directional I/O pin ，total 8 pin or **ADC [7 : 0]** can used as 8-channel ADC Data Input Pin .	Mask Options **:** MO_CPP [7..0] = 1 ~ Push-pull = 0 ~ Open-drain when use them as input (No tri-state structure), it must Output " 1 " before reading.
70..77	**PRTD[7:0]**	B	8-pin bi-directional I/O port, PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask Options **:** MO_DPP [7..0] = l ~ Push-pull = 0 ~ Open-drain when use them as input (No tri-state structure), it must Output " 1 " before reading
16..23	**PRT14[7:0]** **/SEG[23:16]**	B/ O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask Options **:** MO_LIO14 [7..0] = l ~ LCD Pin. = 0 ~ I/O Pin. MO_14PP [7..0] = l ~ Push-pull = 0 ~ Open-drain when use them as input (No tri-state structure), it must Output " 1 " before reading
8..15	**PRT15[7:0]** **/SEG[31:24]**	B/ O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask Options **:** MO_LIO15 [7..0] = l ~ LCD Pin. = 0 ~ I/O Pin. MO_15PP [7..0] = l ~ Push-pull = 0 ~ Open-drain Output must be " 1 " before reading whenever use them as input (No tri-state structure).

40..43	**COM[3:0]**	O	LCD COMmon Output	Please reference LCD and RAM map.
24..31	**SEG[15:8]/D[7:0]**	O	LCD segment Output / OTP writing pin	These are LCD segment and OTP Writer share pin , User Must refer standard interface to arrange these pins on PCB board, let JESS writer can write data to OTP . These Pins are LCD segment pin on normal mode.
32	**SEG[7]/SDO**	O	Segment / OTP writing pin	
33	**SEG[6]/SDI**	O	Segment / OTP writing pin	
34	**SEG[5]/SCLK**	O	Segment / OTP writing pin	
35	**SEG[4]/D_CN**	O	Segment / OTP writing pin	
36	**SEG[3]/R_WN**	O	Segment / OTP writing pin	
37	**SEG[2]/P_SN**	O	Segment / OTP writing pin	
38,39	**SEG[1:0]**	O	LCD Segment Output	
45	**LC2**	B	Charge Pump Switch l	Refer Application circuit.
44	**LC1**	B	Charge Pump Switch2	
48	**LV3**	B	Charge Pump V3	
47	**LV2**	B	Charge Pump V2	
46	**LV1**	B	Charge Pump V1	
63	**PWM**	O	The PWM output can drive speaker or buzzer directly.	Set VOC register's Bit2：PWM=l ; turn on PWM。
65	**PWMP**	O	The PWM positive output can drive speaker or buzzer directly.	Set VOC register's Bit2：PWM =1 ; turn on PWM。
64	**PWMN**	O	The PWM negative output can drive speaker or buzzer directly.	Set VOC register's Bit2：PWM=1 ; turn on PWM。
69	**VO**	O	D/A voice output.	Set VOC register's Bit l：DA=1 ; turn on VO。
67	**OPIN**	I	Negative input of OP comparator	Set the bit0 (OP = 1) of VOC register to turn on OP comparator. The operating range between 0~(VDD-1)
68	**OPIP**	I	Positive input of OP comparator	
66	**OPO**	O	OPAM output pin	
59	**DTMFO**	O	DTMF Output	Through Portl2，can turn on /off **DTMF& write data**。Use Mask Option MO_DTMFSCK set clock source **:** MO_DTMFSCK = 0 ; Clock Source=3.579545 MHz = l ; Clock Source=32768 Hz
58	**MUTE**	O	MUTE Output for Dialer	Through Port12，can turn on/off **MUTE**。
60	**SDO**	O	SDO for Dialer Application	Through Portl2，can turn on/off **SDO & write data**。
61	**KEYTONE**	O	1024Hz 50％Duty Square Wave	Through Ponl2，can turn on/off **KEYTONE**。
57	**LOADER**	I	Define Loader Mode	Not open for users
78	**VREFP**	I	ADC positive Voltage reference	Tie this pin to reference Input：1V to VDDA
79	**VREFN**	I	ADC negative voltage reference	Tie this pin to VSSA
56	**VDD**	P	Digital Positive Power	Adding 0.1⌈F capacitor as by-pass Capacitor on each set is necessary. VDDA and VSSA must always tie to high and low.
49	**GND**	P	Digital Power Ground	
81	**VDDA**	P	Analog Positive Power	
80	**VSSA**	P	Analog Power Ground	
7	**VPP**	P	OTP high voltage power	
62	**GND_PWM**	P	Dedicated GND for PWM	

E. LCD RAM 的配置

Page 0:

F0H	SEG1	SEG0	F8H	SEG17	SEG16
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F1H	SEG3	SEG2	F9H	SEG19	SEG18
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F2H	SEG5	SEG4	FAH	SEG21	SEG20
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F3H	SEG7	SEG6	FBH	SEG23	SEG22
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F4H	SEG9	SEG8	FCH	SEG25	SEG24
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F5H	SEG11	SEG10	FDH	SEG27	SEG26
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F6H	SEG13	SEG12	FEH	SEG29	SEG28
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F7H	SEG15	SEG14	FFH	SEG31	SEG30
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]

F. Build-in 8-channel ADC

Built in 125KHz 8-channel 12-bit ADC block, it contain sample and hold circuit. It' s input pin share with PRTC, user can set MO_PRTC_ADC [7..0] to select what kind of input. **VREFP, VREFN, VDDA** and **VSSA** these pins connected to relative voltage according to specification, then the ADC hardware will operate correctly.

Firmware can Write / Read PRT17, then it will set to ADC control register or read data from ADC result register. Refer following table, if user want to set ADC, write to PRT17, then can set to ADC control register. Read from PRT17, then can read data from ADC result register. The read data is high byte or low nibble, depend on ADC control setting. The ADC result register has only one set, so if there are more than one channel application, it should be saved previous ADC sample data, then switch to another channel to sample ADC data again.

When ADC [7]=0, the whole ADC block will turn on. This chip provide two kind of method to start ADC convert; software interrupt & hardware interrupt (Timer). When ADC [5]=1, the start of covert ADC sample trigger by software, set ADC[6] from 0 to 1, the ADC hardware will begin to sample, the translation time must large than 150 us, the user should be notice this point, otherwise it will fetch the unstable data. The software Interrupt method' s disadvantage is that may produce jitter effect in sample data, such as voice sample. The software Interrupt method’s advantage, it can process 1 to 8 channel sample data, it is suitable for the application less sensitive on phase jitter issue. The other way can use the Timer 2 to generate hardware interrupt, when interrupt occur, the

sample data will be sampled and put in ADC result register, the user can read the sample data back to use. Use the Timer2 interrupt, it can get the advantage to avoid the phase jitter and calculation the delay sample time.

The ADC [4]: Data Select can select the sample data is high byte or low nibble. The ADC [3] Clock Source can select the clock source which is from fast clock divide by 4 or divide by 2. If fast clock greater than 8 MHz, setting ADC [3]=0, otherwise setting ADC [3] = 1. The ADC [2..0] can select one of the 8 ADC input signal channel, there is only one channel once selected.

Address	Name	Function	R/W	Width	Reset
17h : (PRT17)	ADC	ADC control / result register	R/W	8	1111 1111
ADC Control Register (Write Bit Field)					
ADC[7]	ENB	0 : ADC enable			
		1 : ADC disable ; Power-down			
ADC[6]	Start	0 -> 1 : S/W start a ADC conversion			
ADC[5]	SELTM	0 : select T2 interrupt as “start of conversion”			
		1 : select ADC[6]’s rising edge as “start of conversion”			
ADC[4]	DATASEL	0 : ADC read value = { result[3:0], 0 , 0 , 0 , 0 , }			
		1 : ADC read value = result[1:14]			
ADC[3]	CLKS	0 : ADC Clock = fast clock / 4 ; (Clock > 8MHz)			
		1 : ADC Clock = fast clock / 2 ; (Clock <= 8MHz)			
ADC[2:0]	CHNL	0 ~ 7 : select ADC input channel 0 ~ 7			
ADC Result Register (Read Bit Field)					
ADC[7:0]		Result [11:4] , or { result[3:0], 0 , 0 , 0 , 0 , }			

Following program is a ADC sample data example, please reference.

```
Tiner2::
      :
; ADC section
; Use ADC channel : PC7

        lda     #00111111b
        sta     PRT17           ; write ADC Control Register
        lda     PRT17           ; Get result [11..4] from Result Register
        sta     MemA            ; Store in “ Memory Location A ”
        lda     #00101111b
        sta     PRT17           ; write ADC Control Register
        lda     PRT17           ; Get result [3..0] from Result Register
        sta     MemB            ; Store in “ Memory Location B ”
; END ADC sectio
        :
        reti
```

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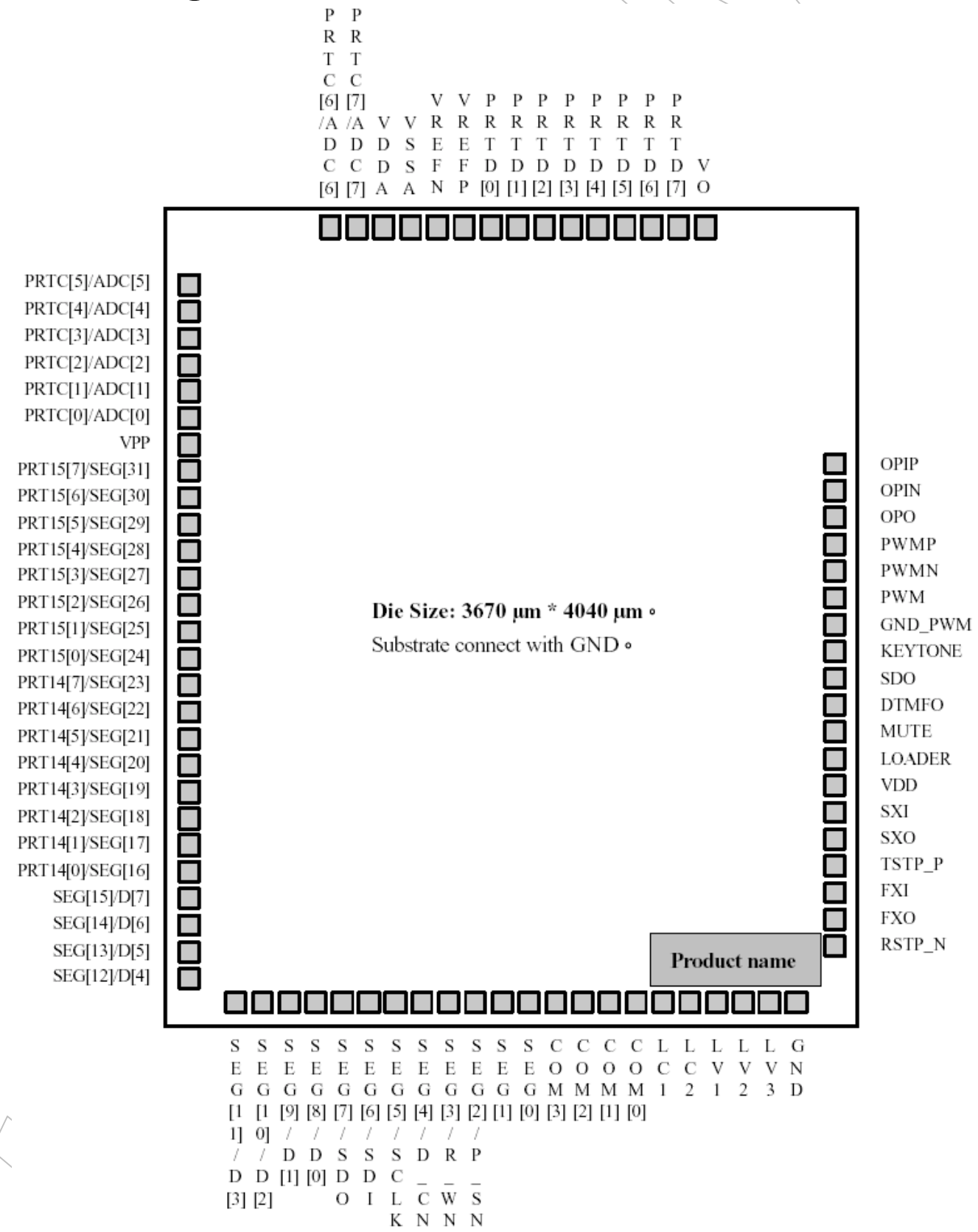
G. Pin Diagram



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H. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRTC[5]	-1700.30	1427.35	43	COM[0]	545.70	-1884.25
2	PRTC[4]	-1700.30	1306.55	44	LC1	663.80	-1884.25
3	PRTC[3]	-1700.30	1185.75	45	LC2	781.85	-1884.25
4	PRTC[2]	-1700.30	1064.95	46	LV1	899.90	-1884.25
5	PRTC[1]	-1700.30	944.15	47	LV2	1017.95	-1884.25
6	PRTC[0]	-1700.30	829.15	48	LV3	1136.00	-1884.25
7	VPP	-1700.30	699.65	49	GND	1254.05	-1884.25
8	PRT15[7]	-1700.40	566.65	50	RSTP_N	1700.40	-1580.70
9	PRT15[6]	-1700.40	451.65	51	FXO	1700.40	-1462.65
10	PRT15[5]	-1700.40	330.45	52	FXI	1700.40	-1341.85
11	PRT15[4]	-1700.40	209.25	53	TSTP_P	1700.40	-1223.80
12	PRT15[3]	-1700.40	88.05	54	SXO	1700.40	-1105.75
13	PRT15[2]	-1700.40	-33.15	55	SXI	1700.40	-987.70
14	PRT15[1]	-1700.40	-154.35	56	VDD	1700.40	-869.65
15	PRT15[0]	-1700.40	-275.55	57	LOADER	1700.40	-751.60
16	PRT14[7]	-1700.40	-396.75	58	MUTE	1700.40	-636.60
17	PRT14[6]	-1700.40	-517.95	59	DTMFO	1700.40	-512.75
18	PRT14[5]	-1700.40	-639.15	60	SDO	1700.40	-391.95
19	PRT14[4]	-1700.40	-760.35	61	KEYTONE	1700.40	-271.15
20	PRT14[3]	-1700.40	-881.55	62	GND_PWM	1700.40	-153.10
21	PRT14[2]	-1700.40	-1002.75	63	PWM	1700.40	-14.45
22	PRT14[1]	-1700.40	-1123.95	64	PWMN	1700.40	129.70
23	PRT14[0]	-1700.40	-1245.15	65	PWMP	1700.40	252.35
24	SEG[15]	-1700.30	-1369.45	66	OPO	1700.40	372.15
25	SEG[14]	-1700.30	-1488.55	67	OPIN	1700.40	490.20
26	SEG[13]	-1700.30	-1607.65	68	OPIP	1700.40	608.25
27	SEG[12]	-1700.30	-1726.75	69	VO	916.60	1884.25
28	SEG[11]	-1240.80	-1884.25	70	PRTD[7]	800.25	1884.25
29	SEG[10]	-1121.70	-1884.25	71	PRTD[6]	678.00	1884.25
30	SEG[9]	-1002.60	-1884.25	72	PRTD[5]	555.75	1884.25
31	SEG[8]	-883.50	-1884.25	73	PRTD[4]	433.50	1884.25
32	SEG[7]	-764.40	-1884.25	74	PRTD[3]	306.70	1884.25
33	SEG[6]	-645.30	-1884.25	75	PRTD[2]	179.90	1884.25
34	SEG[5]	-526.20	-1884.25	76	PRTD[1]	53.10	1884.25
35	SEG[4]	-407.10	-1884.25	77	PRTD[0]	-73.70	1884.25
36	SEG[3]	-288.00	-1884.25	78	VREFP	-197.65	1884.25
37	SEG[2]	-168.90	-1884.25	79	VREFN	-315.70	1884.25
38	SEG[1]	-49.80	-1884.25	80	VSSA	-433.75	1884.25
39	SEG[0]	69.30	-1884.25	81	VDDA	-551.80	1884.25
40	COM[3]	188.40	-1884.25	82	PRTC[7]	-672.60	1884.25
41	COM[2]	307.50	-1884.25	83	PRTC[6]	-793.40	1884.25
42	COM[1]	426.60	-1884.25				

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I. DC / AC Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0℃ ~ 70℃	
Storage Temperature	T_{st}	-50℃ ~ 100℃	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.2V	
Input Voltage	V_{ih}	0.9V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1 V_{dd}	
Operating Frequency	F_{max}	8MHz	V_{dd}=5.2V
		4MHz	V_{dd}=2.4V
Operating Temperature	T_{op}	0℃ ~ 70℃	
Storage Temperature	T_{st}	-50℃ ~ 100℃	

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Testing condition : TEMP=25℃， VDD=3V+/-10%，GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		6	9	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		4	7	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable		2	3	μA
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{PWM}	PWM Output Current	PWMP, PWMN*2	With 32Ω Loading	10	14		mA
			With 64Ω Loading	6	8		mA
			With 100Ω Loading	4	5		mA
I_{oVO}	DAC Output Current	VO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hvs}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{OL}=2.0V	50			μA
$I_{oL\ 1}$	Output Sink Current	I/O pull-low*1	V_{OL}=0.4V	1.0			mA
$I_{oL\ 2}$	Output Sink Current	PRTD [3 : 0]	V_{OL}=0.4V	5.0			mA
$I_{iL\ 1}$	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
$I_{iL\ 2}$	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only

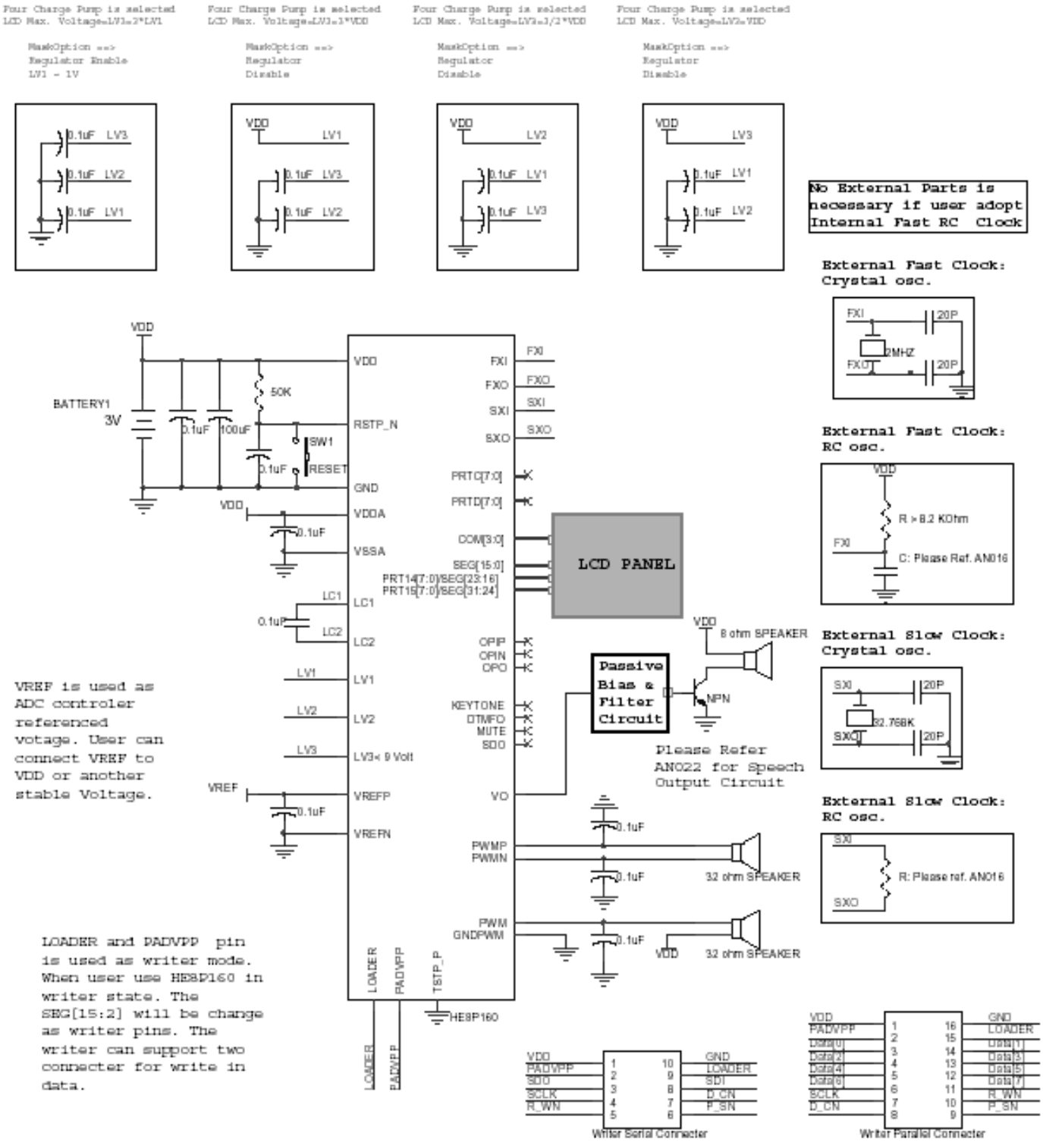
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

*2: This Spec. Base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current.

(I_{PWM}*N; N=0,1,2,3,4,5)

J. Application Circuit

About 80012S, 80016S, HE80021S, 83000, 80012M, HE80016M, HE80021M, 83115, 83116, 89A21, 89R21 and general HE80000 series application, please refer individual data sheet. The following circuit focus on ADC and Writer application.



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Writer Mode Connect Pins Definition:

Pin Nimber	HE8P160 Pin Name	Writer Mode Pin Name
24	SEG[15]	Data[7]
25	SEG[14]	Data[6]
26	SEG[13]	Data[5]
27	SEG[12]	Data[4]
28	SEG[11]	Data[3]
29	SEG[10]	Data[2]
30	SEG[9]	Data[1]
31	SEG[8]	Data[0]
32	SEG[7]	SDO
33	SEG[6]	SDI
34	SEG[5]	SCLK
35	SEG[4]	D_CN
36	SEG[3]	R_WN
37	SEG[2]	P_SN