Single Resistor Gain Programmable, Precision Instrumentation Amplifier

FEATURES

- **Single Gain Set Resistor: G = 1 to 10,000**
- **Gain Error: G = 10, 0.08% Max**
- Gain Nonlinearity: G = 10, 10ppm Max
- Input Offset Voltage: G = 10, 60μV Max
- **Input Offset Voltage Drift: 0.3μV/°C Max**
- Input Bias Current: 350pA Max
- PSRR at G = 1: 105dB Min
- CMRR at G = 1: 90dB Min
- Supply Current: 1.3mA Max
- Wide Supply Range: ±2.3V to ±18V
- 1kHz Voltage Noise: 7.5nV/√Hz
- 0.1Hz to 10Hz Noise: 0.28μV_{P-P}
- Available in 8-Pin PDIP and SO Packages
- **Meets IEC 1000-4-2 Level 4 ESD Tests with Two External 5k Resistors**

APPLICATIONS

- Bridge Amplifiers
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Differential to Single-Ended Converters
- Medical Instrumentation

DESCRIPTION

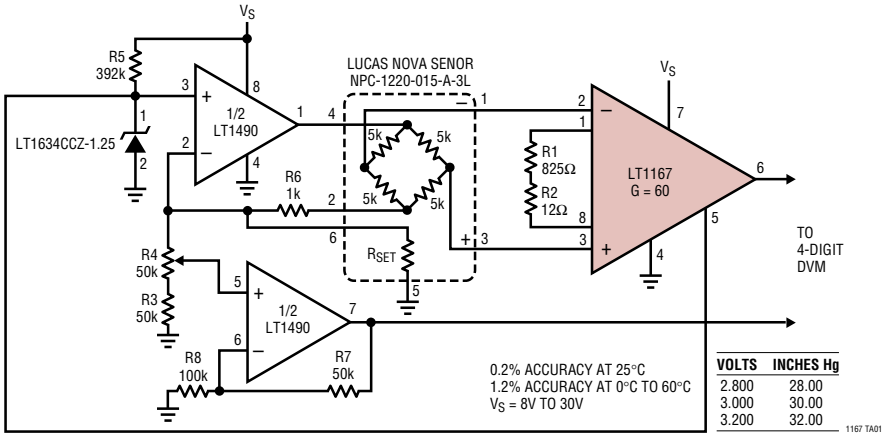
The LT®1167 is a low power, precision instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. The low voltage noise of 7.5nV/√Hz (at 1kHz) is not compromised by low power dissipation (0.9mA typical for ±2.3V to ±15V supplies).

The high accuracy of 10ppm maximum nonlinearity and 0.08% max gain error (G = 10) is not degraded even for load resistors as low as 2k (previous monolithic instrumentation amps used 10k for their nonlinearity specifications). The LT1167 is laser trimmed for very low input offset voltage (40μV max), drift (0.3μV/°C), high CMRR (90dB, G = 1) and PSRR (105dB, G = 1). Low input bias currents of 350pA max are achieved with the use of superbeta processing. The output can handle capacitive loads up to 1000pF in any gain configuration while the inputs are ESD protected up to 13kV (human body). The LT1167 with two external 5k resistors passes the IEC 1000-4-2 level 4 specification.

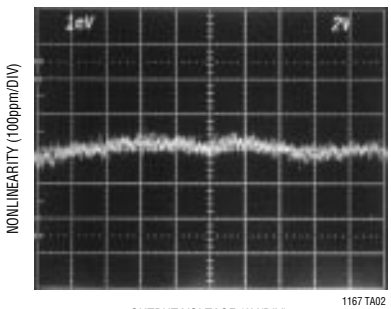
The LT1167, offered in 8-pin PDIP and SO packages, requires significantly less PC board area than discrete multi op amp and resistor designs. These advantages make the LT1167 the most cost effective solution for precision instrumentation amplifier applications.

TYPICAL APPLICATION

Single Supply Barometer



Gain Nonlinearity



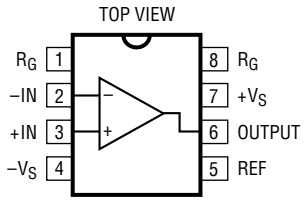
G = 1000
R_L = 1k
V_{OUT} = ±10V

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage (Within the Supply Voltage) ..... ±40V
Input Voltage (Equal to Supply Voltage) ..... ±20V
Input Current (Note 3) ..... ±20mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range
LT1167AC/LT1167C (Note 4) ..... 0°C to 70°C
LT1167AI/LT1167I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1167ACN8 LT1167ACS8 LT1167AIN8 LT1167AIS8 LT1167CN8 LT1167CS8 LT1167IN8 LT1167IS8
S8 PART MARKING
1167A 1167 1167AI 1167I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, R_L = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)	LT1167AC/LT1167AI MIN	LT1167AC/LT1167AI TYP	LT1167AC/LT1167AI MAX	LT1167C/LT1167I MIN	LT1167C/LT1167I TYP	LT1167C/LT1167I MAX	UNITS
G	Gain Range	G = 1 + (49.4k/R_G)	1		10k	1		10k	
	Gain Error	G = 1		0.008	0.02		0.015	0.03	%
		G = 10 (Note 2)		0.010	0.08		0.020	0.10	%
		G = 100 (Note 2)		0.025	0.08		0.030	0.10	%
		G = 1000 (Note 2)		0.040	0.10		0.040	0.10	%
	Gain Nonlinearity (Note 5)	V_O = ±10V, G = 1		1	6		1.5	10	ppm
		V_O = ±10V, G = 10 and 100		2	10		3	15	ppm
		V_O = ±10V, G = 1000		15	40		20	60	ppm
		V_O = ±10V, G = 1, R_L = 600		5	12		6	15	ppm
		V_O = ±10V, G = 10 and 100, R_L = 600		6	15		7	20	ppm
		V_O = ±10V, G = 1000, R_L = 600		20	65		25	80	ppm
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	G = 1000, V_S = ±5V to ±15V		15	40		20	60	µV
V_{OSO}	Output Offset Voltage	G = 1, V_S = ±5V to ±15V		40	200		50	300	µV
I_{OS}	Input Offset Current			90	320		100	450	pA
I_B	Input Bias Current			50	350		80	500	pA
e_n	Input Noise Voltage, RTI	0.1Hz to 10Hz, G = 1		2.00			2.00		μV_{P-P}
		0.1Hz to 10Hz, G = 10		0.50			0.50		μV_{P-P}
		0.1Hz to 10Hz, G = 100 and 1000		0.28			0.28		μV_{P-P}
Total RTI Noise = $\sqrt{e_{ni}^2 + (e_{no}/G)^2}$									
e_{ni}	Input Noise Voltage Density, RTI	f_O = 1kHz		7.5	12		7.5	12	$nV/\sqrt{Hz}$
e_{no}	Output Noise Voltage Density, RTI	f_O = 1kHz (Note 3)		67	90		67	90	$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, $R_L = 2k$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)	LT1167AC/LT1167AI MIN	LT1167AC/LT1167AI TYP	LT1167AC/LT1167AI MAX	LT1167C/LT1167I MIN	LT1167C/LT1167I TYP	LT1167C/LT1167I MAX	UNITS
i_n	Input Noise Current	$f_O = 0.1Hz$ to $10Hz$		10			10		pA_{P-P}
	Input Noise Current Density	$f_O = 10Hz$		124			124		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{IN} = \pm 10V$	200	1000		200	1000		GΩ
$C_{IN(DIFF)}$	Differential Input Capacitance	$f_O = 100kHz$		1.6			1.6		pF
$C_{IN(CM)}$	Common Mode Input Capacitance	$f_O = 100kHz$		1.6			1.6		pF
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded							
		$V_S = \pm 2.3V$ to $\pm 5V$	$-V_S + 1.9$		$+V_S - 1.2$	$-V_S + 1.9$		$+V_S - 1.2$	V
		$V_S = \pm 5V$ to $\pm 18V$	$-V_S + 1.9$		$+V_S - 1.4$	$-V_S + 1.9$		$+V_S - 1.4$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = 0V$ to $\pm 10V$							
		G = 1	90	95		85	95		dB
		G = 10	106	115		100	115		dB
		G = 100	120	125		110	125		dB
		G = 1000	126	140		120	140		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.3$ to $\pm 18V$							
		G = 1	105	120		100	120		dB
		G = 10	125	135		120	135		dB
		G = 100	131	140		126	140		dB
		G = 1000	135	150		130	150		dB
I_S	Supply Current	$V_S = \pm 2.3V$ to $\pm 18V$		0.9	1.3		0.9	1.3	mA
V_{OUT}	Output Voltage Swing	$R_L = 10k$							
		$V_S = \pm 2.3V$ to $\pm 5V$	$-V_S + 1.1$		$+V_S - 1.2$	$-V_S + 1.1$		$+V_S - 1.2$	V
		$V_S = \pm 5V$ to $\pm 18V$	$-V_S + 1.2$		$+V_S - 1.3$	$-V_S + 1.2$		$+V_S - 1.3$	V
I_{OUT}	Output Current		20	27		20	27		mA
BW	Bandwidth	G = 1		1000			1000		kHz
		G = 10		800			800		kHz
		G = 100		120			120		kHz
		G = 1000		12			12		kHz
SR	Slew Rate	G = 1, $V_{OUT} = \pm 10V$	0.75	1.2		0.75	1.2		V/µs
	Settling Time to 0.01%	10V Step							
		G = 1 to 100		14			14		µs
		G = 1000		130			130		µs
R_{REFIN}	Reference Input Resistance			20			20		kΩ
I_{REFIN}	Reference Input Current	$V_{REF} = 0V$		50			50		µA
V_{REF}	Reference Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V
A_{VREF}	Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, $R_L = 2k$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)		LT1167AC MIN	LT1167AC TYP	LT1167AC MAX	LT1167C MIN	LT1167C TYP	LT1167C MAX	UNITS
	Gain Error	G = 1	●		0.01	0.03		0.012	0.04	%
		G = 10 (Note 2)	●		0.08	0.30		0.100	0.33	%
		G = 100 (Note 2)	●		0.09	0.30		0.120	0.33	%
		G = 1000 (Note 2)	●		0.14	0.33		0.140	0.35	%
	Gain Nonlinearity	$V_{OUT} = \pm 10V$, G = 1	●		1.5	10		2	15	ppm
		$V_{OUT} = \pm 10V$, G = 10 and 100	●		3	15		4	20	ppm
		$V_{OUT} = \pm 10V$, G = 1000	●		20	60		25	80	ppm
G/T	Gain vs Temperature	G < 1000 (Note 2)	●		20	50		20	50	ppm/°C
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$								
V_{OSI}	Input Offset Voltage	$V_S = \pm 5V$ to $\pm 15V$	●		18	60		23	80	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 6)			3.0			3.0		µV
V_{OSO}	Output Offset Voltage	$V_S = \pm 5V$ to $\pm 15V$	●		60	380		70	500	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 6)			30			30		µV
V_{OSI}/T	Input Offset Drift (RTI)	(Note 3)	●		0.05	0.3		0.06	0.4	µV/°C
V_{OSO}/T	Output Offset Drift	(Note 3)	●		0.7	3		0.8	4	µV/°C
I_{OS}	Input Offset Current		●		100	400		120	550	pA
I_{OS}/T	Input Offset Current Drift		●		0.3			0.4		pA/°C
I_B	Input Bias Current		●		75	450		105	600	pA
I_B/T	Input Bias Current Drift		●		0.4			0.4		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded								
		$V_S = \pm 2.3V$ to $\pm 5V$	●	$-V_S+2.1$		$+V_S-1.3$	$-V_S+2.1$		$+V_S-1.3$	V
		$V_S = \pm 5V$ to $\pm 18V$	●	$-V_S+2.1$		$+V_S-1.4$	$-V_S+2.1$		$+V_S-1.4$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = 0V$ to $\pm 10V$								
		G = 1	●	88	92		83	92		dB
		G = 10	●	100	110		97	110		dB
		G = 100	●	115	120		113	120		dB
		G = 1000	●	117	135		114	135		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.3V$ to $\pm 18V$								
		G = 1	●	103	115		98	115		dB
		G = 10	●	123	130		118	130		dB
		G = 100	●	127	135		124	135		dB
		G = 1000	●	129	145		126	145		dB
I_S	Supply Current	$V_S = \pm 2.3V$ to $\pm 18V$	●		1.0	1.5		1.0	1.5	mA
V_{OUT}	Output Voltage Swing	$R_L = 10k$								
		$V_S = \pm 2.3V$ to $\pm 5V$	●	$-V_S+1.4$		$+V_S-1.3$	$-V_S+1.4$		$+V_S-1.3$	V
		$V_S = \pm 5V$ to $\pm 18V$	●	$-V_S+1.6$		$+V_S-1.5$	$-V_S+1.6$		$+V_S-1.5$	V
I_{OUT}	Output Current		●	16	21		16	21		mA
SR	Slew Rate	G = 1, $V_{OUT} = \pm 10V$	●	0.65	1.1		0.65	1.1		V/µs
V_{REF}	REF Voltage Range	(Note 3)	●	$-V_S+1.6$		$+V_S-1.6$	$-V_S+1.6$		$+V_S-1.6$	V

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, −40°C ≤ T_A ≤ 85°C, R_L = 2k, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS (Note 7)		LT1167AI MIN	LT1167AI TYP	LT1167AI MAX	LT1167I MIN	LT1167I TYP	LT1167I MAX	UNITS
	Gain Error	G = 1	●		0.014	0.04		0.015	0.05	%
		G = 10 (Note 2)	●		0.130	0.40		0.140	0.42	%
		G = 100 (Note 2)	●		0.140	0.40		0.150	0.42	%
		G = 1000 (Note 2)	●		0.160	0.40		0.180	0.45	%
G_N	Gain Nonlinearity (Notes 2, 4)	V_O = ±10V, G = 1	●		2	15		3	20	ppm
		V_O = ±10V, G = 10 and 100	●		5	20		6	30	ppm
		V_O = ±10V, G = 1000	●		26	70		30	100	ppm
G/T	Gain vs Temperature	G < 1000 (Note 2)	●		20	50		20	50	ppm/°C
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$								
V_{OSI}	Input Offset Voltage		●		20	75		25	100	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 3, 6)			3.0			3.0		µV
V_{OSO}	Output Offset Voltage		●		180	500		200	600	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 3, 6)			30			30		µV
V_{OSI}/T	Input Offset Drift (RTI)	(Note 3)	●		0.05	0.3		0.06	0.4	µV/°C
V_{OSO}/T	Output Offset Drift	(Note 3)	●		0.8	5		1	6	µV/°C
I_{OS}	Input Offset Current		●		110	550		120	700	pA
I_{OS}/T	Input Offset Current Drift		●		0.3			0.3		pA/°C
I_B	Input Bias Current		●		180	600		220	800	pA
I_B/T	Input Bias Current Drift		●		0.5			0.6		pA/°C
V_{CM}	Input Voltage Range	V_S = ±2.3V to ±5V	●	$-V_S + 2.1$		$+V_S - 1.3$	$-V_S + 2.1$		$+V_S - 1.3$	V
		V_S = ±5V to ±18V	●	$-V_S + 2.1$		$+V_S - 1.4$	$-V_S + 2.1$		$+V_S - 1.4$	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V								
		G = 1	●	86	90		81	90		dB
		G = 10	●	98	105		95	105		dB
		G = 100	●	114	118		112	118		dB
		G = 1000	●	116	133		112	133		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V								
		G = 1	●	100	112		95	112		dB
		G = 10	●	120	125		115	125		dB
		G = 100	●	125	132		120	132		dB
		G = 1000	●	128	140		125	140		dB
I_S	Supply Current		●		1.1	1.6		1.1	1.6	mA
V_{OUT}	Output Voltage Swing	V_S = ±2.3V to ±5V	●	$-V_S + 1.4$		$+V_S - 1.3$	$-V_S + 1.4$		$+V_S - 1.3$	V
		V_S = ±5V to ±18V	●	$-V_S + 1.6$		$+V_S - 1.5$	$-V_S + 1.6$		$+V_S - 1.5$	V
I_{OUT}	Output Current		●	15	20		15	20		mA
SR	Slew Rate	G = 1, V_{OUT} = ±10V	●	0.55	0.95		0.55	0.95		V/µs
V_{REF}	REF Voltage Range	(Note 3)	●	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V

The ● denotes specifications that apply over the full specified temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be imparied.

Note 2: Does not include the effect of the external gain resistor R_G.

Note 3: This parameter is not 100% tested.

Note 4: The LT1167AC/LT1167C are designed, characterized and expected to meet the industrial temperature limits, but are not tested at –40°C and 85°C. I-grade parts are guaranteed.

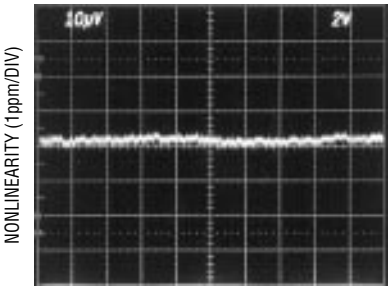
Note 5: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, heat sinking and air flow conditions.

Note 6: Hysteresis in offset voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Offset voltage hysteresis is always measured at 25°C, but the IC is cycled to 85°C I-grade (or 70°C C-grade) or –40°C I-grade (0°C C-grade) before successive measurement. 60% of the parts will pass the typical limit on the data sheet.

Note 7: Typical parameters are defined as the 60% of the yield parameter distribution.

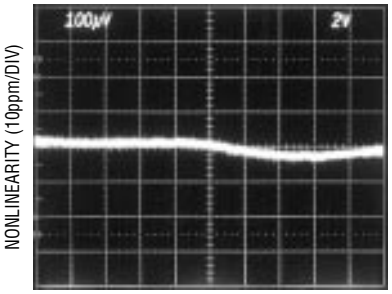
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Nonlinearity, G = 1



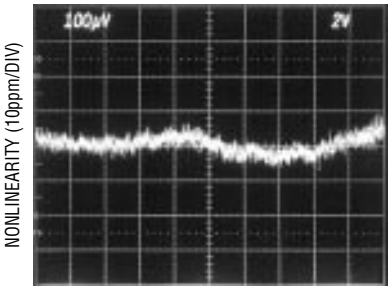
G = 1 OUTPUT VOLTAGE (2V/DIV)
R_L = 2k
V_{OUT} = ±10V

Gain Nonlinearity, G = 10



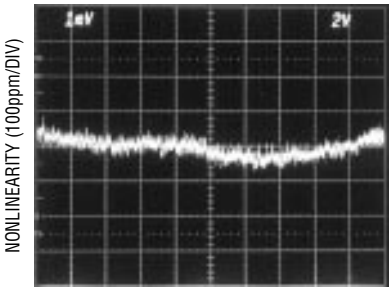
G = 10 OUTPUT VOLTAGE (2V/DIV)
R_L = 2k
V_{OUT} = ±10V

Gain Nonlinearity, G = 100



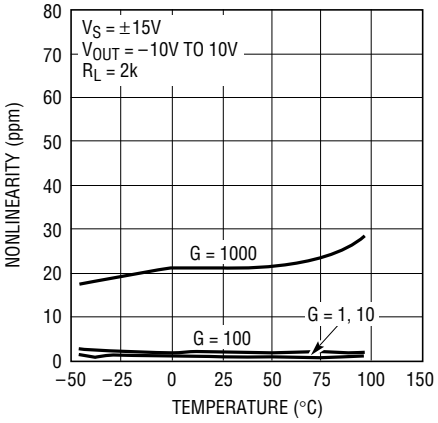
G = 100 OUTPUT VOLTAGE (2V/DIV)
R_L = 2k
V_{OUT} = ±10V

Gain Nonlinearity, G = 1000

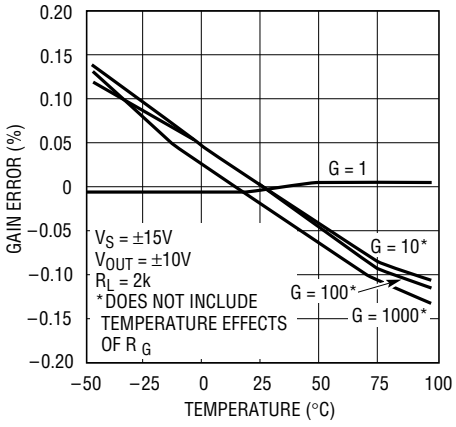


G = 1000 OUTPUT VOLTAGE (2V/DIV)
R_L = 2k
V_{OUT} = ±10V

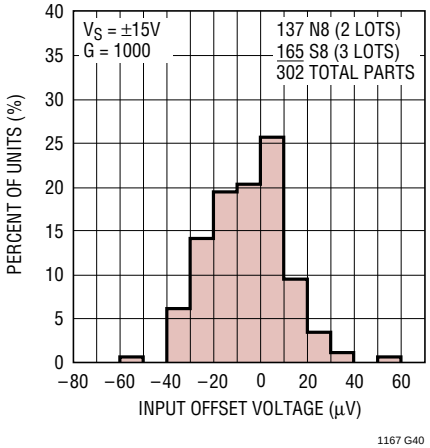
Gain Nonlinearity vs Temperature



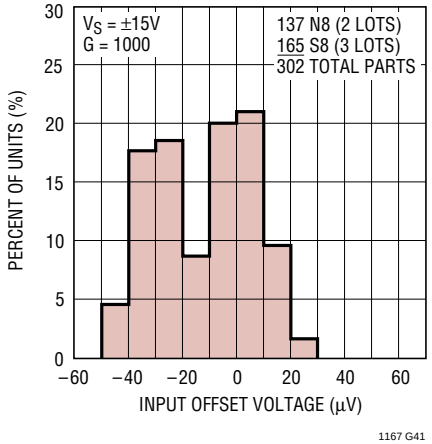
Gain Error vs Temperature



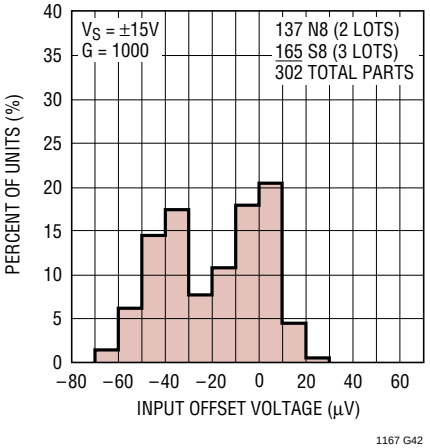
Distribution of Input Offset Voltage, T_A = –40°C



Distribution of Input Offset Voltage, T_A = 25°C

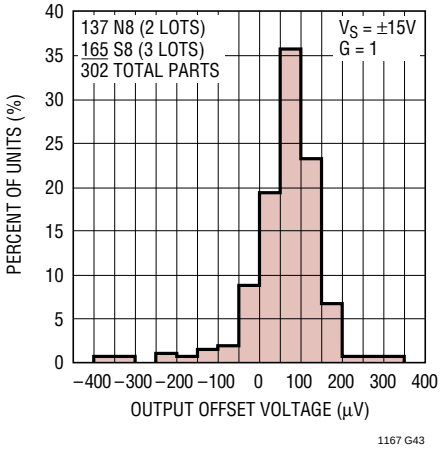


Distribution of Input Offset Voltage, T_A = 85°C

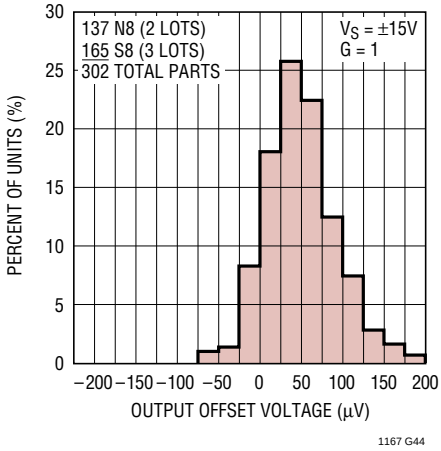


TYPICAL PERFORMANCE CHARACTERISTICS

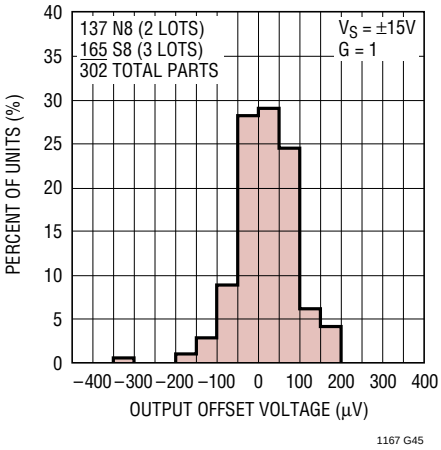
Distribution of Output Offset Voltage, $T_A = -40°C$



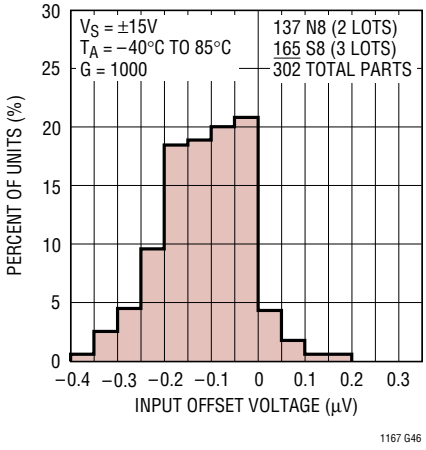
Distribution of Output Offset Voltage, $T_A = 25°C$



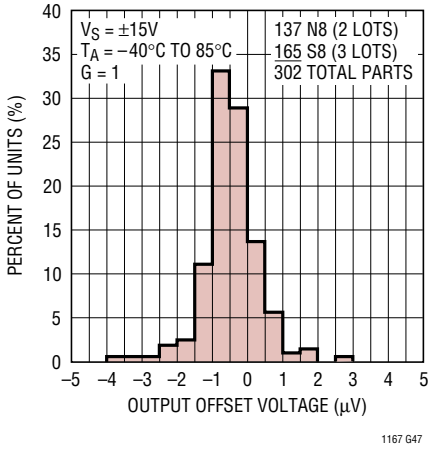
Distribution of Output Offset Voltage, $T_A = 85°C$



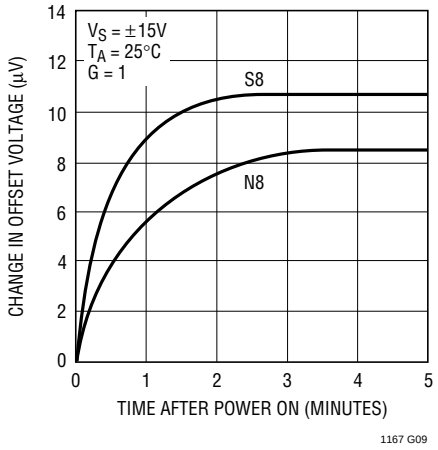
Distribution of Input Offset Voltage Drift



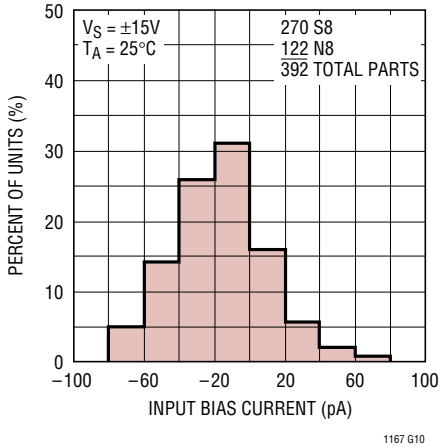
Distribution of Output Offset Voltage Drift



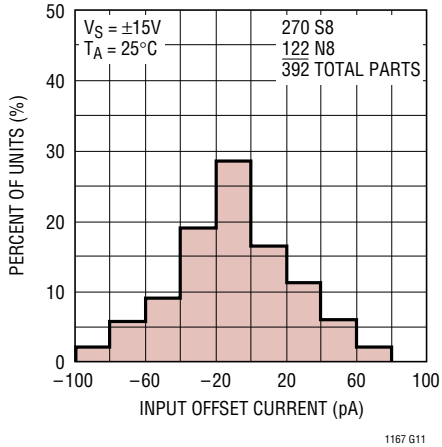
Warm-Up Drift



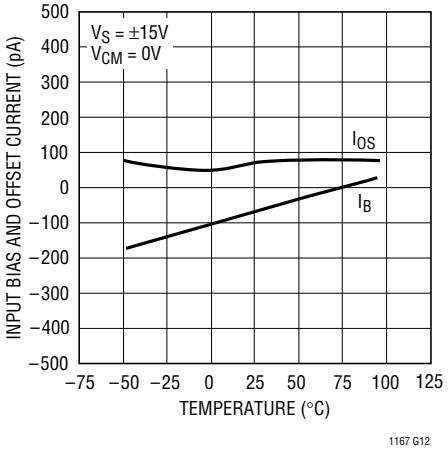
Input Bias Current



Input Offset Current

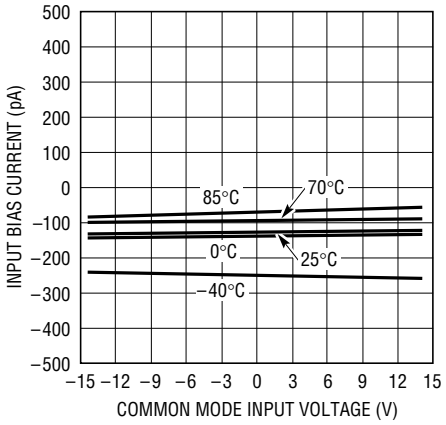


Input Bias and Offset Current vs Temperature

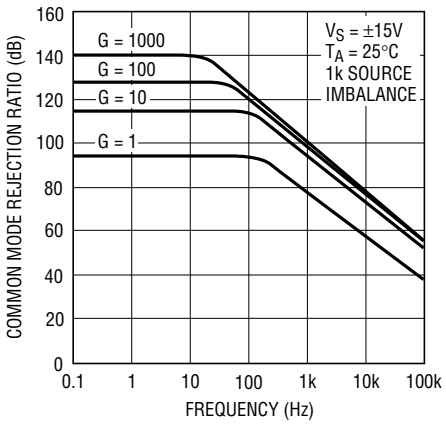


TYPICAL PERFORMANCE CHARACTERISTICS

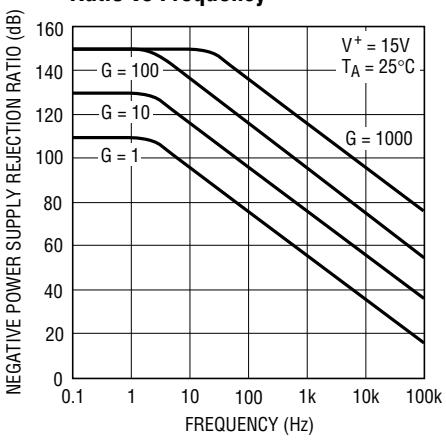
Input Bias Current vs Common Mode Input Voltage



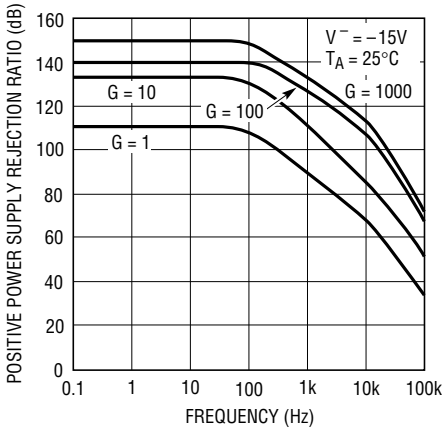
Common Mode Rejection Ratio vs Frequency



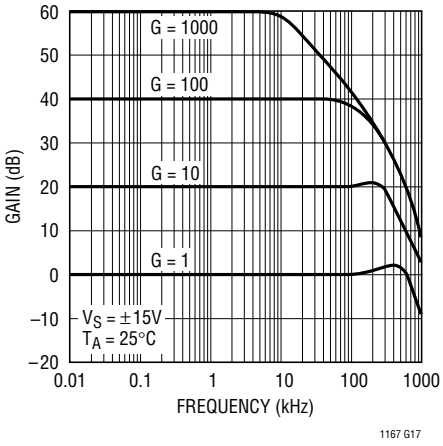
Negative Power Supply Rejection Ratio vs Frequency



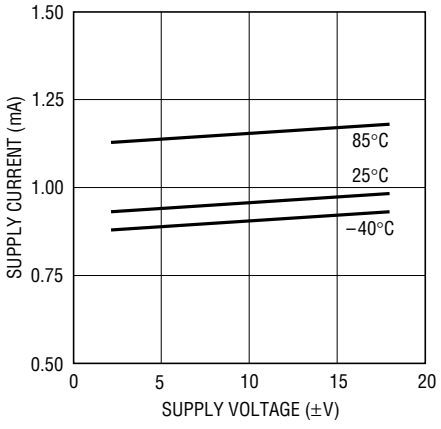
Positive Power Supply Rejection Ratio vs Frequency



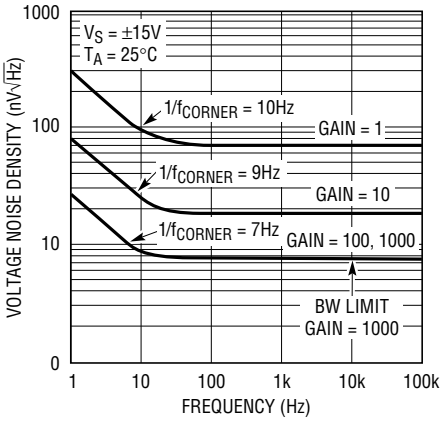
Gain vs Frequency



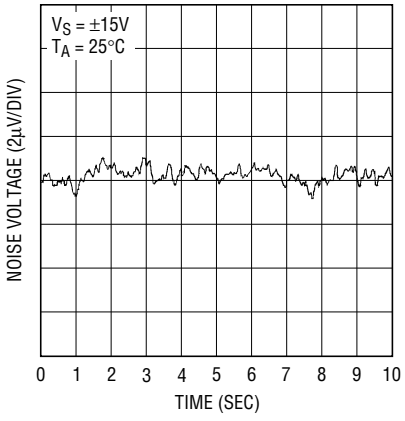
Supply Current vs Supply Voltage



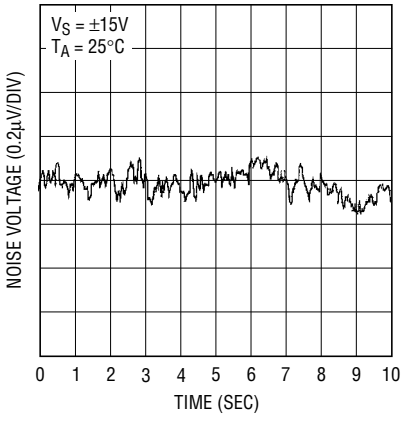
Voltage Noise Density vs Frequency



0.1Hz to 10Hz Noise Voltage, G = 1

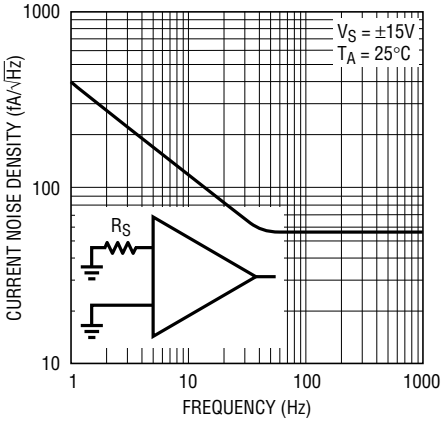


0.1Hz to 10Hz Noise Voltage, RTI G = 1000

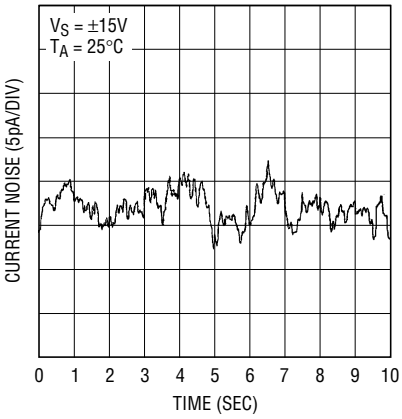


TYPICAL PERFORMANCE CHARACTERISTICS

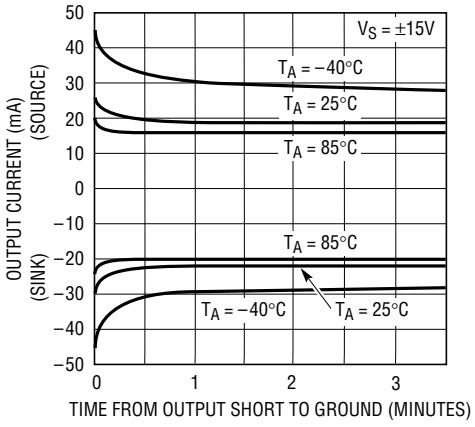
Current Noise Density vs Frequency



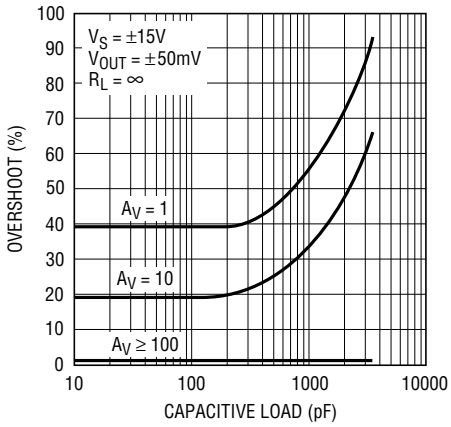
0.1Hz to 10Hz Current Noise



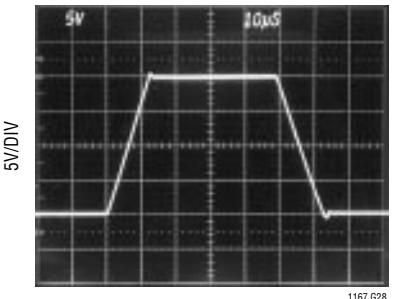
Short-Circuit Current vs Time



Overshoot vs Capacitive Load

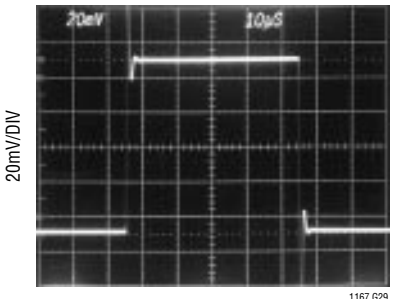


Large-Signal Transient Response



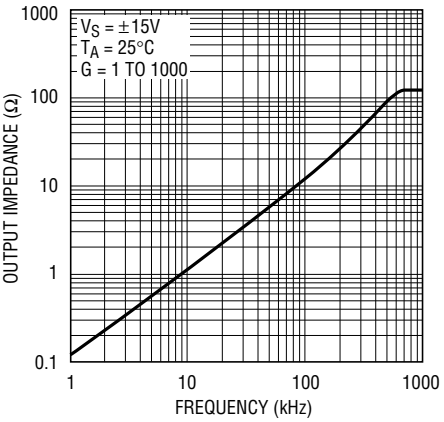
G = 1 10µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

Small-Signal Transient Response

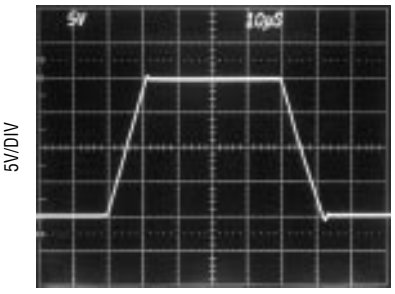


G = 1 10µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

Output Impedance vs Frequency

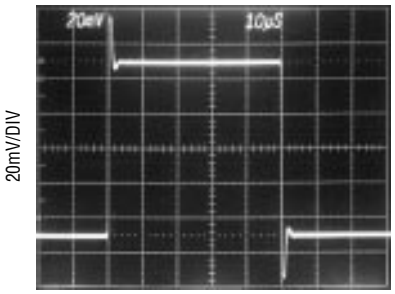


Large-Signal Transient Response



G = 10 10µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

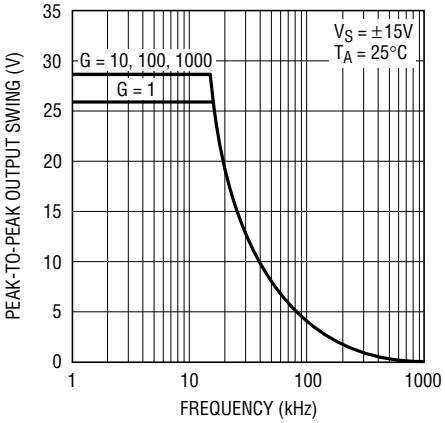
Small-Signal Transient Response



G = 10 10µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

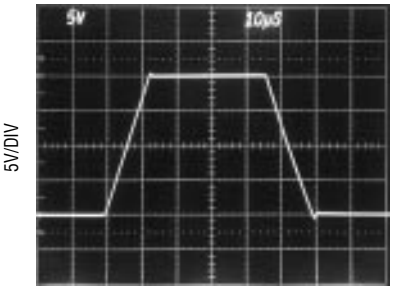
TYPICAL PERFORMANCE CHARACTERISTICS

Undistorted Output Swing vs Frequency



1167 G27

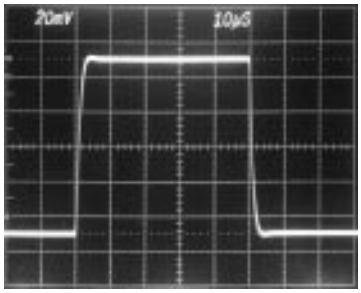
Large-Signal Transient Response



1167 G34

G = 100
V_S = ±15V
R_L = 2k
C_L = 60pF
10µs/DIV

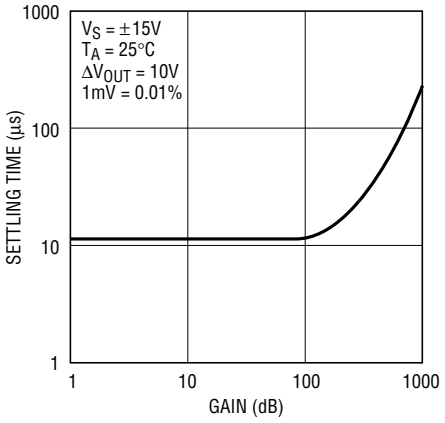
Small-Segment Transient Response



1167 G35

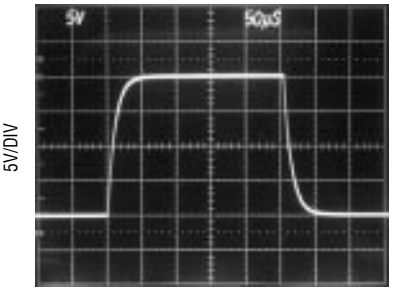
G = 100
V_S = ±15V
R_L = 2k
C_L = 60pF
10µs/DIV

Settling Time vs Gain



1167 G30

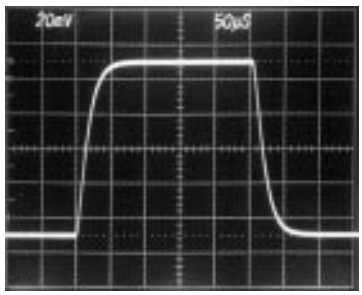
Large-Signal Transient Response



1167 G37

G = 1000
V_S = ±15V
R_L = 2k
C_L = 60pF
50µs/DIV

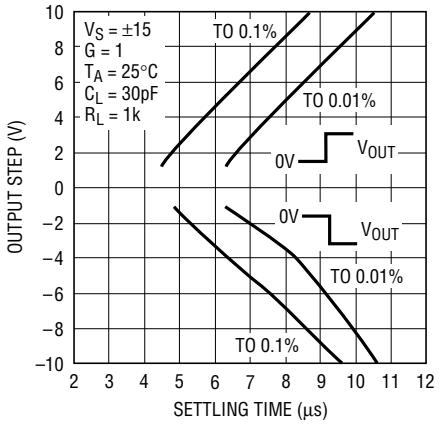
Small-Signal Transient Response



1167 G38

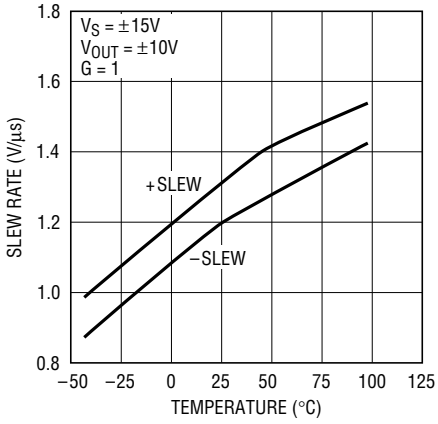
G = 1000
V_S = ±15V
R_L = 2k
C_L = 60pF
50µs/DIV

Settling Time vs Step Size



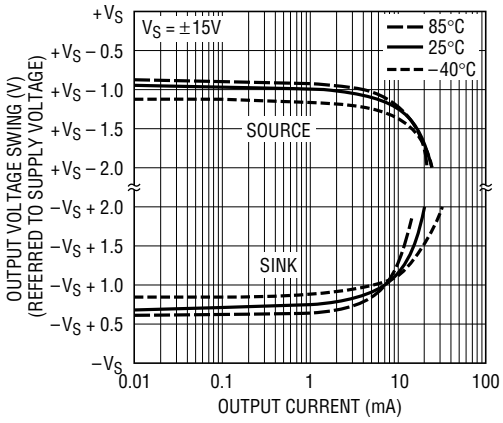
1167 G33

Slew Rate vs Temperature



1167 G36

Output Voltage Swing vs Load Current



1167 G39

BLOCK DIAGRAM

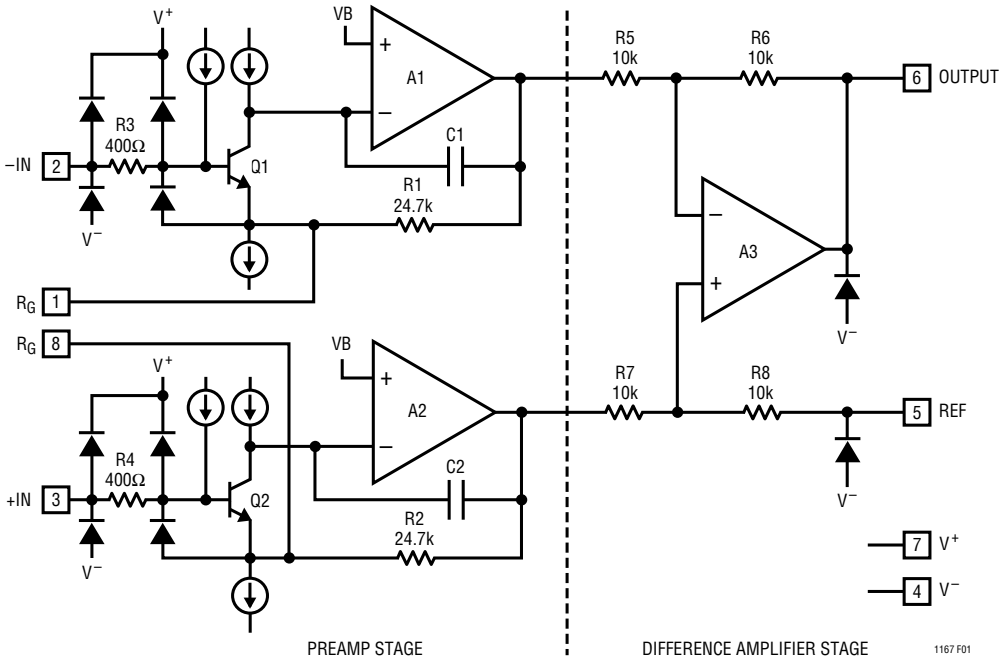


Figure 1. Block Diagram

THEORY OF OPERATION

The LT1167 is a modified version of the three op amp instrumentation amplifier. Laser trimming and monolithic construction allow tight matching and tracking of circuit parameters over the specified temperature range. Refer to the block diagram (Figure 1) to understand the following circuit description. The collector currents in Q1 and Q2 are trimmed to minimize offset voltage drift, thus assuring a high level of performance. R1 and R2 are trimmed to an absolute value of 24.7k to assure that the gain can be set accurately (0.05% at G = 100) with only one external resistor R_G. The value of R_G in parallel with R1 (R2) determines the transconductance of the preamp stage. As R_G is reduced for larger programmed gains, the transconductance of the input preamp stage increases to that of the input transistors Q1 and Q2. This increases the open-loop gain when the programmed gain is increased, reducing the input referred gain related errors and noise. The input voltage noise at gains greater than 50 is determined only by Q1 and Q2. At lower gains the noise of the difference amplifier and preamp gain setting resistors increase the noise. The gain bandwidth product is determined by C1, C2 and the preamp transconductance which increases with programmed gain. Therefore, the bandwidth does not drop proportional to gain.

The input transistors Q1 and Q2 offer excellent matching, which is inherent in NPN bipolar transistors, as well as picoampere input bias current due to superbeta processing. The collector currents in Q1 and Q2 are held constant due to the feedback through the Q1-A1-R1 loop and Q2-A2-R2 loop which in turn impresses the differential input voltage across the external gain set resistor R_G. Since the current that flows through R_G also flows through R1 and R2, the ratios provide a gained-up differential voltage, $G = (R1 + R2)/R_G$, to the unity-gain difference amplifier A3. The common mode voltage is removed by A3, resulting in a single-ended output voltage referenced to the voltage on the REF pin. The resulting gain equation is:

$$V_{OUT} - V_{REF} = G(V_{IN}^{+} - V_{IN}^{-})$$

where:

$$G = (49.4k\Omega/R_G) + 1$$

solving for the gain set resistor gives:

$$R_G = 49.4k\Omega/(G - 1)$$

THEORY OF OPERATION

Input and Output Offset Voltage

The offset voltage of the LT1167 has two components: the output offset and the input offset. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain (G) and adding it to the input offset. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI)
= input offset + (output offset/G)

Total output offset voltage (RTO)
= (input offset • G) + output offset

Reference Terminal

The reference terminal is one end of one of the four 10k resistors around the difference amplifier. The output voltage of the LT1167 (Pin 6) is referenced to the voltage on the reference terminal (Pin 5). Resistance in series with the REF pin must be minimized for best common mode rejection. For example, a 2Ω resistance from the REF pin to ground will not only increase the gain error by 0.02% but will lower the CMRR to 80dB.

Single Supply Operation

For single supply operation, the REF pin can be at the same potential as the negative supply (Pin 4) provided the output of the instrumentation amplifier remains inside the specified operating range and that one of the inputs is at least 2.5V above ground. The barometer application on the front page of this data sheet is an example that satisfies these conditions. The resistance R_b from the bridge transducer to ground sets the operating current for the bridge and also has the effect of raising the input common mode voltage. The output of the LT1167 is always inside the specified range since the barometric pressure rarely goes low enough to cause the output to rail (30.00 inches of Hg corresponds to 3.000V). For applications that require the output to swing at or below the REF potential, the voltage on the REF pin can be level shifted. An op amp is used to buffer the voltage on the REF pin since a parasitic series resistance will degrade the CMRR. The application in the back of this data sheet, Four Digit Pressure Sensor, is an example.

Output Offset Trimming

The LT1167 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset needs to be adjusted, the circuit in Figure 2 is an example of an optional offset adjust circuit. The op amp buffer provides a low impedance to the REF pin where resistance must be kept to minimum for best CMRR and lowest gain error.

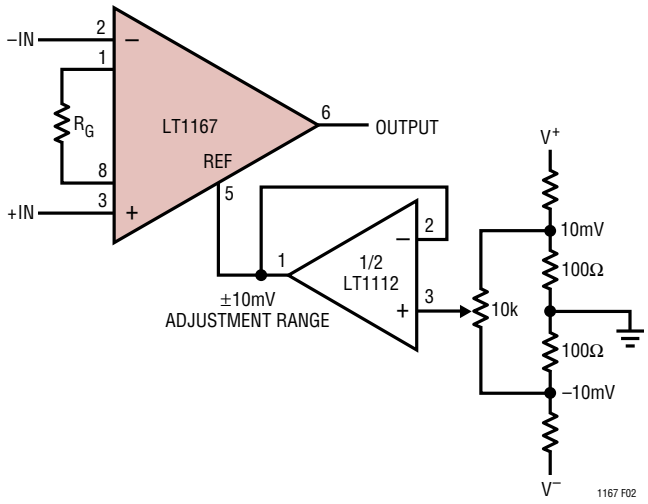


Figure 2. Optional Trimming of Output Offset Voltage

Input Bias Current Return Path

The low input bias current of the LT1167 (350pA) and the high input impedance (200GΩ) allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path the inputs will float to either rail and exceed the input common mode range of the LT1167, resulting in a saturated input stage. Figure 3 shows three examples of an input bias current path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both common mode rejection and DC offset. The need for input resistors is eliminated if a center tap is present as shown in the third example.

THEORY OF OPERATION

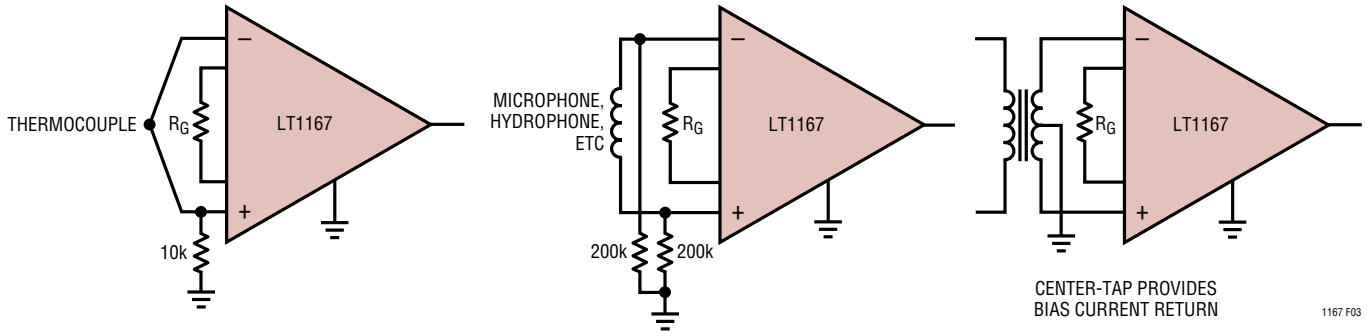


Figure 3. Providing an Input Common Mode Current Path

APPLICATIONS INFORMATION

The LT1167 is a low power precision instrumentation amplifier that requires only one external resistor to accurately set the gain anywhere from 1 to 1000. The output can handle capacitive loads up to 1000pF in any gain configuration and the inputs are protected against ESD strikes up to 13kV (human body).

Input Protection

The LT1167 can safely handle up to ±20mA of input current in an overload condition. Adding an external 5k input resistor in series with each input allows DC input fault voltages up to ±100V and improves the ESD immunity to 8kV (contact) and 15kV (air discharge), which is the IEC 1000-4-2 level 4 specification. If lower value input resistors are needed, a clamp diode from the positive supply to each input will maintain the IEC 1000-4-2 specification to level 4 for both air and contact discharge.

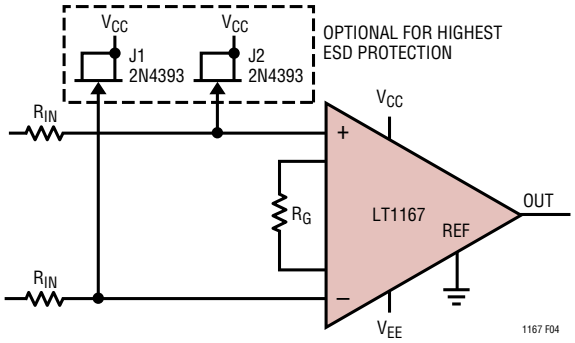


Figure 4. Input Protection

A 2N4393 drain/source to gate is a good low leakage diode for use with 1k resistors, see Figure 4. The input resistors should be carbon and not metal film or carbon film.

RFI Reduction

In many industrial and data acquisition applications, instrumentation amplifiers are used to accurately amplify small signals in the presence of large common mode voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry, using shielded or unshielded twisted-pair cabling, the cabling may act as antennae, conveying very high frequency interference directly into the input stage of the LT1167.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing an unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

APPLICATIONS INFORMATION

To significantly reduce the effect of these out-of-band signals on the input offset voltage of instrumentation amplifiers, simple lowpass filters can be used at the inputs. This filter should be located very close to the input pins of the circuit. An effective filter configuration is illustrated in Figure 5, where three capacitors have been added to the inputs of the LT1167. Capacitors C_{XCM1} and C_{XCM2} form lowpass filters with the external series resistors $R_{S1, 2}$ to any out-of-band signal appearing on each of the input traces. Capacitor C_{XD} forms a filter to reduce any unwanted signal that would appear across the input traces. An added benefit to using C_{XD} is that the circuit's AC common mode rejection is not degraded due to common mode capacitive imbalance. The differential mode and common mode time constants associated with the capacitors are:

$$t_{DM(LPF)} = (2)(R_S)(C_{XD})$$

$$t_{CM(LPF)} = (R_{S1, 2})(C_{XCM1, 2})$$

Setting the time constants requires a knowledge of the frequency, or frequencies of the interference. Once this frequency is known, the common mode time constants can be set followed by the differential mode time constant. To avoid any possibility of inadvertently affecting the signal to be processed, set the common mode time constant an order of magnitude (or more) larger than the differential mode time constant. To avoid any possibility of common mode to differential mode signal conversion, match the common mode time constants to 1% or better. If the sensor is an RTD or a resistive strain gauge, then the series resistors $R_{S1, 2}$ can be omitted, if the sensor is in proximity to the instrumentation amplifier.

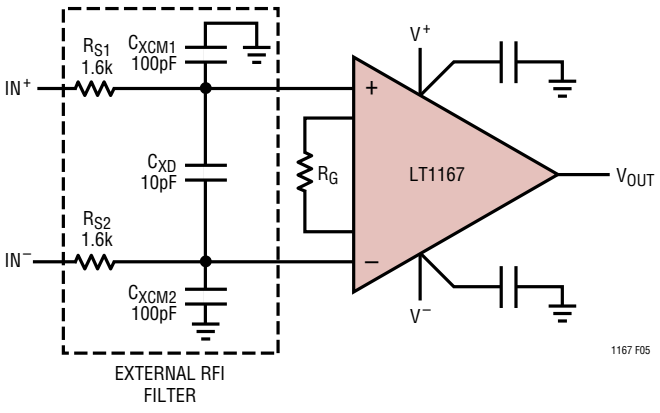


Figure 5. Adding a Simple RC Filter at the Inputs to an Instrumentation Amplifier is Effective in Reducing Rectification of High Frequency Out-of-Band Signals

"Roll Your Own"—Discrete vs Monolithic LT1167 Error Budget Analysis

The LT1167 offers performance superior to that of "roll your own" three op amp discrete designs. A typical application that amplifies and buffers a bridge transducer's differential output is shown in Figure 6. The amplifier, with its gain set to 100, amplifies a differential, full-scale output voltage of 20mV over the industrial range. To make the comparison challenging, the low cost version of the LT1167 will be compared to a discrete instrumentation amp made with the A grade of one of the best precision quad op amps, the LT1114A. The LT1167C outperforms the discrete amplifier that has lower V_{OS}, lower I_B and comparable V_{OS} drift. The error budget comparison in Table 1 shows how various errors are calculated and how each error affects the total error budget. The table shows the greatest differences between the discrete solution and the LT1167 are input offset voltage and CMRR. Note that for the discrete solution, the noise voltage specification is multiplied by $\sqrt{2}$ which is the RMS sum of the uncorelated noise of the two input amplifiers. Each of the amplifier errors is referenced to a full-scale bridge differential voltage of 20mV. The common mode range of the bridge is 5V. The LT1114 data sheet provides offset voltage, offset voltage drift and offset current specifications for the matched op amp pairs used in the error-budget table. Even with an excellent matching op amp like the LT1114, the discrete solution's total error is significantly higher than the LT1167's total error. The LT1167 has additional advantages over the discrete design, including lower component cost and smaller size.

APPLICATIONS INFORMATION

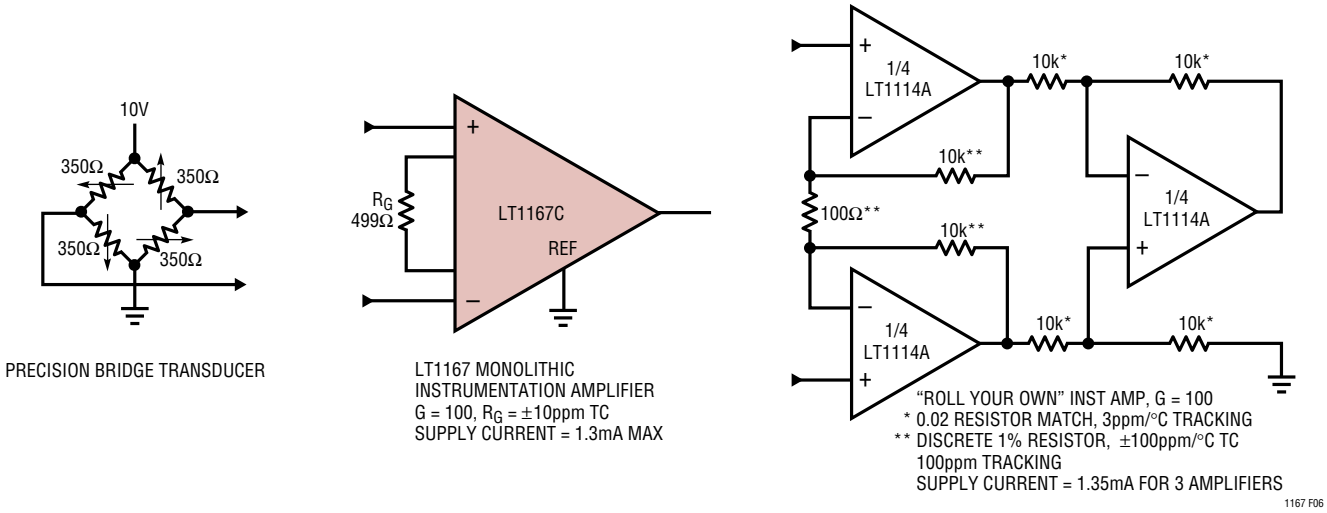


Figure 6. "Roll Your Own" vs LT1167

Table 1. "Roll Your Own" vs LT1167 Error Budget

ERROR SOURCE	LT1167C CIRCUIT CALCULATION	"ROLL YOUR OWN"' CIRCUIT CALCULATION	ERROR, ppm OF FULL SCALE	
			LT1167C	"ROLL YOUR OWN"
Absolute Accuracy at T_A = 25°C				
Input Offset Voltage, µV	60µV/20mV	100µV/20mV	3000	5000
Output Offset Voltage, µV	(300µV/100)/20mV	[(60µV)(2)/100]/20mV	150	60
Input Offset Current, nA	[(450pA)(350/2)Ω]/20mV	[(450pA)(350Ω)/2]/20mV	4	4
CMR, dB	110dB→[(3.16ppm)(5V)]/20mV	[(0.02% Match)(5V)]/20mV	790	500
		Total Absolute Error	**3944**	**5564**
Drift to 85°C				
Gain Drift, ppm/°C	(50ppm + 10ppm)(60°C)	(100ppm/°C Track)(60°C)	3600	6000
Input Offset Voltage Drift, µV/°C	[(0.4µV/°C)(60°C)]/20mV	[(1.6µV/°C)(60°C)]/20mV	1200	4800
Output Offset Voltage Drift, µV/°C	[6µV/°C)(60°C)]/100/20mV	[(1.1µV/°C)(2)(60°C)]/100/20mV	180	66
		Total Drift Error	**4980**	**10866**
Resolution				
Gain Nonlinearity, ppm of Full Scale	15ppm	10ppm	15	10
Typ 0.1Hz to 10Hz Voltage Noise, μV_{P-P}	$0.28\mu V_{P-P}$/20mV	$(0.3\mu V_{P-P})(\sqrt{2})$/20mV	14	21
		Total Resolution Error	**29**	**31**
		Grand Total Error	**8953**	**16461**

G = 100, V_S = ±15V
All errors are min/max and referred to input.

Current Source

Figure 7 shows a simple, accurate, low power programmable current source. The differential voltage across Pins 2 and 3 is mirrored across R_G. The voltage across R_G is amplified and applied across R_X, defining the output current. The 50µA bias current flowing from Pin 5 is buffered by the LT1464 JFET operational amplifier. This has the effect of improving the resolution of the current source to 3pA, which is the maximum I_B of the LT1464A. Replacing R_G with a programmable resistor greatly increases the range of available output currents.

APPLICATIONS INFORMATION

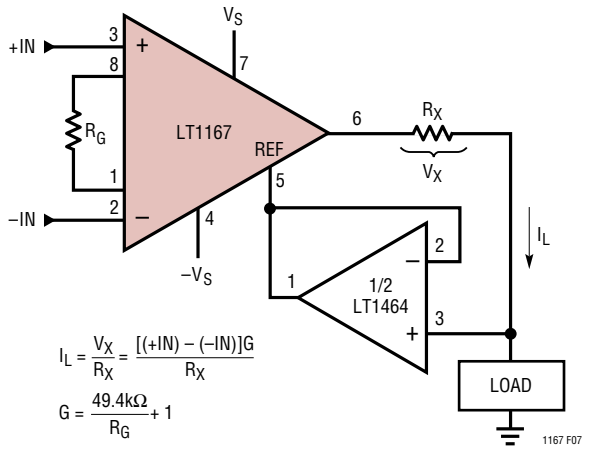


Figure 7. Precision Voltage-to-Current Converter

Nerve Impulse Amplifier

The LT1167's low current noise makes it ideal for high source impedance EMG monitors. Demonstrating the LT1167's ability to amplify low level signals, the circuit in Figure 8 takes advantage of the amplifier's high gain and low noise operation. This circuit amplifies the low level nerve impulse signals received from a patient at Pins 2 and 3. R_G and the parallel combination of R3 and R4 set a gain of ten. The potential on LT1112's Pin 1 creates a ground for the common mode signal. C1 was chosen to maintain the stability of the patient ground. The LT1167's high CMRR ensures that the desired differential signal is amplified and unwanted common mode signals are attenuated. Since the DC portion of the signal is not important, R6 and C2 make up a 0.3Hz highpass filter. The AC signal at LT1112's Pin 5 is amplified by a gain of 101 set by (R7/R8) +1. The parallel combination of C3 and R7 form a lowpass filter that decreases this gain at frequencies above 1kHz. The ability to operate at ±3V on 0.9mA of supply current makes the LT1167 ideal for battery-powered applications. Total supply current for this application is 1.7mA. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

Low I_B Favors High Impedance Bridges, Lowers Dissipation

The LT1167's low supply current, low supply voltage operation and low input bias currents optimize it for battery-powered applications. Low overall power dissipation necessitates using higher impedance bridges. The single supply pressure monitor application (Figure 9) shows the LT1167 connected to the differential output of a 3.5k bridge. The bridge's impedance is almost an order of magnitude higher than that of the bridge used in the error-budget table. The picoampere input bias currents keep the error caused by offset current to a negligible level. The LT1112 level shifts the LT1167's reference pin and the ADC's analog ground pins above ground. The LT1167's and LT1112's combined power dissipation is still less than the bridge's. This circuit's total supply current is just 2.8mA.

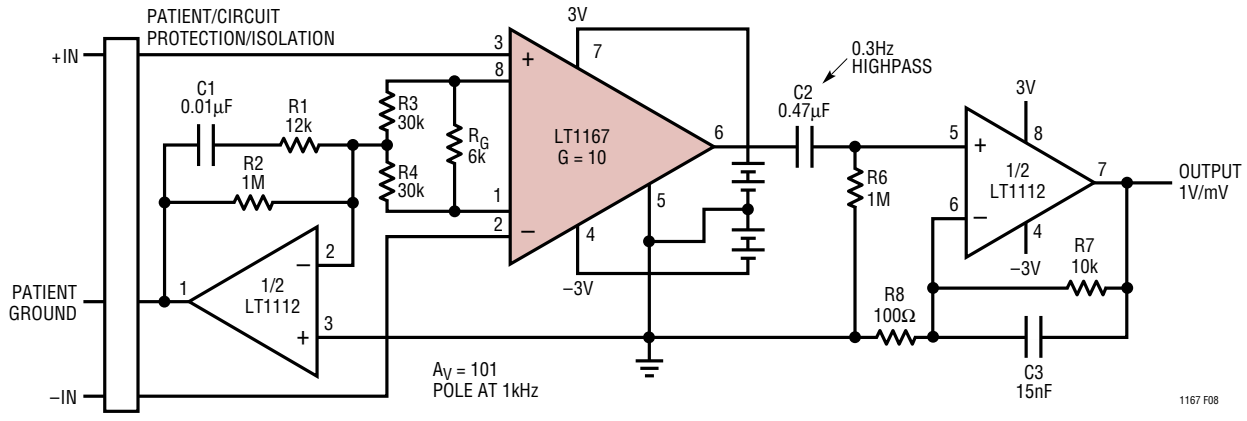


Figure 8. Nerve Impulse Amplifier

APPLICATIONS INFORMATION

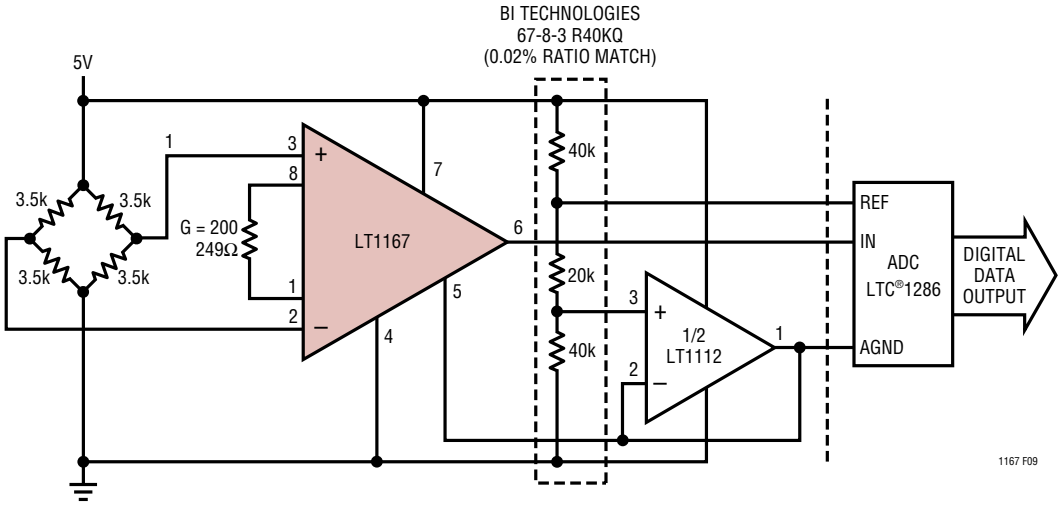
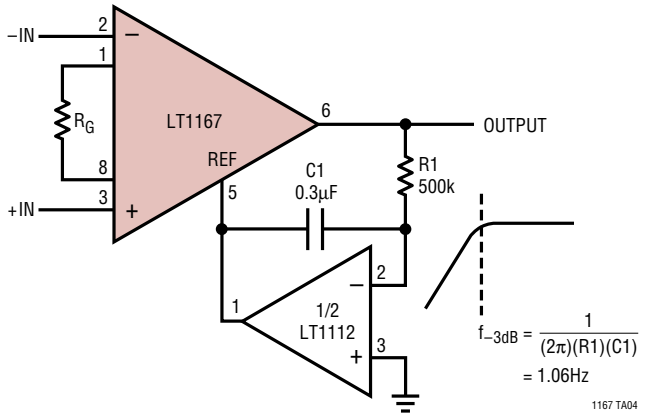


Figure 9. Single Supply Pressure Monitor

TYPICAL APPLICATION

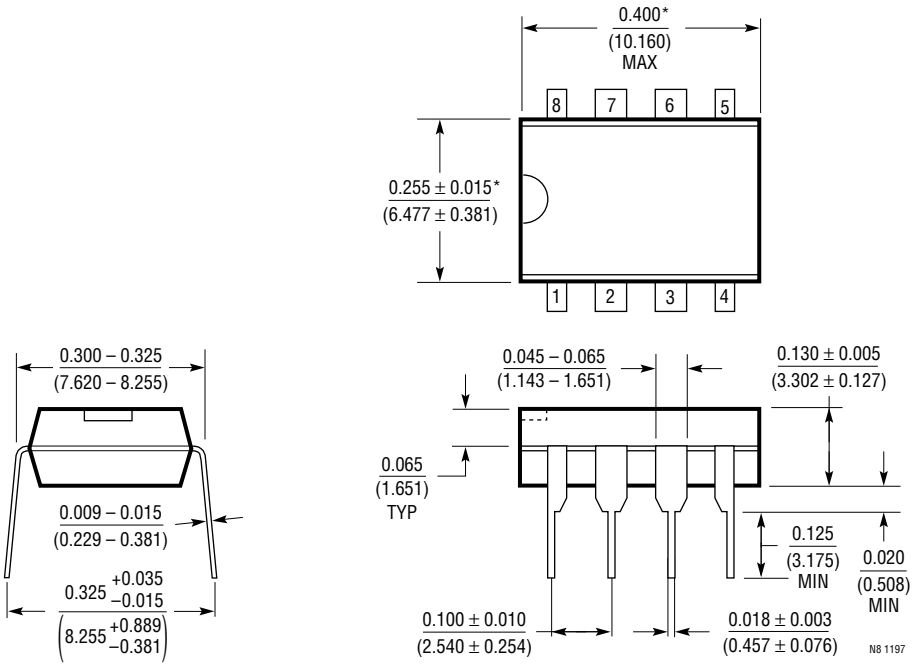
AC Coupled Instrumentation Amplifier



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

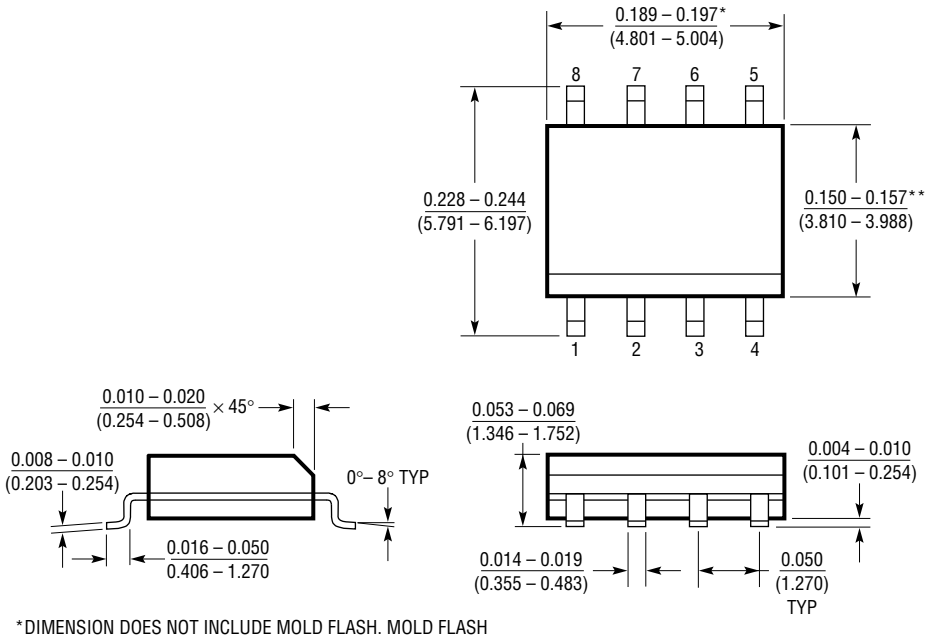


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



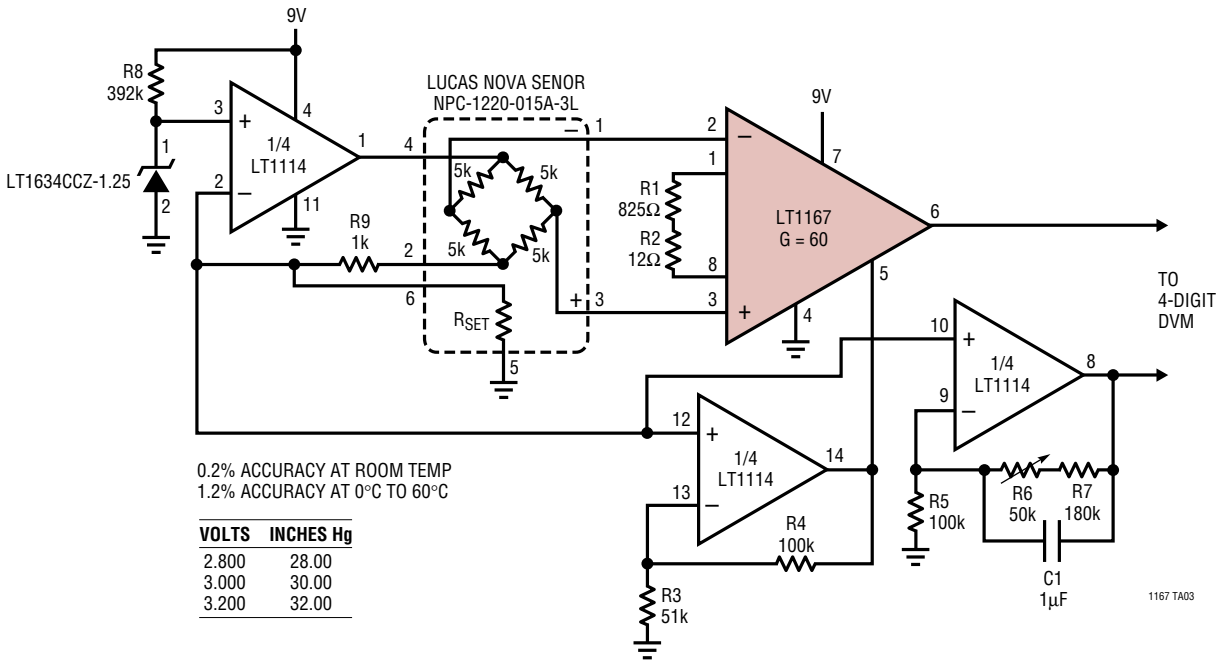
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

TYPICAL APPLICATION

4-Digit Pressure Sensor



0.2% ACCURACY AT ROOM TEMP
1.2% ACCURACY AT 0°C TO 60°C

VOLTS	INCHES Hg
2.800	28.00
3.000	30.00
3.200	32.00

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1100	Precision Chopper-Stabilized Instrumentation Amplifier	Best DC Accuracy
LT1101	Precision, Micropower, Single Supply Instrumentation Amplifier	Fixed Gain of 10 or 100, I_S < 105µA
LT1102	High Speed, JFET Instrumentation Amplifier	Fixed Gain of 10 or 100, 30V/µs Slew Rate
LTC®1418	14-Bit, Low Power, 200ksps ADC with Serial and Parallel I/O	Single Supply 5V or ±5V Operation, ±1.5LSB INL and ±1LSB DNL Max
LT1460	Precision Series Reference	Micropower; 2.5V, 5V, 10V Versions; High Precision
LT1468	16-Bit Accurate Op Amp, Low Noise Fast Settling	16-Bit Accuracy at Low and High Frequencies, 90MHz GBW, 22V/µs, 900ns Settling
LTC1562	Active RC Filter	Lowpass, Bandpass, Highpass Responses; Low Noise, Low Distortion, Four 2nd Order Filter Sections
LTC1605	16-Bit, 100ksps, Sampling ADC	Single 5V Supply, Bipolar Input Range: ±10V, Power Dissipation: 55mW Typ

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