Dual and Quad 45MHz, 400V/µs Op Amps

FEATURES

- 45MHz Gain-Bandwidth
- 400V/µs Slew Rate
- Unity-Gain Stable
- 7V/mV DC Gain, R_L = 500Ω
- 3mV Maximum Input Offset Voltage
- ±12V Minimum Output Swing into 500Ω
- Wide Supply Range: ±2.5V to ±15V
- 7mA Supply Current per Amplifier
- 90ns Settling Time to 0.1%, 10V Step
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

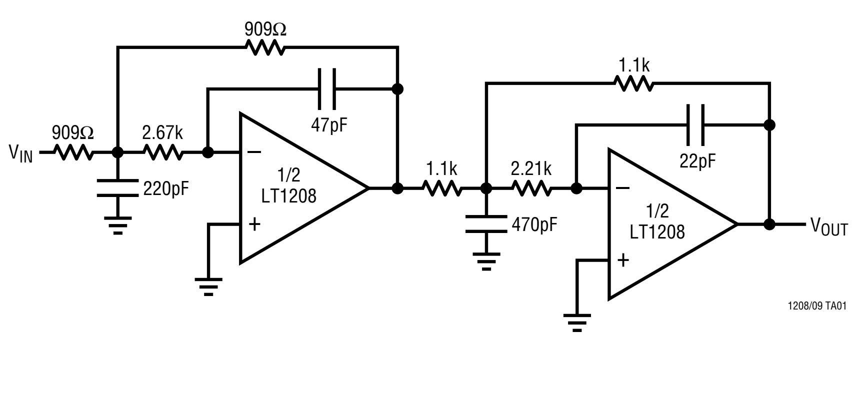
DESCRIPTION

The LT1208/LT1209 are dual and quad very high speed operational amplifiers with excellent DC performance. The LT1208/LT1209 feature reduced input offset voltage and higher DC gain than devices with comparable bandwidth and slew rate. Each amplifier is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. Each output is capable of driving a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifiers are also capable of driving large capacitive loads which make them useful in buffer or cable driver applications.

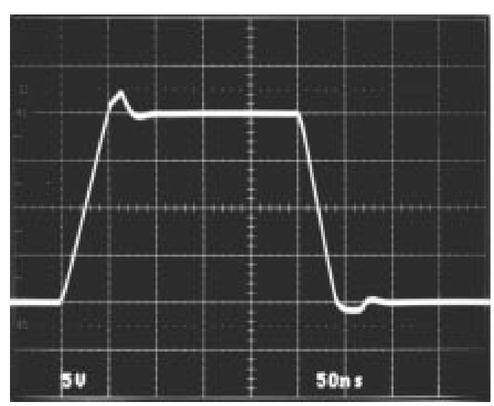
The LT1208/LT1209 are members of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

TYPICAL APPLICATION

1MHz, 4th Order Butterworth Filter



Inverter Pulse Response



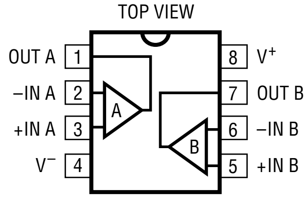
1208/09 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1208C/LT1209C .... −40°C to 85°C
Maximum Junction Temperature
Plastic Package .... 150°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



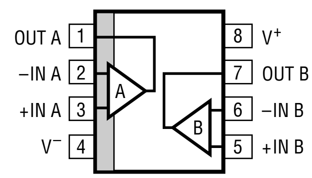
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1208CN8

CONTACT FACTORY FOR MILITARY/883B PARTS

TOP VIEW

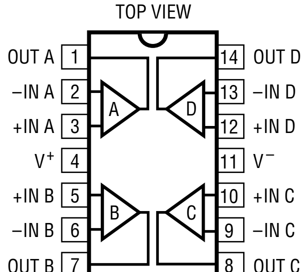


S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1208CS8
S8 PART MARKING
1208

TOP VIEW

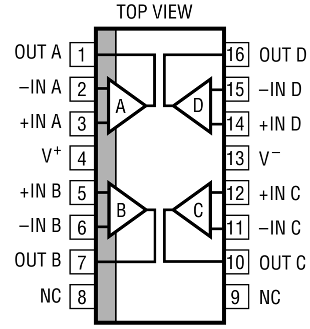


N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER
LT1209CN

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1209CS

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 1k$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 5V$ (Note 2)			0.5	3.0	mV
		0°C to 70°C	●			4.0	mV
		$V_S = \pm 15V$ (Note 2)			1.0	5.0	mV
		0°C to 70°C	●			6.0	mV
	Input V_{OS} Drift				25		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 5V$ and $V_S = \pm 15V$			100	400	nA
		0°C to 70°C	●			600	nA
I_B	Input Bias Current	$V_S = \pm 5V$ and $V_S = \pm 15V$			4	8	µA
		0°C to 70°C	●			9	µA
e_n	Input Noise Voltage	f = 10kHz			22		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz			1.1		$pA/\sqrt{Hz}$

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $R_L = 1k$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	$V_{CM} = \pm12V$ Differential		20	40 250		MΩ kΩ
C_{IN}	Input Capacitance				2		pF
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$; $V_S = \pm5V$, $V_{CM} = \pm2.5V$, 0°C to 70°C	 ●	86 83	98		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$ 0°C to 70°C	 ●	76 75	84		dB dB
	Input Voltage Range	$V_S = \pm15V$ $V_S = \pm5V$		±12 ±2.5	±13 ±3		V V
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 500\Omega$ 0°C to 70°C	 ●	3.3 2.5	7		V/mV V/mV
		$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 500\Omega$ 0°C to 70°C	 ●	2.5 2.0	7		V/mV V/mV
		$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 150\Omega$			3		V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 500\Omega$, 0°C to 70°C $V_S = \pm5V$, $R_L = 150\Omega$, 0°C to 70°C	● ●	12.0 3.0	13.3 3.3		±V ±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$, 0°C to 70°C $V_S = \pm5V$, $V_{OUT} = \pm3V$, 0°C to 70°C	● ●	24 20	40 40		mA mA
SR	Slew Rate	$V_S = \pm15V$, $A_{VCL} = -2$, (Note 3) 0°C to 70°C	 ●	250 200	400		V/µs V/µs
		$V_S = \pm5V$, $A_{VCL} = -2$, (Note 3) 0°C to 70°C	 ●	150 130	250		V/µs V/µs
	Full Power Bandwidth	10V Peak, (Note 4)			6.4		MHz
GBW	Gain-Bandwidth	$V_S = \pm15V$, f = 1MHz $V_S = \pm5V$, f = 1MHz			45 34		MHz MHz
t_r, t_f	Rise Time, Fall Time	$V_S = \pm15V$, $A_{VCL} = 1$, 10% to 90%, 0.1V $V_S = \pm5V$, $A_{VCL} = 1$, 10% to 90%, 0.1V			5 7		ns ns
	Overshoot	$V_S = \pm15V$, $A_{VCL} = 1$, 0.1V $V_S = \pm5V$, $A_{VCL} = 1$, 0.1V			30 20		% %
	Propagation Delay	$V_S = \pm15V$, 50% V_{IN} to 50%V_{OUT} $V_S = \pm5V$, 50% V_{IN} to 50%V_{OUT}			5 7		ns ns
t_s	Settling Time	$V_S = \pm15V$, 10V Step, $V_S = \pm5V$, 5V Step, 0.1%			90		ns
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$ f = 3.58MHz, $R_L = 1k$			1.30 0.09		% %
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$ f = 3.58MHz, $R_L = 1k$			1.8 0.1		Deg Deg
R_O	Output Resistance	$A_{VCL} = 1$, f = 1MHz			2.5		Ω
	Crosstalk	$V_{OUT} = \pm10V$, $R_L = 500\Omega$			–100	–94	dB
I_S	Supply Current	Each Amplifier, $V_S = \pm5V$ and $V_S = \pm15V$ 0°C to 70°C	 ●		7	9 10.5	mA mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

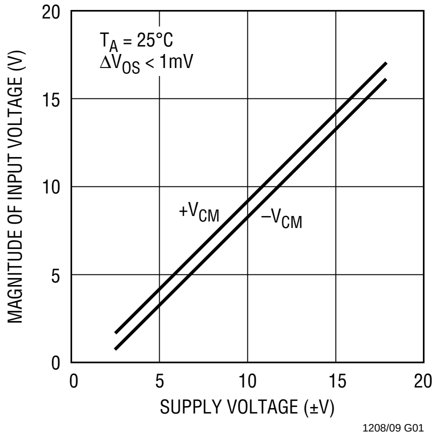
Note 2: Input offset voltage is tested with automated test equipment and is exclusive of warm-up drift.

Note 3: Slew rate is measured in a gain of –2. For ±15V supplies measure between ±10V on the output with ±6V on the input. For ±5V supplies measure between ±2V on the output with ±1.75V on the input.

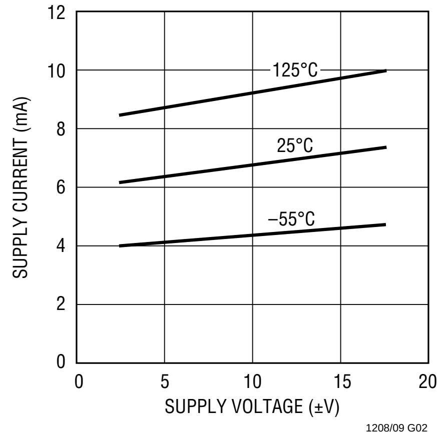
Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = $SR/2\pi V_P$.

TYPICAL PERFORMANCE CHARACTERISTICS

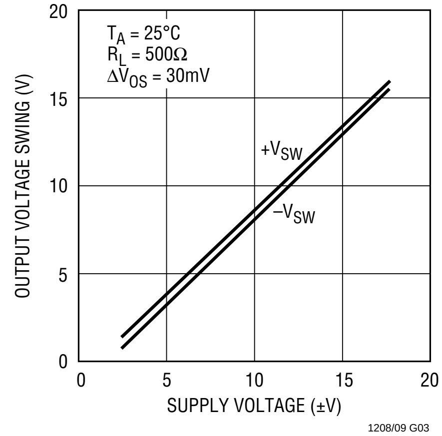
Input Common-Mode Range vs Supply Voltage



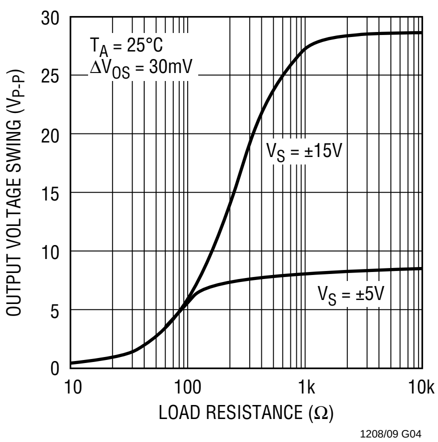
Supply Current vs Supply Voltage and Temperature



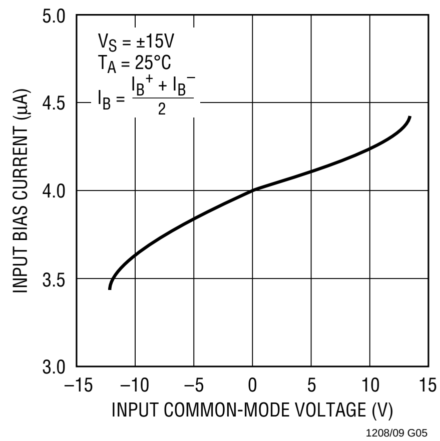
Output Voltage Swing vs Supply Voltage



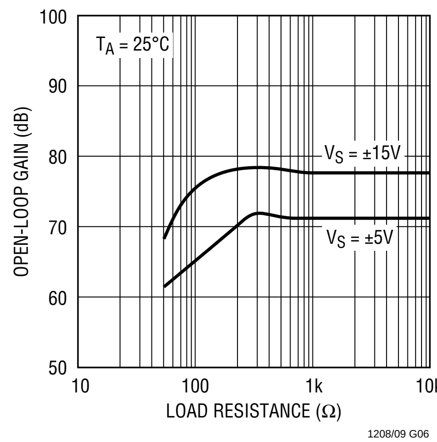
Output Voltage Swing vs Resistive Load



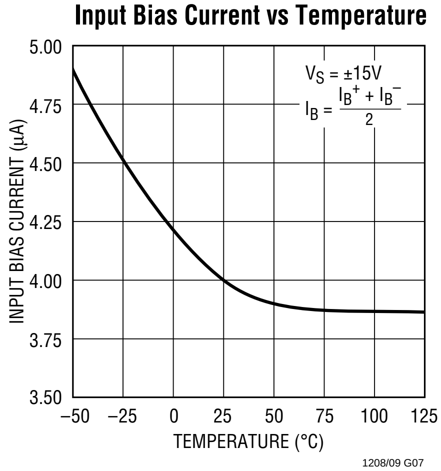
Input Bias Current vs Input Common-Mode Voltage



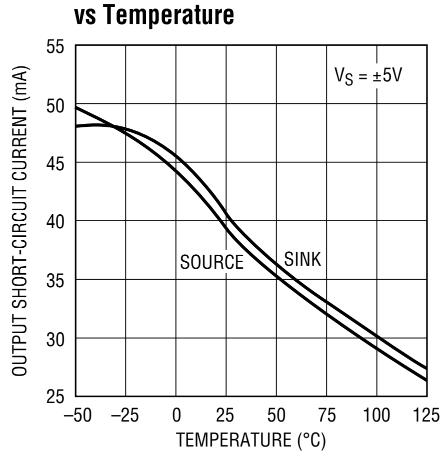
Open-Loop Gain vs Resistive Load



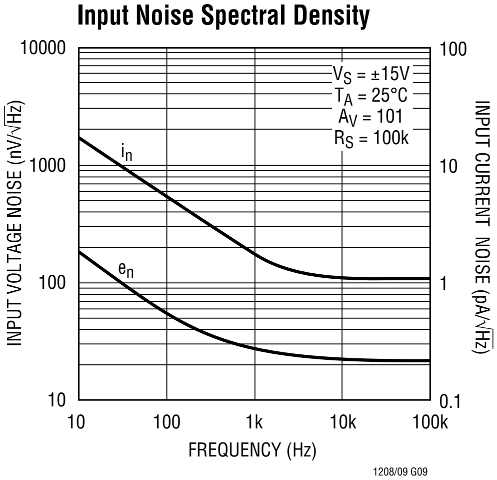
Input Bias Current vs Temperature



Output Short-Circuit Current vs Temperature

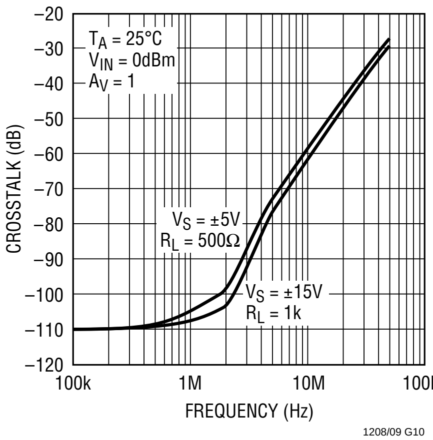


Input Noise Spectral Density

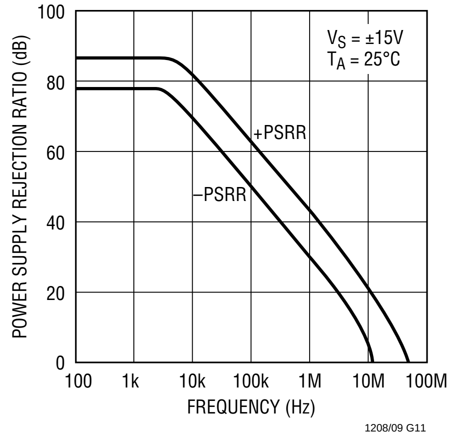


TYPICAL PERFORMANCE CHARACTERISTICS

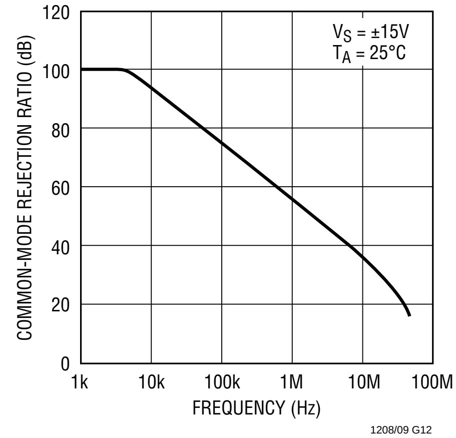
Crosstalk vs Frequency



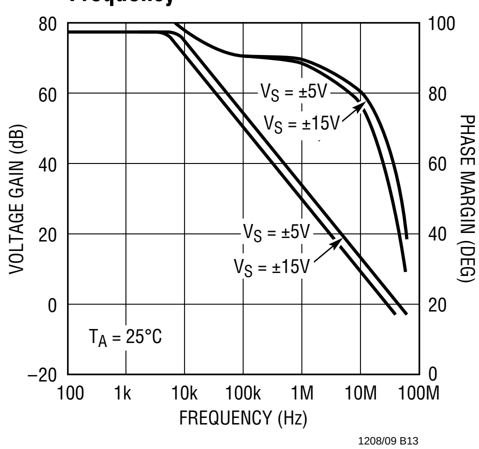
Power Supply Rejection Ratio vs Frequency



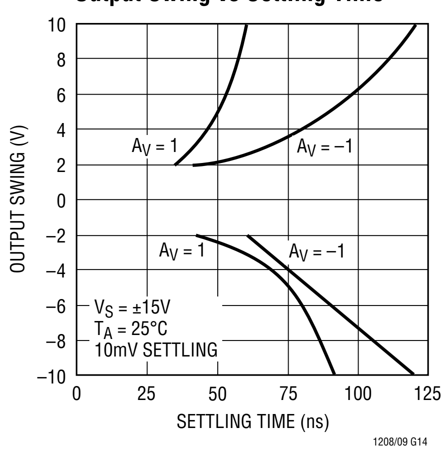
Common-Mode Rejection Ratio vs Frequency



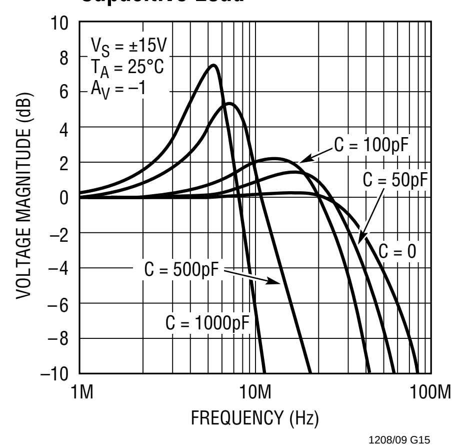
Voltage Gain and Phase vs Frequency



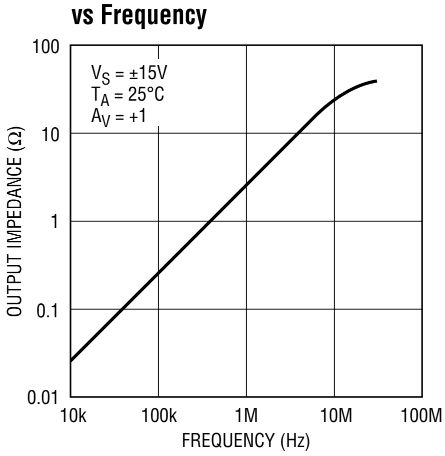
Output Swing vs Settling Time



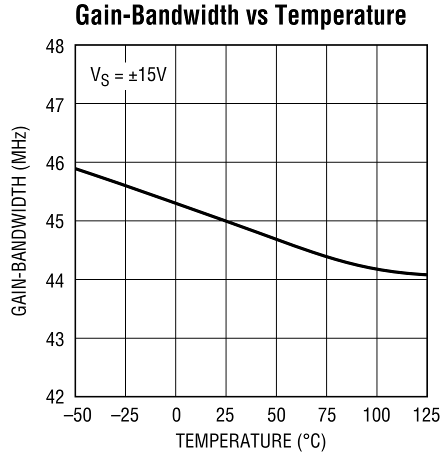
Frequency Response vs Capacitive Load



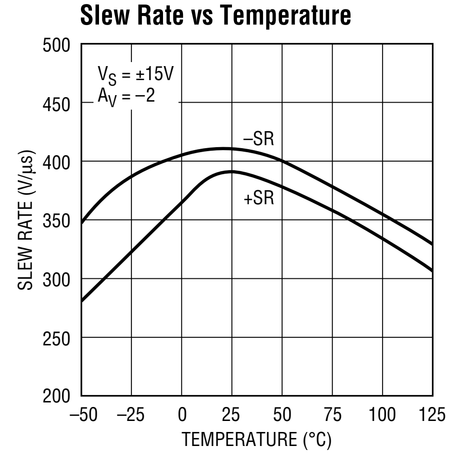
Closed-Loop Output Impedance vs Frequency



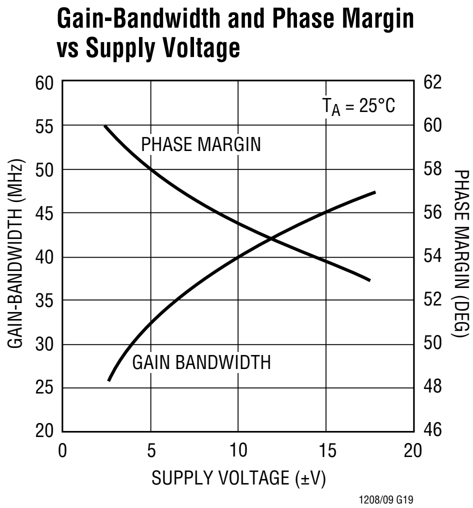
Gain-Bandwidth vs Temperature

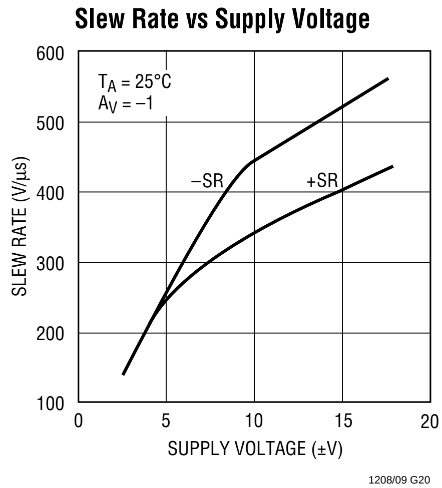


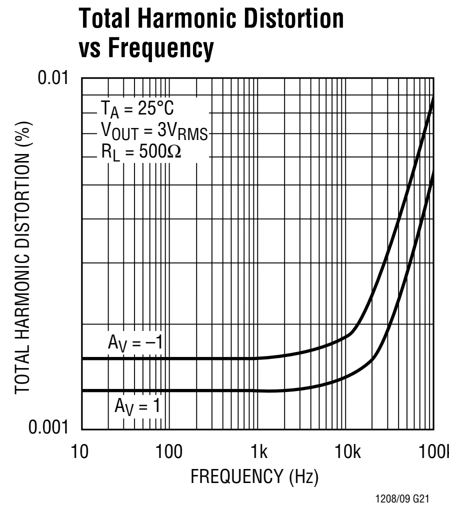
Slew Rate vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS







APPLICATIONS INFORMATION

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking. If feedback resistors greater than 5k are used, a parallel capacitor of value

$$C_F \geq R_G \times C_{IN}/R_F$$

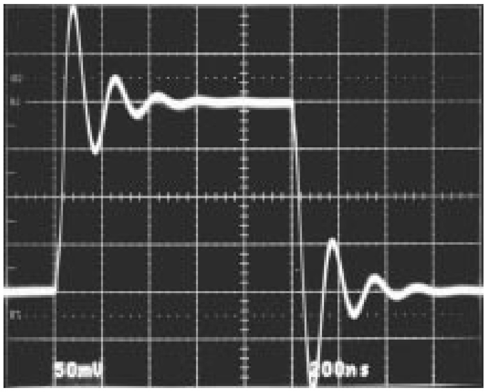
should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1208/LT1209 amplifiers are stable with capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small-signal response with 1000pF load shows 50% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current. To reduce peaking with capacitive loads, insert a small decoupling resistor between the output and the load, and add a capacitor between the output and inverting input to provide an AC feedback path. Coaxial cable can be driven directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

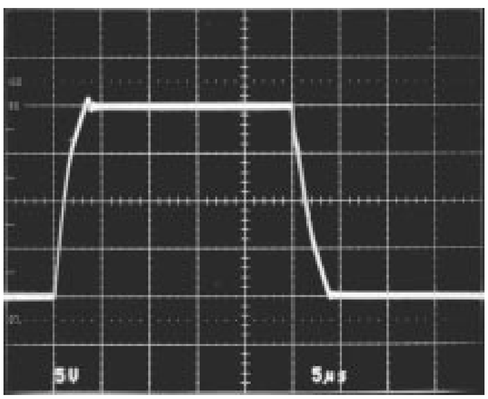
APPLICATIONS INFORMATION

Small-Signal Capacitive Loading



$A_V = -1$
$C_L = 1000pF$ 1208/09 AI01

Large-Signal Capacitive Loading



$A_V = 1$
$C_L = 10,000pF$ 1208/09 AI02

Input Considerations

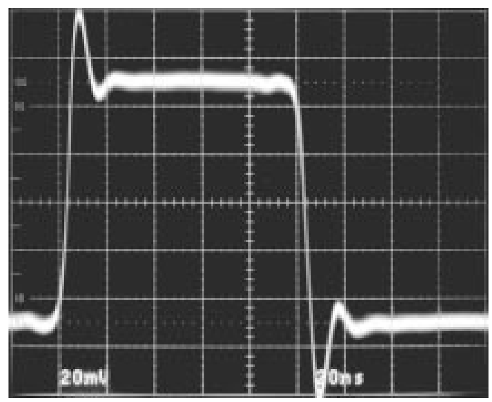
Resistors in series with the inputs are recommended for the LT1208/LT1209 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

Transient Response

The LT1208/LT1209 gain-bandwidth is 45MHz when measured at 100kHz. The actual frequency response in unity-gain is considerably higher than 45MHz due to peaking caused by a second pole beyond the unity-gain crossover. This is reflected in the 50° phase margin and shows up as overshoot in the unity-gain small-signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

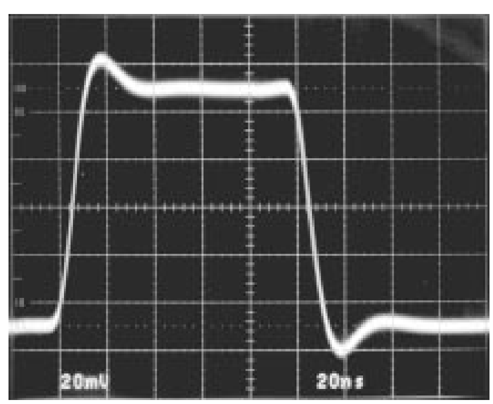
The large-signal response in both inverting and noninverting gain show symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common-mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1208/LT1209 so that the falling edge slew rate is balanced.

Small-Signal Transient Response



$A_V = 1$ 1208/09 AI03

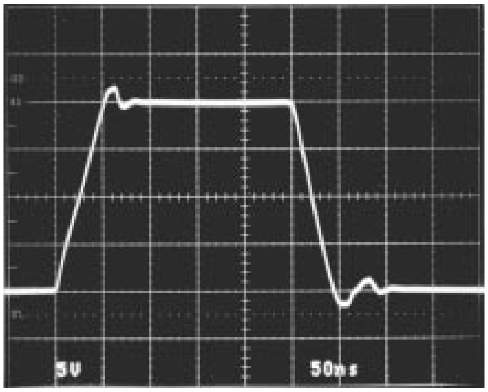
Small-Signal Transient Response



$A_V = -1$ 1208/09 AI04

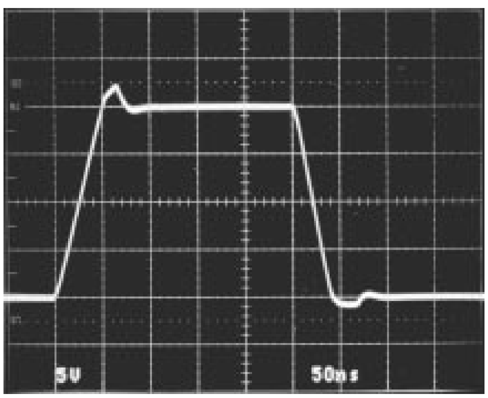
APPLICATIONS INFORMATION

Large-Signal Transient Response



$A_V = 1$ 1208/09 AI04

Large-Signal Transient Response



$A_V = -1$ 1208/09 AI06

Low Voltage Operation

The LT1208/LT1209 are functional at room temperature with only 3V of total supply voltage. Under this condition, however, the undistorted output swing is only $0.8V_{P-P}$. A more realistic condition is operation at ±2.5V supplies (or 5V and ground). Under these conditions, at room temperature, the typical input common-mode range is 1.9V to –1.3V (for a V_{OS} change of 1mV), and a 5MHz, $2V_{P-P}$ sine wave can be faithfully reproduced. With 5V total supply voltage the gain-bandwidth is reduced to 26MHz and the slew rate is reduced to 135V/μs.

Power Dissipation

The LT1208/LT1209 combine high speed and large output current drive in small packages. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions.

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1208CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1208CS8: $T_J = T_A + (P_D \times 150°C/W)$
LT1209CN: $T_J = T_A + (P_D \times 70°C/W)$
LT1209CS: $T_J = T_A + (P_D \times 100°C/W)$

Maximum power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage).

For each amplifier P_{DMAX} is as follows:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + \frac{(0.5V^+)^2}{R_L}$$

Example: LT1208 in S8 at 70°C, $V_S = \pm10V$, $R_L = 500\Omega$

$$P_{DMAX} = (20V)(10.5mA) + \frac{(5V)^2}{500\Omega} = 260mW$$

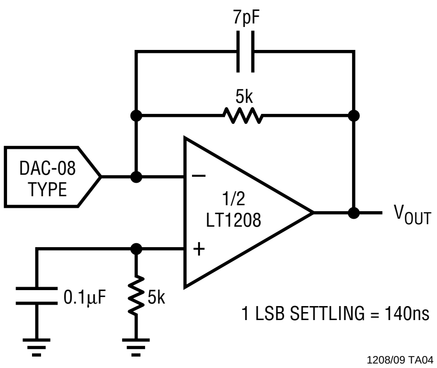
$$T_J = 70°C + (2 \times 260mW)(150°C/W) = 148°C$$

DAC Current-to-Voltage Converter

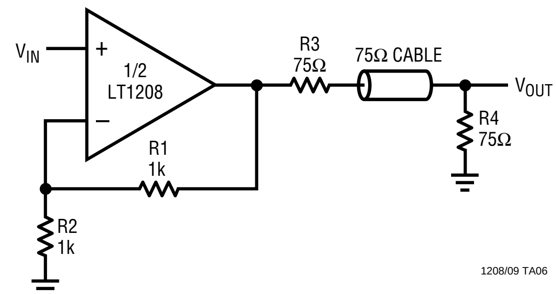
The wide bandwidth, high slew rate and fast settling time of the LT1208/LT1209 make them well-suited for current-to-voltage conversion after current output D/A converters. A typical application with a DAC-08 type converter (full-scale output of 2mA) uses a 5k feedback resistor. A 7pF compensation capacitor across the feedback resistor is used to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1208/LT1209 and DAC settles to less than 40mV (1LSB) in 140ns for a 10V step.

TYPICAL APPLICATIONS

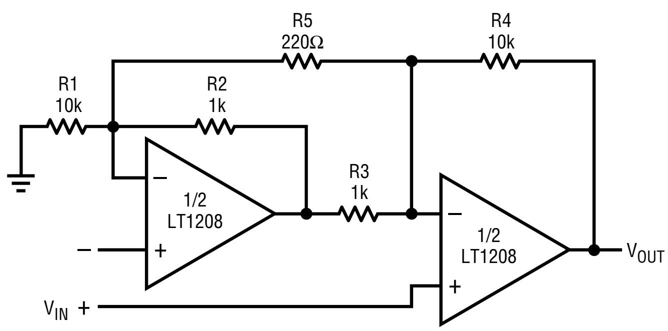
DAC Current-to-Voltage Converter



Cable Driving



Instrumentation Amplifier

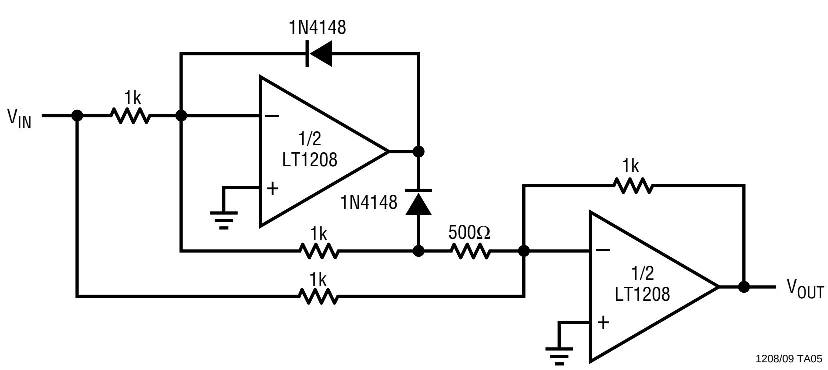


$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 102$$

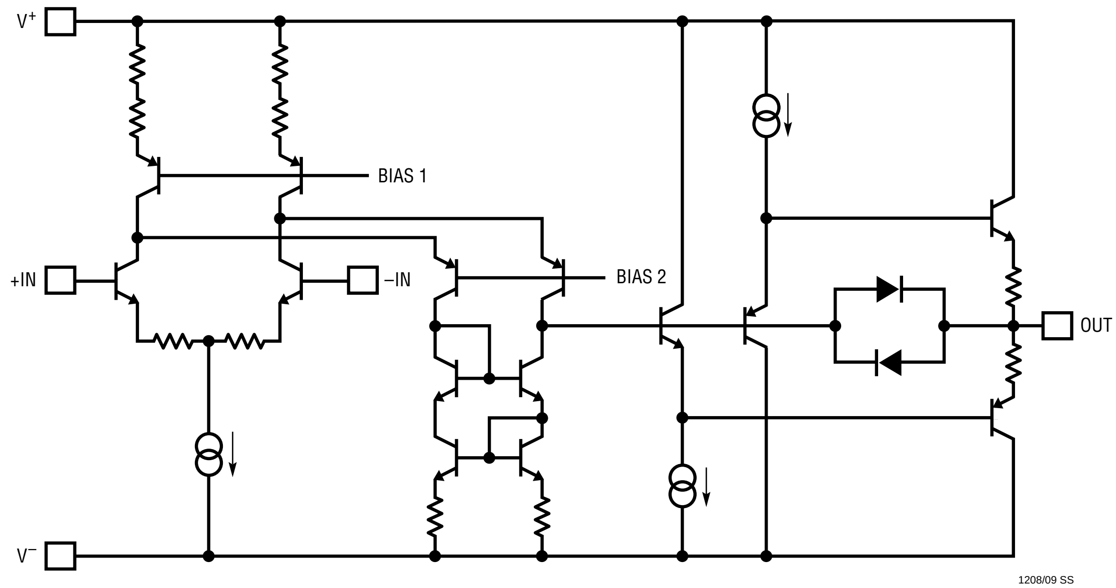
TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 430kHz

1208/09 TA03

Full-Wave Rectifier

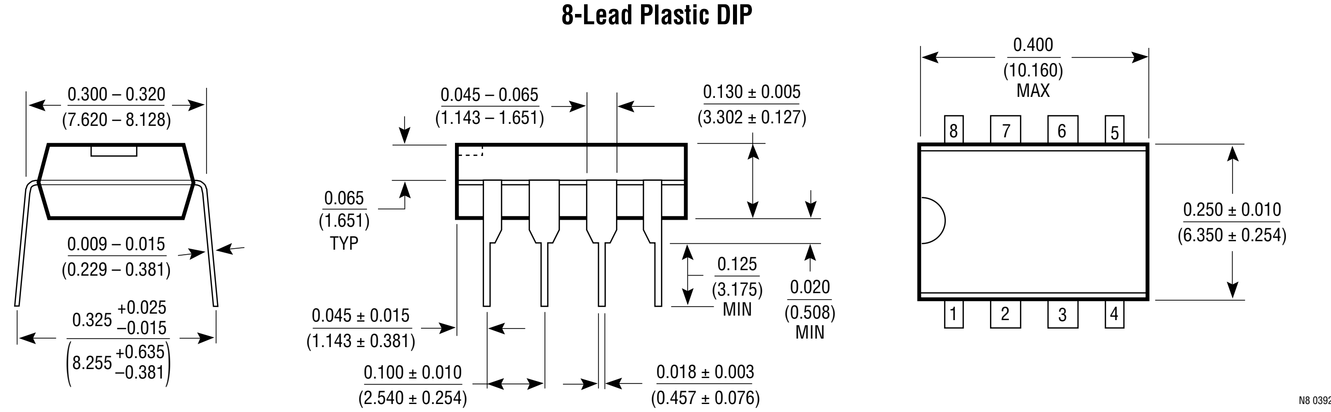


SIMPLIFIED SCHEMATIC

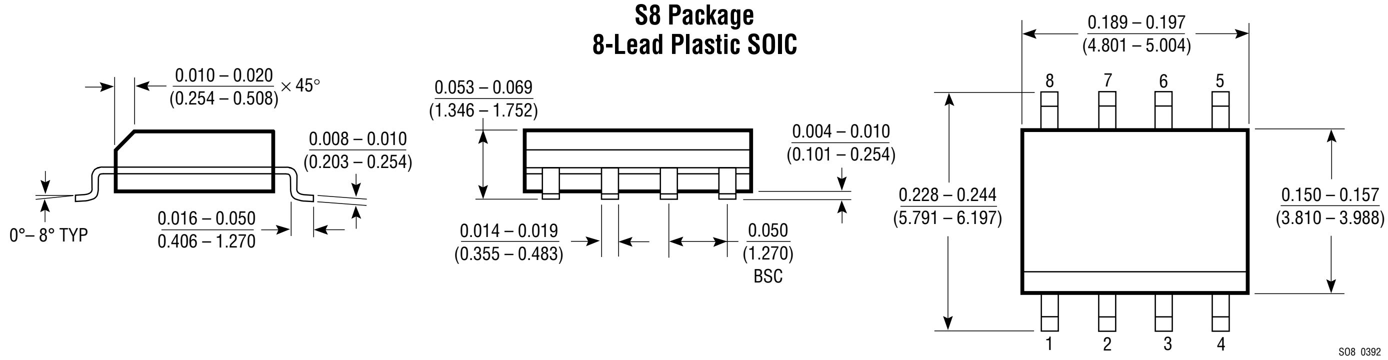


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC

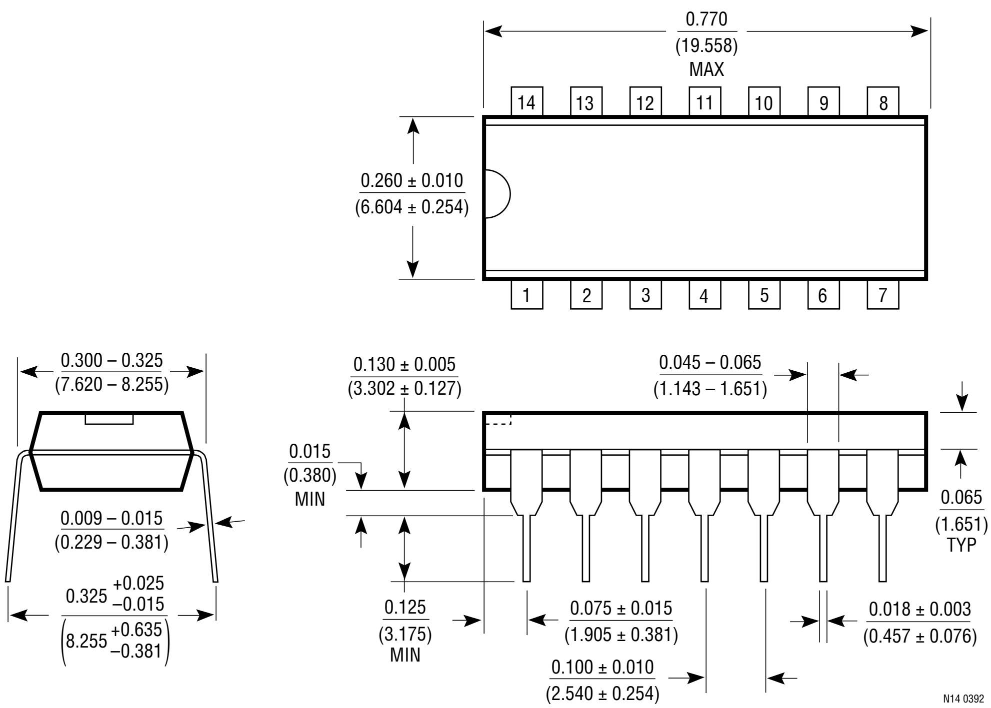


LINEAR TECHNOLOGY

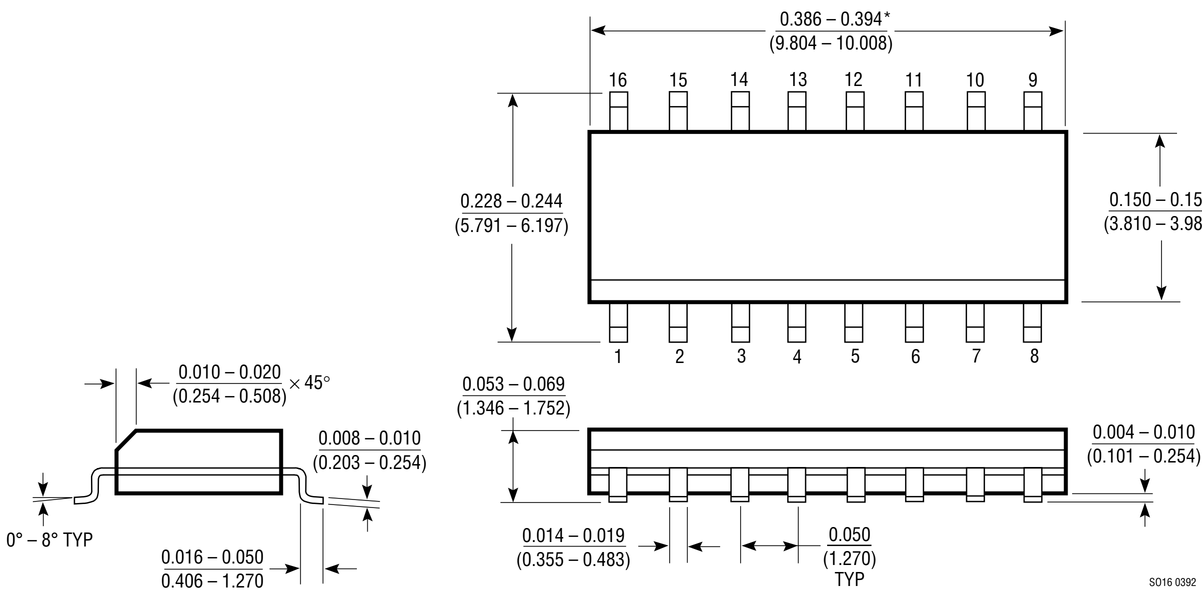
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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