LTC1407-1/LTC1407A-1

Serial 12-Bit/14-Bit, 3Msps Simultaneous Sampling ADCs with Shutdown

FEATURES

- **3Msps Sampling ADC with Two Simultaneous Differential Inputs**
- **1.5Msps Throughput per Channel**
- **Low Power Dissipation: 14mW (Typ)**
- **3V Single Supply Operation**
- ±1.25V Differential Input Range
- Pin Compatible 0V to 2.5V Input Range Version (LTC1407/LTC1407A)
- 2.5V Internal Bandgap Reference with External Overdrive
- 3-Wire Serial Interface
- Sleep (10µW) Shutdown Mode
- Nap (3mW) Shutdown Mode
- 80dB Common Mode Rejection at 100kHz
- Tiny 10-Lead MS Package

APPLICATIONS

- Telecommunications
- Data Acquisition Systems
- Uninterrupted Power Supplies
- Multiphase Motor Control
- I & Q Demodulation
- Industrial Radio

DESCRIPTION

The LTC®1407-1/LTC1407A-1 are 12-bit/14-bit, 3Msps ADCs with two 1.5Msps simultaneously sampled differential inputs. The devices draw only 4.7mA from a single 3V supply and come in a tiny 10-lead MS package. A Sleep shutdown feature lowers power consumption to 10µW. The combination of speed, low power and tiny package makes the LTC1407-1/LTC1407A-1 suitable for high speed, portable applications.

The LTC1407-1/LTC1407A-1 contain two separate differential inputs that are sampled simultaneously on the rising edge of the CONV signal. These two sampled inputs are then converted at a rate of 1.5Msps per channel.

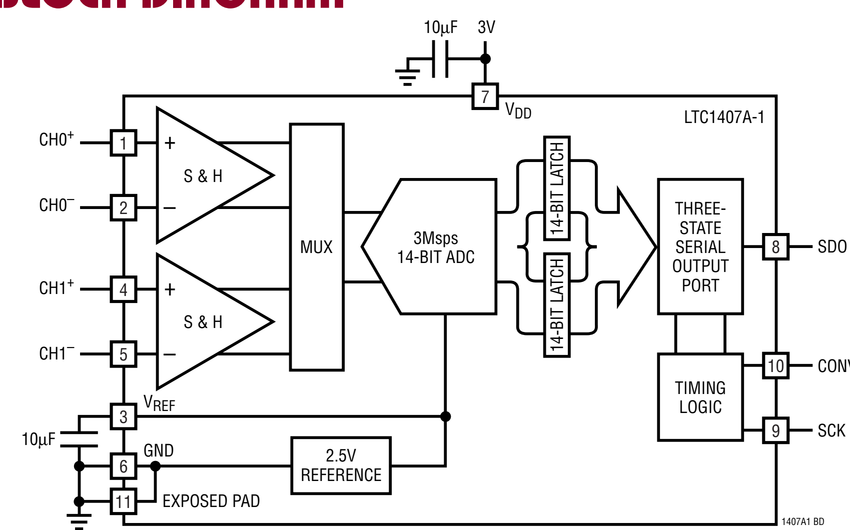
The 80dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The devices convert –1.25V to 1.25V bipolar inputs differentially. The absolute voltage swing for $CH0^+$, $CH0^-$, $CH1^+$ and $CH1^-$ extends from ground to the supply voltage.

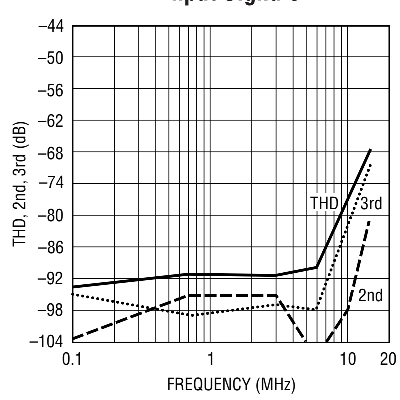
The serial interface sends out the two conversion results in 32 clocks for compatibility with standard serial interfaces.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
U.S. patent numbers 6084440, 6522187

BLOCK DIAGRAM



THD, 2nd and 3rd vs Input Frequency for Differential Input Signals

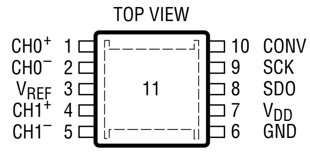


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 4V
Analog Input Voltage
(Note 3) .... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage .... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage .... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 100mW
Operation Temperature Range
LTC1407C-1/LTC1407AC-1 .... 0°C to 70°C
LTC1407I-1/LTC1407AI-1 .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 150°C/W
EXPOSED PAD IS GND (PIN 11)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC1407CMSE-1 LTC1407IMSE-1 LTC1407ACMSE-1 LTC1407AIMSE-1
MSE PART MARKING
LTBGT LTBGV LTBGW LTBGX

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V.

PARAMETER	CONDITIONS		LTC1407-1 MIN	LTC1407-1 TYP	LTC1407-1 MAX	LTC1407A-1 MIN	LTC1407A-1 TYP	LTC1407A-1 MAX	UNITS
Resolution (No Missing Codes)		●	12			14			Bits
Integral Linearity Error	(Notes 5, 17)	●	–2	±0.25	2	–4	±0.5	4	LSB
Offset Error	(Notes 4, 17)	●	–10	±1	10	–20	±2	20	LSB
Offset Match from CH0 to CH1	(Note 17)		–5	±0.5	5	–10	±1	10	LSB
Gain Error	(Notes 4, 17)	●	–30	±5	30	–60	±10	60	LSB
Gain Match from CH0 to CH1	(Note 17)		–5	±1	5	–10	±2	10	LSB
Gain Tempco	Internal Reference (Note 4) External Reference			±15 ±1			±15 ±1		ppm/°C ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Differential Input Range (Notes 3, 8, 9)	2.7V ≤ V_{DD} ≤ 3.3V			–1.25 to 1.25		V
V_{CM}	Analog Common Mode + Differential Input Range (Note 10)				0 to V_{DD}		V
I_{IN}	Analog Input Leakage Current		●			1	µA
C_{IN}	Analog Input Capacitance	(Note 18)			13		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	(Note 6)	●			39	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				0.3		ps
t_{SK}	Sample-and-Hold Aperture Skew from CH0 to CH1				200		ps
CMRR	Analog Input Common Mode Rejection Ratio	f_{IN} = 1MHz, V_{IN} = 0V to 3V f_{IN} = 100MHz, V_{IN} = 0V to 3V			–60 –15		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V. Single ended signal drive CH0+/CH1+ with CH0–/CH1– = 1.5V DC. Differential signals drive both inputs of each channel with V_{CM} = 1.5V DC.

SYMBOL	PARAMETER	CONDITIONS		LTC1407-1 MIN	LTC1407-1 TYP	LTC1407-1 MAX	LTC1407A-1 MIN	LTC1407A-1 TYP	LTC1407A-1 MAX	UNITS
SINAD	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal (Note 19)			70.5			73.5		dB
		750kHz Input Signal (Note 19)	●	68	70.5		70	73.5		dB
		100kHz Input Signal, External V_{REF} = 3.3V, V_{DD} ≥ 3.3V (Note 19)			72.0			76.3		dB
		750kHz Input Signal, External V_{REF} = 3.3V, V_{DD} ≥ 3.3V (Note 19)			72.0			76.3		dB
THD	Total Harmonic Distortion	100kHz First 5 Harmonics (Note 19)			–87			–90		dB
		750kHz First 5 Harmonics (Note 19)	●		–83	–77		–86	–80	dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal (Note 19)			–87			–90		dB
		750kHz Input Signal (Note 19)			–83			–86		dB
IMD	Intermodulation Distortion	$0.625V_{P-P}$ 1.4MHz Summed with $0.625V_{P-P}$, 1.56MHz into CH0+ and Inverted into CH0–. Also Applicable to CH1+ and CH1–			–82			–82		dB
	Code-to-Code Transition Noise	V_{REF} = 2.5V (Note 17)			0.25			1		LSB_{RMS}
	Full Power Bandwidth	V_{IN} = $2.5V_{P-P}$, SDO = $11585LSB_{P-P}$ (–3dBFS) (Note 15)			50			50		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB			5			5		MHz

INTERNAL REFERENCE CHARACTERISTICS

T_A = 25°C. V_{DD} = 3V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.5		V
V_{REF} Output Tempco			15		ppm/°C
V_{REF} Line Regulation	V_{DD} = 2.7V to 3.6V, V_{REF} = 2.5V		600		µV/V
V_{REF} Output Resistance	Load Current = 0.5mA		0.2		Ω
V_{REF} Settling Time			2		ms

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 3.3V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 2.7V	●			0.6	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 3V, I_{OUT} = –200µA	●	2.5	2.9		V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.7V, I_{OUT} = 160µA			0.05		V
		V_{DD} = 2.7V, I_{OUT} = 1.6mA	●		0.10	0.4	V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{DD}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT}				1		pF
I_{SOURCE}	Output Short-Circuit Source Current	V_{OUT} = 0V, V_{DD} = 3V			20		mA
I_{SINK}	Output Short-Circuit Sink Current	V_{OUT} = V_{DD} = 3V			15		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference, V_{DD} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage			2.7		3.6	V
I_{DD}	Supply Current	Active Mode, f_{SAMPLE} = 1.5Msps	●		4.7	7.0	mA
		Nap Mode	●		1.1	1.5	mA
		Sleep Mode (LTC1407)			2.0	15	µA
		Sleep Mode (LTC1407A)			2.0	10	µA
PD	Power Dissipation	Active Mode with SCK in Fixed State (Hi or Lo)			12		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency per Channel (Conversion Rate)		●	1.5			MHz
$t_{THROUGHPUT}$	Minimum Sampling Period (Conversion + Acquisiton Period)		●			667	ns
t_{SCK}	Clock Period	(Note 16)	●	19.6		10000	ns
t_{CONV}	Conversion Time	(Note 6)		32	34		SCLK cycles
t_1	Minimum Positive or Negative SCLK Pulse Width	(Note 6)		2			ns
t_2	CONV to SCK Setup Time	(Notes 6, 10)		3			ns
t_3	SCK Before CONV	(Note 6)		0			ns
t_4	Minimum Positive or Negative CONV Pulse Width	(Note 6)		4			ns
t_5	SCK to Sample Mode	(Note 6)		4			ns
t_6	CONV to Hold Mode	(Notes 6, 11)		1.2			ns
t_7	32nd SCK↑ to CONV↑ Interval (Affects Acquisition Period)	(Notes 6, 7, 13)		45			ns
t_8	Minimum Delay from SCK to Valid Bits 0 Through 11	(Notes 6, 12)		8			ns
t_9	SCK to Hi-Z at SDO	(Notes 6, 12)		6			ns
t_{10}	Previous SDO Bit Remains Valid After SCK	(Notes 6, 12)		2			ns
t_{12}	V_{REF} Settling Time After Sleep-to-Wake Transition	(Notes 6, 14)			2		ms

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground GND.

Note 3: When these pins are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below GND or greater than V_{DD} without latchup.

Note 4: Offset and range specifications apply for a single-ended $CH0^+$ or $CH1^+$ input with $CH0^-$ or $CH1^-$ grounded and using the internal 2.5V reference.

Note 5: Integral linearity is tested with an external 2.55V reference and is defined as the deviation of a code from the straight line passing through the actual endpoints of a transfer curve. The deviation is measured from the center of quantization band.

Note 6: Guaranteed by design, not subject to test.

Note 7: Recommended operating conditions.

Note 8: The analog input range is defined for the voltage difference between $CH0^+$ and $CH0^-$ or $CH1^+$ and $CH1^-$. Performance is specified with $CH0^-$ = 1.5V DC while driving $CH0^+$ and with $CH1^-$ = 1.5V DC while driving $CH1^+$.

Note 9: The absolute voltage at $CH0^+$, $CH0^-$, $CH1^+$ and $CH1^-$ must be within this range.

Note 10: If less than 3ns is allowed, the output data will appear one clock cycle later. It is best for CONV to rise half a clock before SCK, when running the clock at rated speed.

Note 11: Not the same as aperture delay. Aperture delay (1ns) is the difference between the 2.2ns delay through the sample-and-hold and the 1.2ns CONV to Hold mode delay.

Note 12: The rising edge of SCK is guaranteed to catch the data coming out into a storage latch.

Note 13: The time period for acquiring the input signal is started by the 32nd rising clock and it is ended by the rising edge of CONV.

Note 14: The internal reference settles in 2ms after it wakes up from Sleep mode with one or more cycles at SCK and a 10µF capacitive load.

Note 15: The full power bandwidth is the frequency where the output code swing drops by 3dB with a $2.5V_{P-P}$ input sine wave.

Note 16: Maximum clock period guarantees analog performance during conversion. Output data can be read with an arbitrarily long clock period.

Note 17: The LTC1407A-1 is measured and specified with 14-bit Resolution (1LSB = 152µV) and the LTC1407-1 is measured and specified with 12-bit Resolution (1LSB = 610µV).

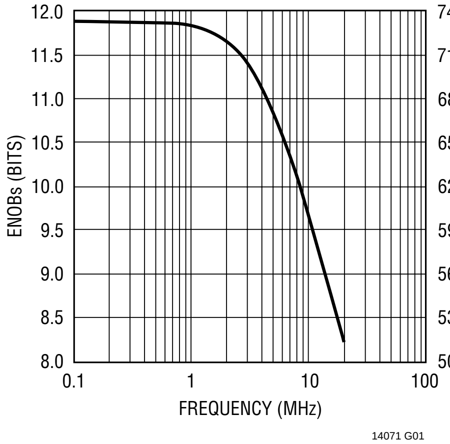
Note 18: The sampling capacitor at each input accounts for 4.1pF of the input capacitance.

Note 19: Full-scale sinewaves are fed into the noninverting inputs while the inverting inputs are kept at 1.5V DC.

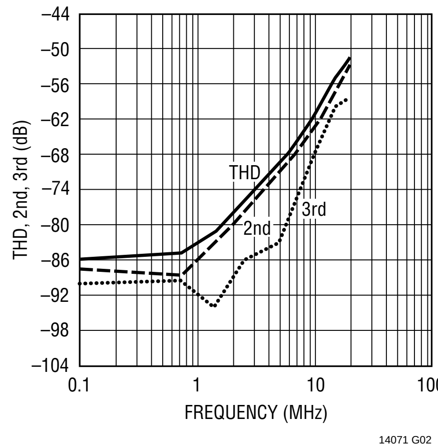
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, T_A = 25°C. Single ended signals drive +CH0/+CH1 with –CH0/–CH1 = 1.5V DC, differential signals drive both inputs with V_{CM} = 1.5V DC (LTC1407A-1)

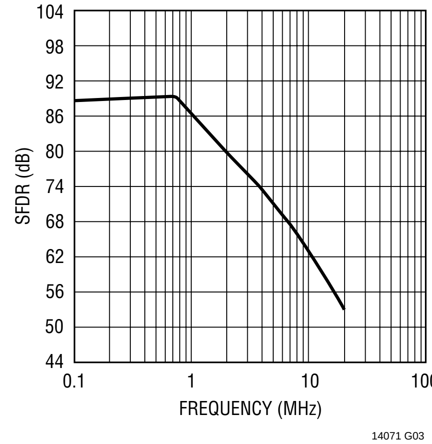
ENOBs and SINAD vs Input Sinewave Frequency



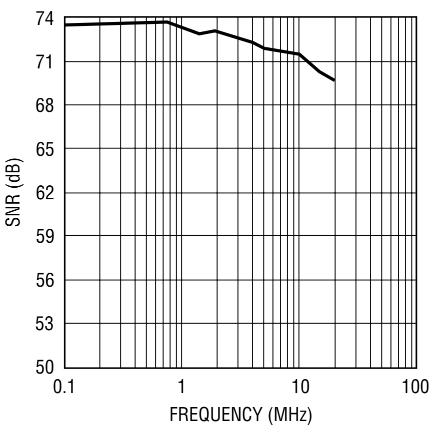
THD, 2nd and 3rd vs Input Frequency



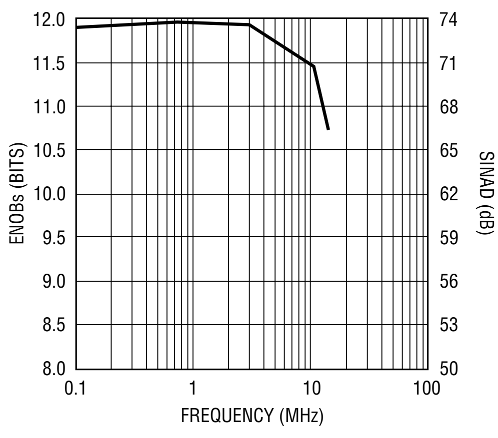
SFDR vs Input Frequency



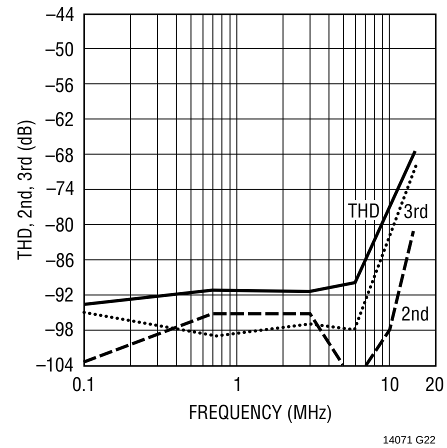
SNR vs Input Frequency



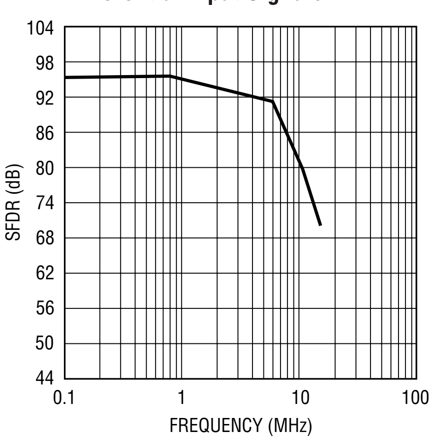
ENOBs and SINAD vs Input Sinewave Frequency for Differential Input Signals



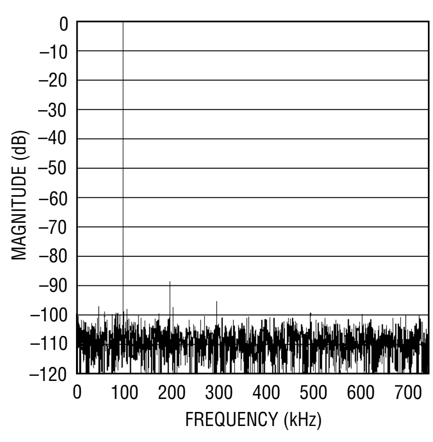
THD, 2nd and 3rd vs Input Frequency for Differential Input Signals



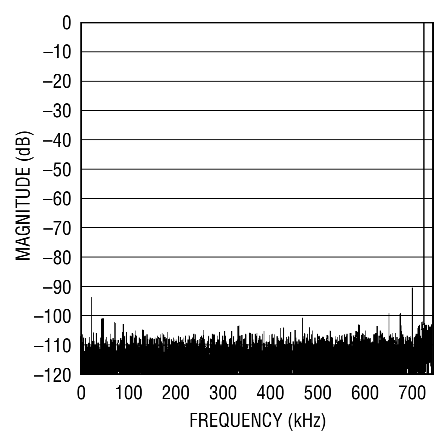
SFDR vs Input Frequency for Differential Input Signals



98kHz Sine Wave 4096 Point FFT Plot



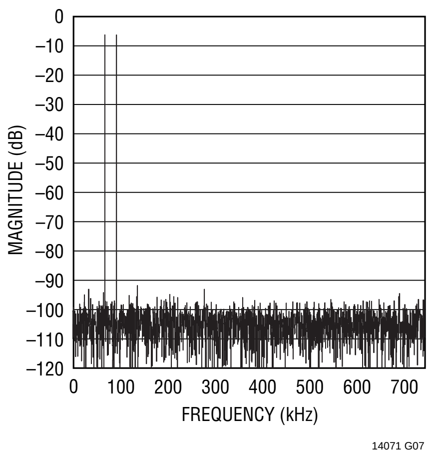
748kHz Sine Wave 4096 Point FFT Plot



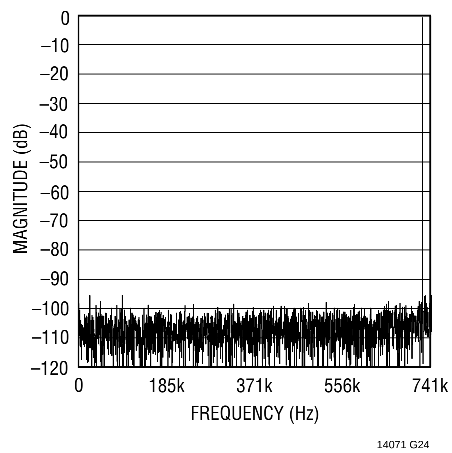
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, T_A = 25°C. Single ended signals drive +CH0/+CH1 with –CH0/–CH1 = 1.5V DC, differential signals drive both inputs with V_{CM} = 1.5V DC (LTC1407A-1)

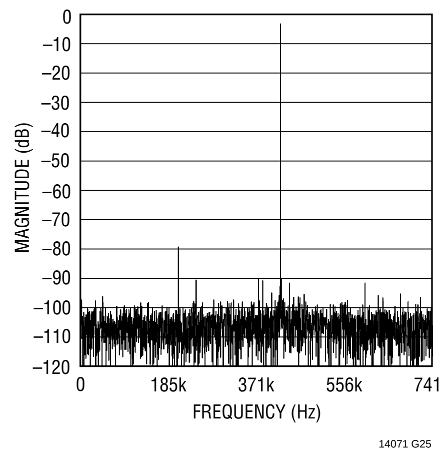
1403kHz Input Summed with 1563kHz Input IMD 4096 Point FFT Plot for Differential Input Signals



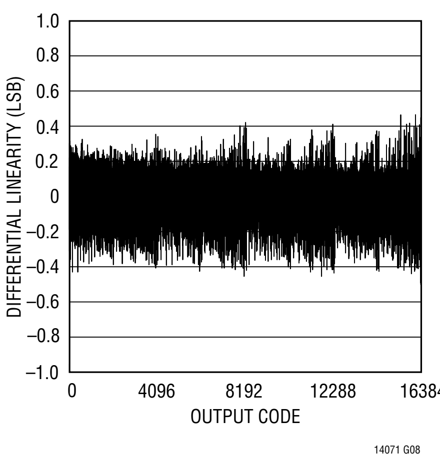
748kHz Sine Wave 4096 Point FFT Plot for Differential Input Signals



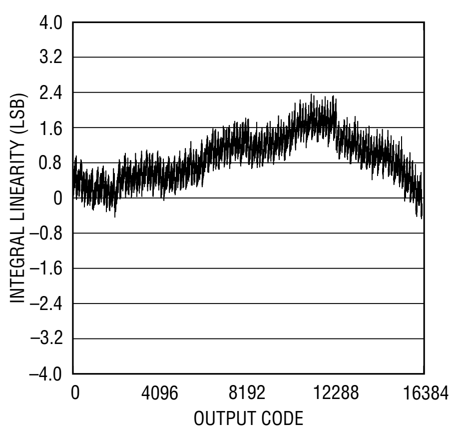
10.7MHz Sine Wave 4096 Point FFT Plot for Differential Input Signals



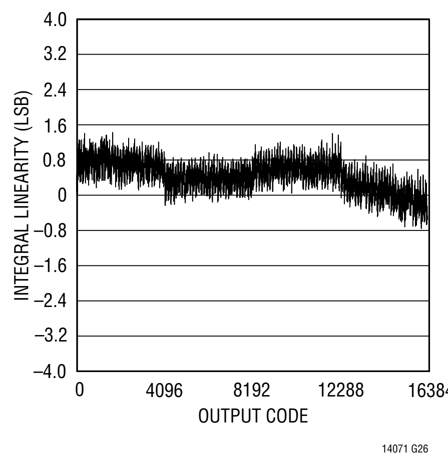
Differential Linearity for CH0 with Internal 2.5V Reference



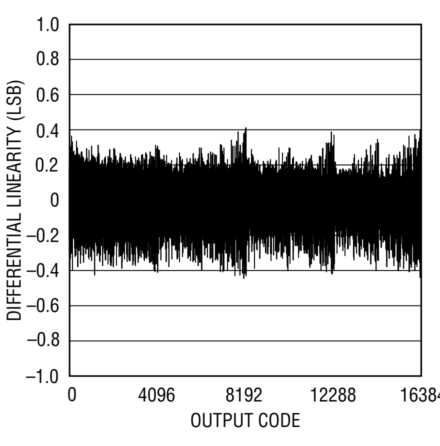
Integral Linearity End Point Fit for CH0 with Internal 2.5V Reference



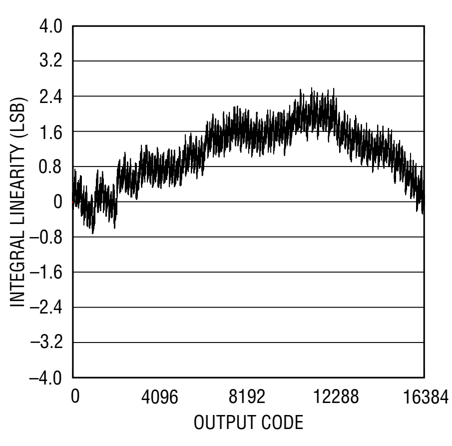
Integral Linearity End Point Fit for CH0 with Internal 2.5V Reference for Differential Input Signals



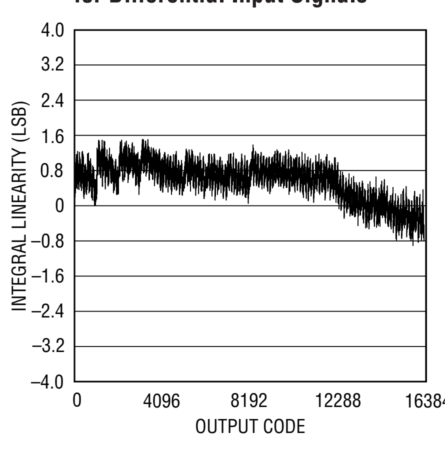
Differential Linearity for CH1 with Internal 2.5V Reference



Integral Linearity End Point Fit for CH1 with Internal 2.5V Reference



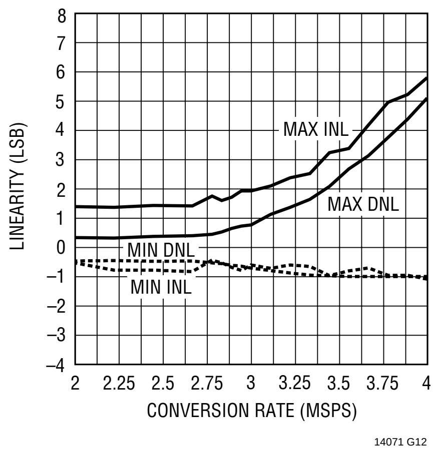
Integral Linearity End Point Fit for CH1 with Internal 2.5V Reference for Differential Input Signals



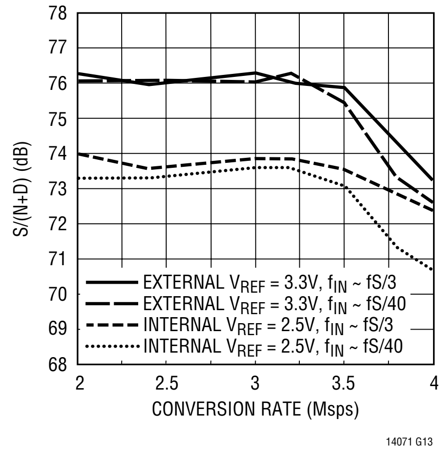
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3V, T_A = 25°C. Single ended signals drive +CH0/+CH1 with –CH0/–CH1 = 1.5V DC, differential signals drive both inputs with V_{CM} = 1.5V DC (LTC1407A-1)

Differential and Integral Linearity vs Conversion Rate

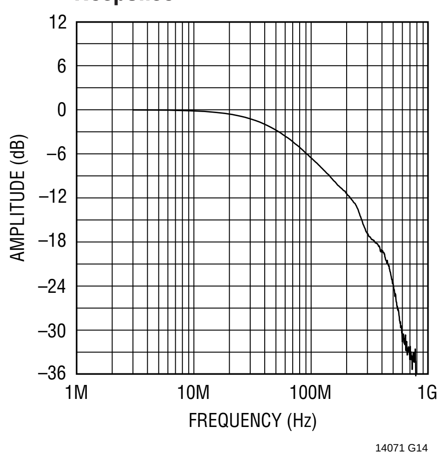


SINAD vs Conversion Rate

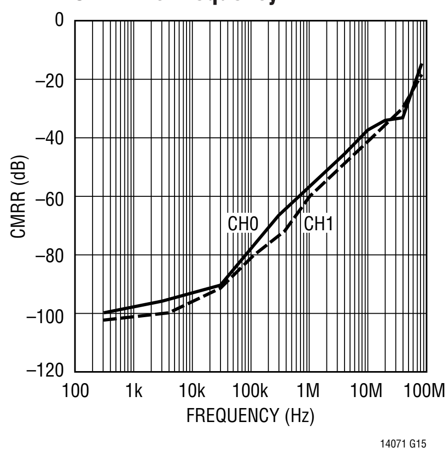


V_{DD} = 3V, T_A = 25°C (LTC1407-1/LTC1407A-1)

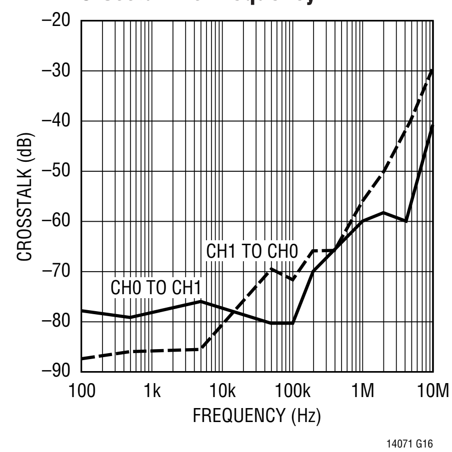
Full-Scale Signal Frequency Response



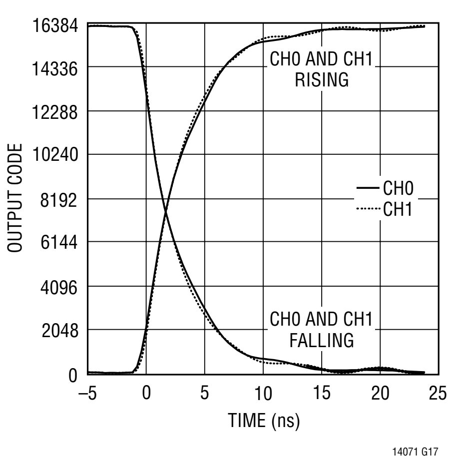
CMRR vs Frequency



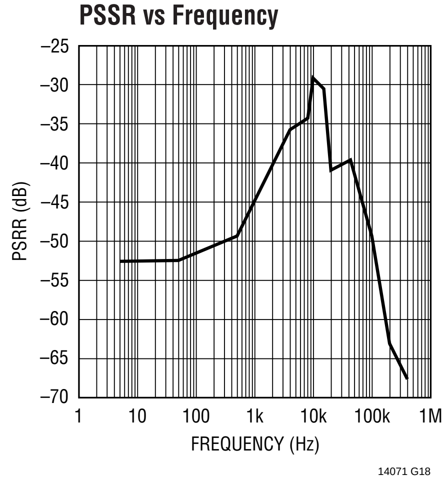
Crosstalk vs Frequency



Output Match with Simultaneous Input Steps at CH0 and CH1 from 25Ω

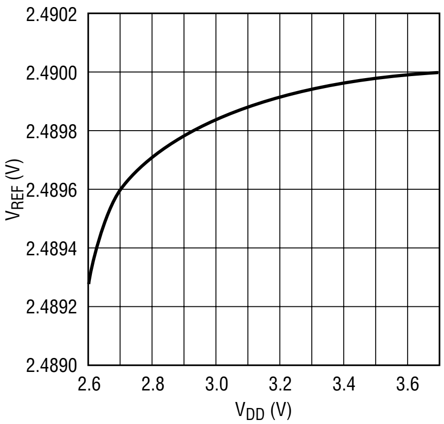


PSSR vs Frequency

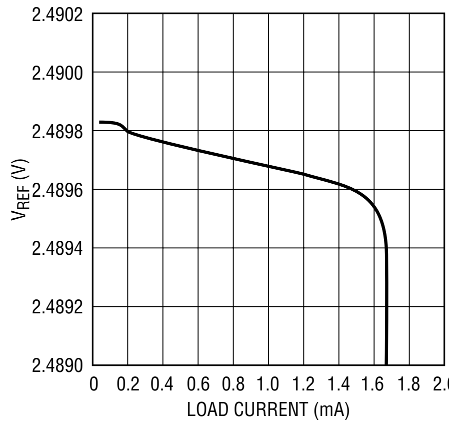


TYPICAL PERFORMANCE CHARACTERISTICS V_{DD} = 3V, T_A = 25°C (LTC1407-1/LTC1407A-1)

Reference Voltage vs V_{DD}



Reference Voltage vs Load Current



PIN FUNCTIONS

$CH0^+$ (Pin 1): Noninverting Channel 0. $CH0^+$ operates fully differentially with respect to $CH0^-$, with a –1.25V to 1.25V differential swing with respect to $CH0^-$ and a 0 to V_{DD} absolute input range.

$CH0^-$ (Pin 2): Inverting Channel 0. $CH0^-$ operates fully differentially with respect to $CH0^+$, with a 1.25V to –1.25V differential swing with respect to $CH0^+$ and a 0 to V_{DD} absolute input range.

V_{REF} (Pin 3): 2.5V Internal Reference. Bypass to GND and a solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic). Can be overdriven by an external reference voltage ≥2.55V and $\leq V_{DD}$.

$CH1^+$ (Pin 4): Noninverting Channel 1. $CH1^+$ operates fully differentially with respect to $CH1^-$, with a –1.25V to 1.25V differential swing with respect to $CH1^-$ and a 0 to V_{DD} absolute input range.

$CH1^-$ (Pin 5): Inverting Channel 1. $CH1^-$ operates fully differentially with respect to $CH1^+$, with a 1.25V to –1.25V differential swing with respect to $CH1^+$ and a 0 to V_{DD} absolute input range.

GND (Pins 6, 11): Ground and Exposed Pad. This single ground pin and the Exposed Pad must be tied directly to the solid ground plane under the part. Keep in mind that analog signal currents and digital output signal currents flow through these connections.

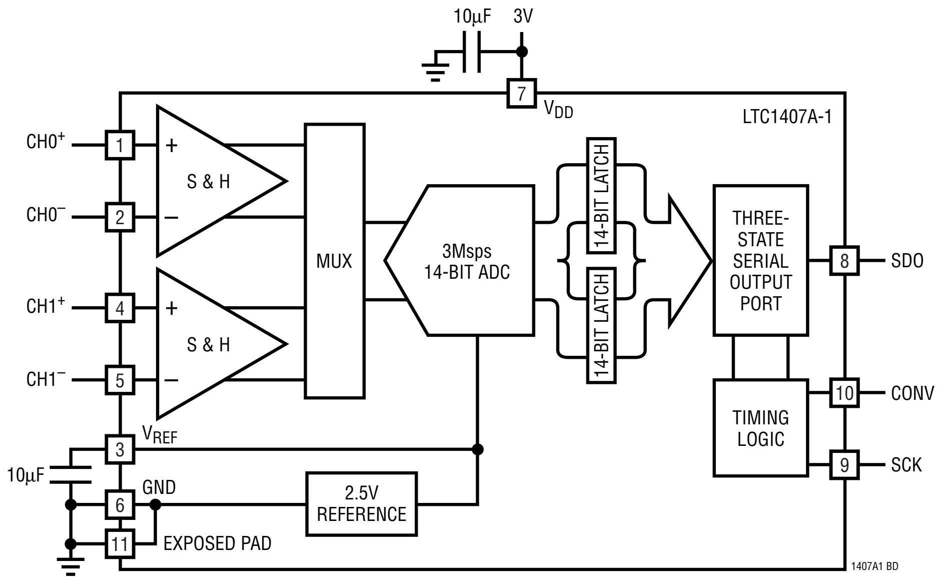
V_{DD} (Pin 7): 3V Positive Supply. This single power pin supplies 3V to the entire chip. Bypass to GND pin and solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum) in parallel with 0.1µF ceramic. Keep in mind that internal analog currents and digital output signal currents flow through this pin. Care should be taken to place the 0.1µF bypass capacitor as close to Pins 6 and 7 as possible.

SDO (Pin 8): Three-state Serial Data Output. Each pair of output data words represent the two analog input channels at the start of the previous conversion. The output format is 2's complement.

SCK (Pin 9): External Clock Input. Advances the conversion process and sequences the output data on the rising edge. One or more pulses wake from sleep.

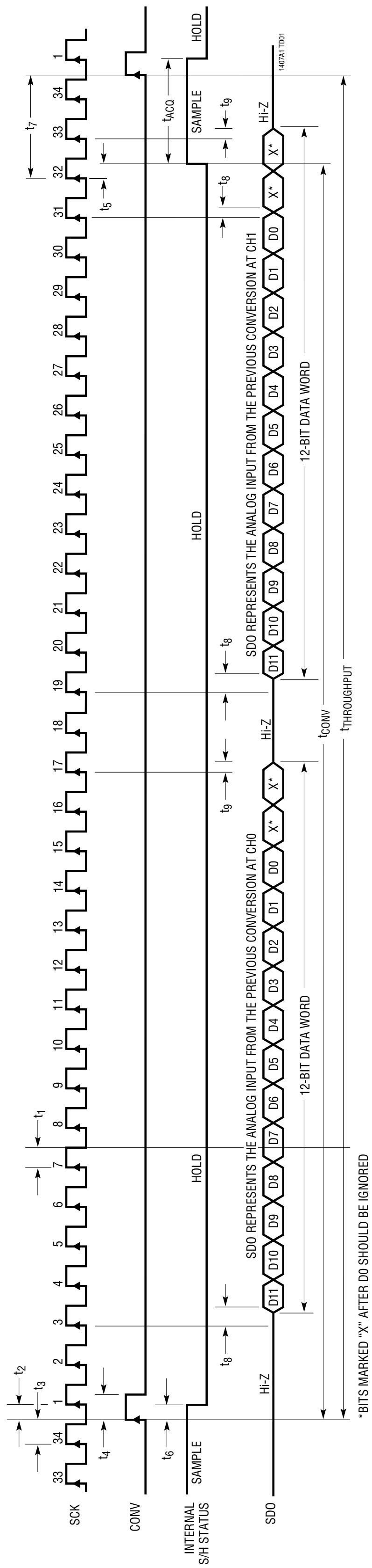
CONV (Pin 10): Convert Start. Holds the two analog input signals and starts the conversion on the rising edge. Two pulses with SCK in fixed high or fixed low state starts Nap mode. Four or more pulses with SCK in fixed high or fixed low state starts Sleep mode.

BLOCK DIAGRAM

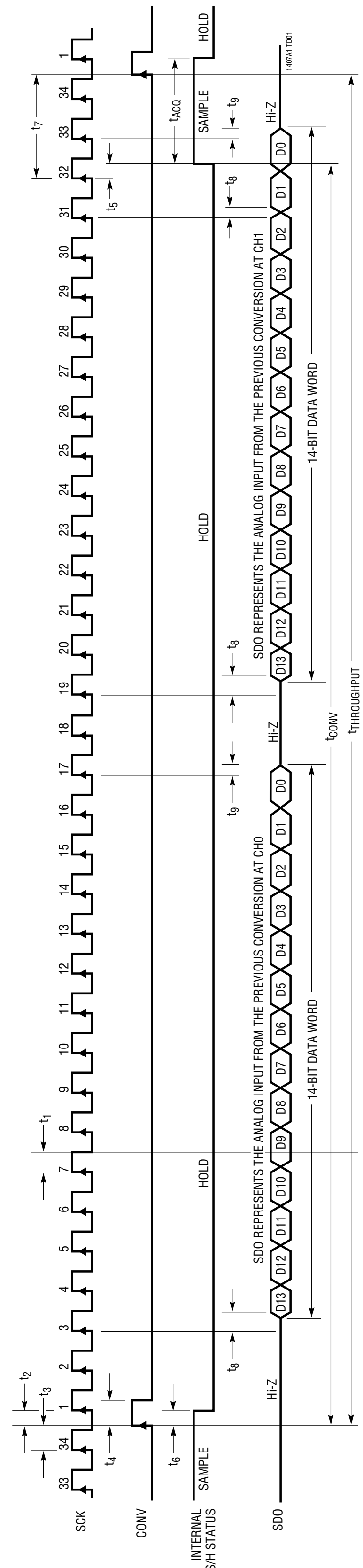


TIMING DIAGRAMS

LTC1407 Timing Diagram

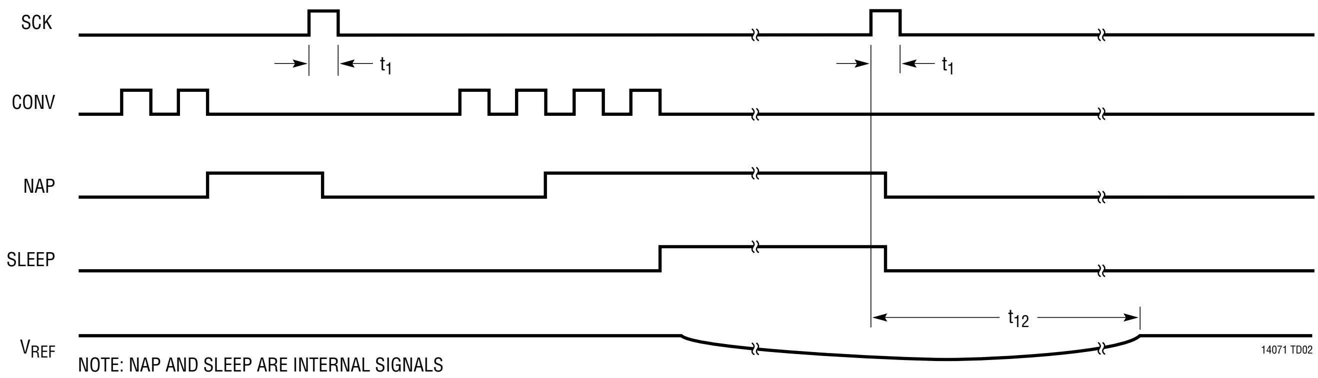


LTC1407A Timing Diagram

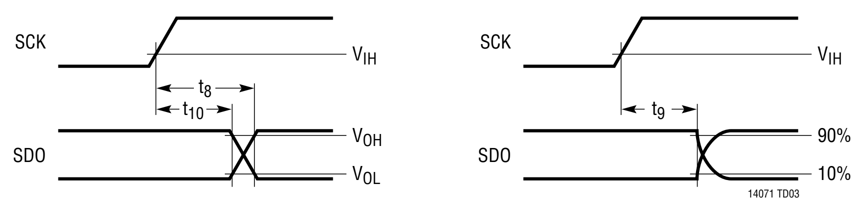


TIMING DIAGRAMS

Nap Mode and Sleep Mode Waveforms



SCK to SDO Delay



APPLICATIONS INFORMATION

DRIVING THE ANALOG INPUT

The differential analog inputs of the LTC1407-1/LTC1407A-1 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $CH0^-$ input is AC grounded at $V_{CC}/2$). All four analog inputs of both differential analog input pairs, $CH0^+$ with $CH0^-$ and $CH1^+$ with $CH1^-$, are sampled at the same instant. Any unwanted signal that is common to both inputs of each input pair will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1407-1/LTC1407A-1 inputs can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier must be used. The main requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 39ns for full throughput rate). Also keep in mind, while choosing an input amplifier, the amount of noise and harmonic distortion added by the amplifier.

CHOOSING AN INPUT AMPLIFIER

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (< 100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC1407-1/LTC1407A-1 depends on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1407-1/LTC1407A-1. (More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.)

LTC1566-1: Low Noise 2.3MHz Continuous Time Lowpass Filter.

LT®1630: Dual 30MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 500μV offset and 520ns settling to 0.5LSB for a 4V swing. THD and noise are –93dB to 40kHz and below 1LSB to 320kHz ($A_V = 1$, $2V_{P-P}$ into 1kΩ, $V_S = 5V$), making the part excellent for AC applications (to 1/3 Nyquist) where rail-to-rail performance is desired. Quad version is available as LT1631.

LT1632: Dual 45MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 1.5mV offset and 400ns settling to 0.5LSB for a 4V swing. It is suitable for applications with a single 5V supply. THD and noise are –93dB to 40kHz and below 1LSB to 800kHz ($A_V = 1$, $2V_{P-P}$ into 1kΩ, $V_S = 5V$), making the part excellent for AC applications where rail-to-rail performance is desired. Quad version is available as LT1633.

LT1801: 80MHz GBWP, –75dBc at 500kHz, 2mA/amplifier, 8.5nV/√Hz.

LT1806/LT1807: 325MHz GBWP, –80dBc distortion at 5MHz, unity gain stable, rail-to-rail in and out, 10mA/amplifier, 3.5nV/√Hz.

LT1810: 180MHz GBWP, –90dBc distortion at 5MHz, unity gain stable, rail-to-rail in and out, 15mA/amplifier, 16nV/√Hz.

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LT1818/LT1819: 400MHz, 2500V/µs, 9mA, Single/Dual Voltage Mode Operational Amplifier.

LT6200: 165MHz GBWP, –85dBc distortion at 1MHz, unity gain stable, rail-to-rail in and out, 15mA/amplifier, 0.95nV/√Hz.

LT6203: 100MHz GBWP, –80dBc distortion at 1MHz, unity gain stable, rail-to-rail in and out, 3mA/amplifier, 1.9nV/√Hz.

LT6600: Amplifier/Filter Differential In/Out with 10MHz Cutoff.

INPUT FILTERING AND SOURCE IMPEDANCE

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1407-1/LTC1407A-1 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 50MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 1 shows a 47pF capacitor from $CH0^+$ to ground and a 51Ω source resistor to limit the net input bandwidth to 30MHz. The 47pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling-glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silvermica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency a multiple pole filter is required.

High external source resistance, combined with 13pF of input capacitance, will reduce the rated 50MHz input bandwidth and increase acquisition time beyond 39ns.

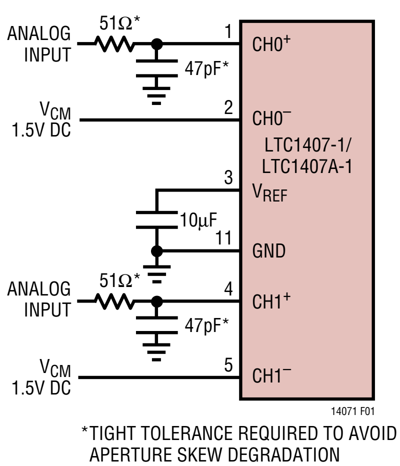

Figure 1. RC Input Filter

INPUT RANGE

The analog inputs of the LTC1407-1/LTC1407A-1 may be driven fully differentially with a single supply. Either input may swing up to 3V, provided the differential swing is no greater than 1.25V. In the valid input range, each input of each channel is always up to ±1.25V away from the other input of each channel. The –1.25V to 1.25V range is also ideally suited for AC-coupled signals in single supply applications. Figure 2 shows how to AC couple signals in a single supply system without needing a mid-supply 1.5V DC external reference. The DC common mode level is supplied by the previous stage that is already bounded by single supply voltage of the system. The common mode range of the inputs extends from ground to the supply voltage V_{DD}. If the difference between the $CH0^+$ and $CH0^–$ inputs or the $CH1^+$ and $CH1^–$ inputs exceeds 1.25V, the output code will stay fixed at zero and all ones, and if this difference goes below –1.25V, the ouput code will stay fixed at one and all zeros.

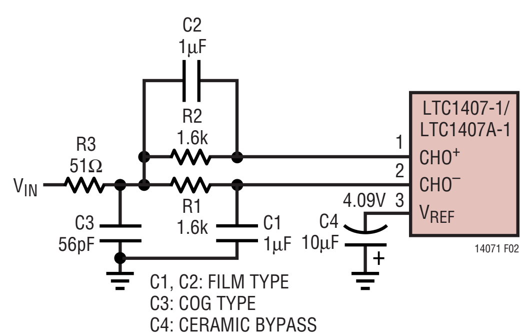

Figure 2. AC Coupling of AC Signals with 1kHz Low Cut

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INTERNAL REFERENCE

The LTC1407-1/LTC1407A-1 have an on-chip, temperature compensated, bandgap reference that is factory trimmed near 2.5V to obtain a precise ±1.25V input span. The reference amplifier output V_{REF}, (Pin 3) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or a 10µF tantalum in parallel with a 0.1µF ceramic is recommended. The V_{REF} pin can be overdriven with an external reference as shown in Figure 3. The voltage of the external reference must be higher than the 2.5V of the open-drain P-channel output of the internal reference. The recommended range for an external reference is 2.55V to V_{DD}. An external reference at 2.55V will see a DC quiescent load of 0.75mA and as much as 3mA during conversion.

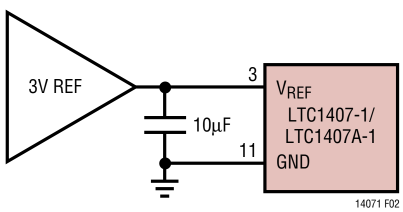

Figure 3

INPUT SPAN VERSUS REFERENCE VOLTAGE

The differential input range has a unipolar voltage span that equals the difference between the voltage at the reference buffer output V_{REF} (Pin 3) and the voltage at the Exposed Pad ground. The differential input range of ADC is –1.25V to 1.25V when using the internal reference. The internal ADC is referenced to these two nodes. This relationship also holds true with an external reference.

DIFFERENTIAL INPUTS

The ADC will always convert the bipolar difference of $CH0^+$ minus $CH0^-$ or the bipolar difference of $CH1^+$ minus $CH1^-$, independent of the common mode voltage at either set of inputs. The common mode rejection holds up at high frequencies (see Figure 4). The only requirement is that both inputs not go below ground or exceed V_{DD}. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are largely independent of the common mode voltage. However, the offset error will vary. CMRR is typically better than 60dB.

Figure 5 shows the ideal input/output characteristics for the LTC1407-1/LTC1407A-1. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, FS – 1.5LSB). The output code is 2's complement with 1LSB = 2.5V/16384 = 153µV for the LTC1407A-1 and 1LSB = 2.5V/4096 = 610µV for the LTC1407-1. The LTC1407A-1 has 1LSB RMS of Gaussian white noise. Figure 6a shows the LTC1819 converting a single ended input signal to differential input signals for optimum THD and SFDR performance as shown in the FFT plot (Figure 6b).

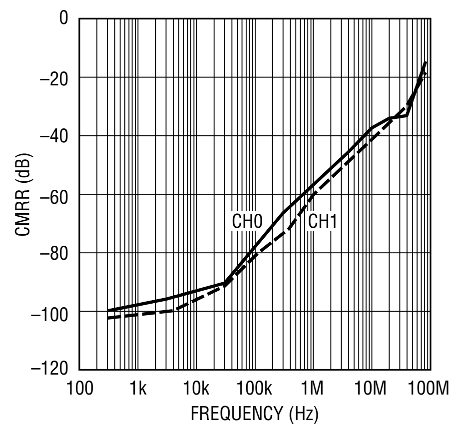

Figure 4. CMRR vs Frequency

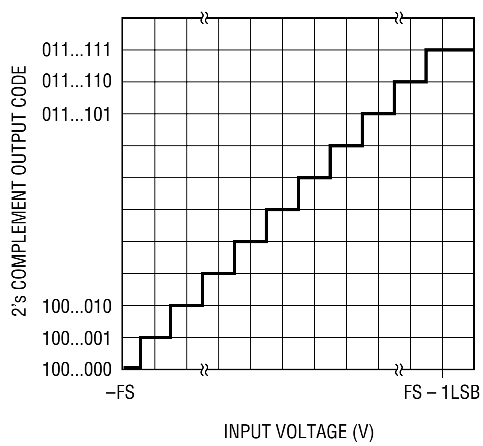

Figure 5. LTC1407-1/LTC1407A-1 Transfer Characteristic

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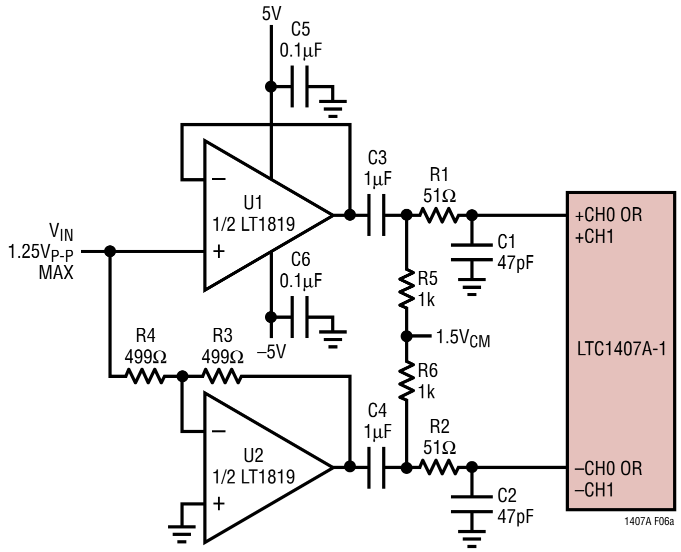

Figure 6a. The LT1819 Driving the LTC1407A-1 Differentially

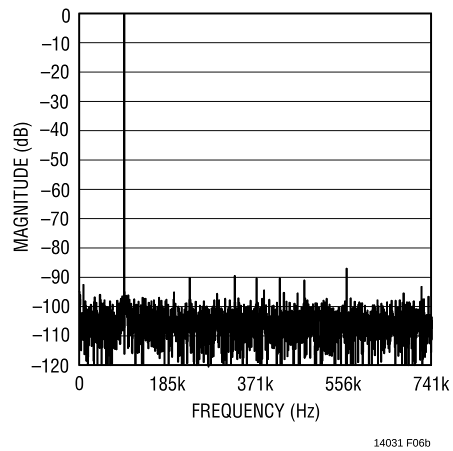

Figure 6b. LTC1407-1 6MHz Sine Wave 4096 Point FFT Plot with the LT1819 Driving the Inputs Differentially

Board Layout and Bypassing

Wire wrap boards are not recommended for high resolution and/or high speed A/D converters. To obtain the best performance from the LTC1407-1/LTC1407A-1, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. If optimum phase match between the inputs is desired, the length of the four input wires of the two input channels should be kept matched. But each pair of input wires to the two input channels should be kept separated by a ground trace to avoid high frequency crosstalk between channels.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in the Block Diagram on the first page of this data sheet. For optimum performance, a 10μF surface mount tantalum capacitor with a 0.1μF ceramic is recommended for the V_{DD} and V_{REF} pins. Alternatively, 10μF ceramic chip capacitors such as X5R or X7R may be used. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible. The V_{DD} bypass capacitor returns to GND (Pin 6) and the V_{REF} bypass capacitor returns to the Exposed Pad ground (Pin 11). Care should be taken to place the 0.1μF V_{DD} bypass capacitor as close to Pins 6 and 7 as possible.

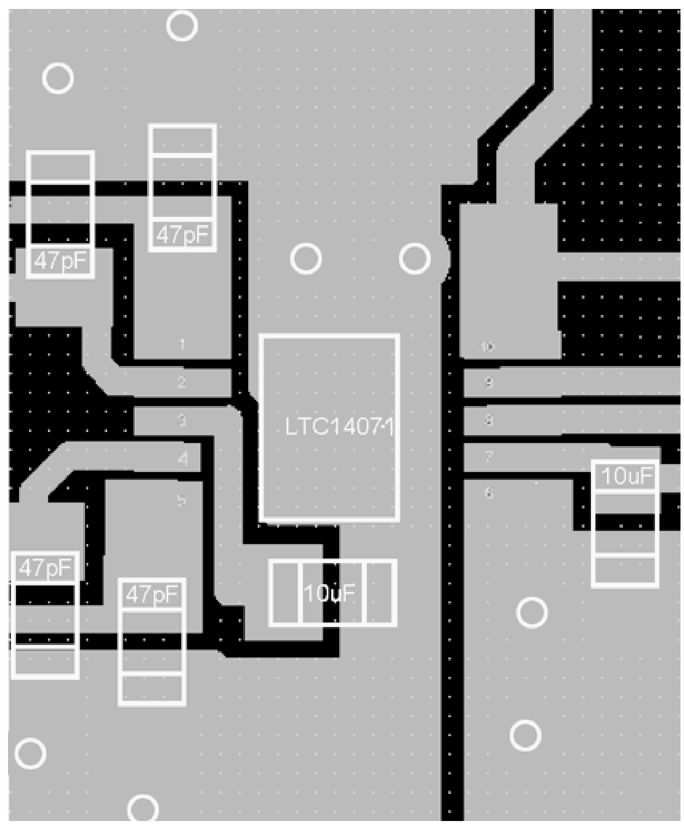

Figure 7. Recommended Layout

Figure 7 shows the recommended system ground connections. All analog circuitry grounds should be terminated at

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the LTC1407-1/LTC1407A-1 Exposed Pad. The ground return from the LTC1407-1/LTC1407A-1 Pin 6 to the power supply should be low impedance for noise-free operation. The Exposed Pad of the 10-lead MSE package is also tied to Pin 6 and the LTC1407-1/LTC1407A-1 GND. The Exposed Pad should be soldered on the PC board to reduce ground connection inductance. Digital circuitry grounds must be connected to the digital supply common.

POWER-DOWN MODES

Upon power-up, the LTC1407-1/LTC1407A-1 are initialized to the active state and is ready for conversion. The Nap and Sleep mode waveforms show the power down modes for the LTC1407-1/LTC1407A-1. The SCK and CONV inputs control the power down modes (see Timing Diagrams). Two rising edges at CONV, without any intervening rising edges at SCK, put the LTC1407-1/LTC1407A-1 in Nap mode and the power drain drops from 14mW to 6mW. The internal reference remains powered in Nap mode. One or more rising edges at SCK wake up the LTC1407-1/LTC1407A-1 for service very quickly and CONV can start an accurate conversion within a clock cycle. Four rising edges at CONV, without any intervening rising edges at SCK, put the LTC1407-1/LTC1407A-1 in Sleep mode and the power drain drops from 14mW to 10μW. One or more rising edges at SCK wake up the LTC1407-1/LTC1407A-1 for operation. The internal reference (V_{REF}) takes 2ms to slew and settle with a 10μF load. Using sleep mode more frequently compromises the settled accuracy of the internal reference. Note that for slower conversion rates, the Nap and Sleep modes can be used for substantial reductions in power consumption.

DIGITAL INTERFACE

The LTC1407-1/LTC1407A-1 have a 3-wire SPI (Serial Protocol Interface) interface. The SCK and CONV inputs and SDO output implement this interface. The SCK and CONV inputs accept swings from 3V logic and are TTL compatible, if the logic swing does not exceed V_{DD}. A detailed description of the three serial port signals follows:

Conversion Start Input (CONV)

The rising edge of CONV starts a conversion, but subsequent rising edges at CONV are ignored by the LTC1407-1/LTC1407A-1 until the following 32 SCK rising edges have occurred. The duty cycle of CONV can be arbitrarily chosen to be used as a frame sync signal for the processor serial port. A simple approach to generate CONV is to create a pulse that is one SCK wide to drive the LTC1407-1/LTC1407A-1 and then buffer this signal to drive the frame sync input of the processor serial port. It is good practice to drive the LTC1407-1/LTC1407A-1 CONV input first to avoid digital noise interference during the sample-to-hold transition triggered by CONV at the start of conversion. It is also good practice to keep the width of the low portion of the CONV signal greater than 15ns to avoid introducing glitches in the front end of the ADC just before the sample-and-hold goes into Hold mode at the rising edge of CONV.

Minimizing Jitter on the CONV Input

In high speed applications where high amplitude sinewaves above 100kHz are sampled, the CONV signal must have as little jitter as possible (10ps or less). The square wave output of a common crystal clock module usually meets this requirement easily. The challenge is to generate a CONV signal from this crystal clock without jitter corruption from other digital circuits in the system. A clock divider and any gates in the signal path from the crystal clock to the CONV input should not share the same integrated circuit with other parts of the system. As shown in the interface circuit examples, the SCK and CONV inputs should be driven first, with digital buffers used to drive the serial port interface. Also note that the master clock in the DSP may already be corrupted with jitter, even if it comes directly from the DSP crystal. Another problem with high speed processor clocks is that they often use a low cost, low speed crystal (i.e., 10MHz) to generate a fast, but jittery, phase-locked-loop system clock (i.e., 40MHz). The jitter in these PLL-generated high speed clocks can be several nanoseconds. Note that if you choose to use the frame sync signal generated by the DSP port, this signal will have the same jitter of the DSP's master clock.

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Serial Clock Input (SCK)

The rising edge of SCK advances the conversion process and also udpates each bit in the SDO data stream. After CONV rises, the third rising edge of SCK sends out two sets of 12/14 data bits, with the MSB sent first. A simple approach is to generate SCK to drive the LTC1407-1/ LTC1407A-1 first and then buffer this signal with the appropriate number of inverters to drive the serial clock input of the processor serial port. Use the falling edge of the clock to latch data from the Serial Data Output (SDO) into your processor serial port. The 14-bit Serial Data will be received right justified, in two 16-bit words with 32 or more clocks per frame sync. It is good practice to drive the LTC1407-1/LTC1407A-1 SCK input first to avoid digital noise interference during the internal bit comparison decision by the internal high speed comparator. Unlike the CONV input, the SCK input is not sensitive to jitter because the input signal is already sampled and held constant.

Serial Data Output (SDO)

Upon power-up, the SDO output is automatically reset to the high impedance state. The SDO output remains in high impedance until a new conversion is started. SDO sends out two sets of 12/14 bits in 2's complement format in the output data stream after the third rising edge of SCK after the start of conversion with the rising edge of CONV. The two 12-/14-bit words are separated by two clock cycles in high impedance mode. Please note the delay specification from SCK to a valid SDO. SDO is always guaranteed to be valid by the next rising edge of SCK. The 32-bit output data stream is compatible with the 16-bit or 32-bit serial port of most processors.

HARDWARE INTERFACE TO TMS320C54x

The LTC1407-1/LTC1407A-1 are serial output ADCs whose interface has been designed for high speed buffered serial ports in fast digital signal processors (DSPs). Figure 8 shows an example of this interface using a TMS320C54X.

The buffered serial port in the TMS320C54x has direct access to a 2kB segment of memory. The ADC's serial data can be collected in two alternating 1kB segments, in real time, at the full 3Msps conversion rate of the LTC1407-1/ LTC1407A-1. The DSP assembly code sets frame sync mode at the BFSR pin to accept an external positive going pulse and the serial clock at the BCLKR pin to accept an external positive edge clock. Buffers near the LTC1407-1/ LTC1407A-1 may be added to drive long tracks to the DSP to prevent corruption of the signal to LTC1407-1/ LTC1407A-1. This configuration is adequate to traverse a typical system board, but source resistors at the buffer outputs and termination resistors at the DSP, may be needed to match the characteristic impedance of very long transmission lines. If you need to terminate the SDO transmission line, buffer it first with one or two 74ACxx gates. The TTL threshold inputs of the DSP port respond properly to the 3V swing used with the LTC1407-1/ LTC1407A-1.

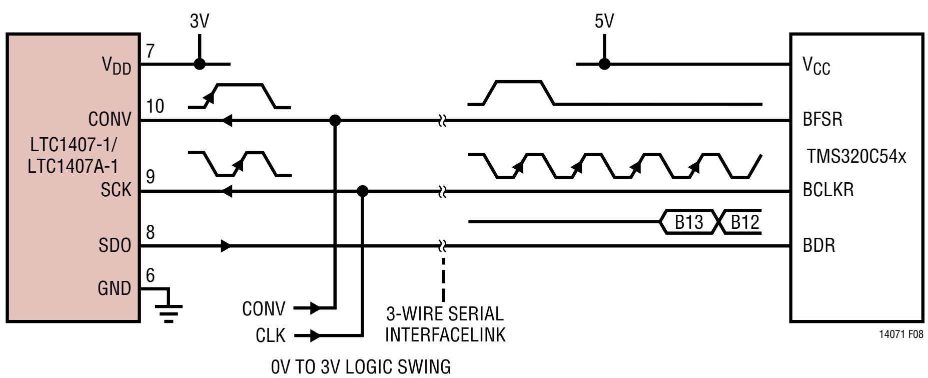

Figure 8. DSP Serial Interface to TMS320C54x

APPLICATIONS INFORMATION

```
; 12-03-03 *******************************************************************
; Files: 014SIAB.ASM ->   1407A Sine wave collection with Serial Port interface
;        bvectors.asm     both channels collected in sequence in the same 2k record.
;        s2k14ini.asm     Buffered mode 2k buffer size.
; First element at 1024, last element at 1023, two middles at 2047 and 0000
; bipolar mode
; Works 16 or 64 clock frames.
; negative edge BCLKR
; negative BFSR pulse
; -0 data shifted
; ***************************************************************************

         .width   160
         .length  110
         .title “sineb0 BSP in auto buffer mode”
         .mmregs
         .setsect “.text”,   0x500,0    ;Set address of executable
         .setsect “vectors”, 0x180,0    ;Set address of incoming 1403 data
         .setsect “buffer”,  0x800,0    ;Set address of BSP buffer for clearing
         .setsect “result”, 0x1800,0    ;Set address of result for clearing
        .text                           ;.text marks start of code

start:
                        ;this label seems necessary
                        ;Make sure /PWRDWN is low at J1-9
                        ;to turn off AC01 adc
        tim=#0fh
        prd=#0fh
        tcr = #10h      ; stop timer
        tspc = #0h      ; stop TDM serial port to AC01
        pmst = #01a0h   ; set up iptr. Processor Mode STatus register
        sp = #0700h     ; init stack pointer.
        dp = #0         ; data page
        ar2 = #1800h    ; pointer to computed receive buffer.
        ar3 = #0800h    ; pointer to Buffered Serial Port receive buffer
        ar4 = #0h       ; reset record counter
        call sineinit    ; Double clutch the initialization to insure a proper
sinepeek:
        call sineinit    ; reset. The external frame sync must occur 2.5 clocks
                        ; or more after the port comes out of reset.
wait    goto   wait


;      ————————Buffered Receive Interrupt Routine —————————

breceive:
        ifr = #10h               ; clear interrupt flags
        TC = bitf(@BSPCE,#4000h) ; check which half (bspce(bit14)) of buffer
        if (NTC) goto bufull      ; if this still the first half get next half
        bspce = #(2023h + 08000h); turn on halt for second half (bspce(bit15))
        return_enable
```

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```
;       ———————mask and shift input data ——————————————

bufull:
        b = *ar3+ << -0         ; load acc b with BSP buffer and shift right -0
        b = #07FFFh & b         ; mask out the TRISTATE bits with #03FFFh
        b = b ^ #2000h          ; invert the MSB for bipolar operation
;
        *ar2+ = data(#0bh)      ; store B to out buffer and advance AR2 pointer
        TC = (@ar2 == #02000h)  ; output buffer is 2k starting at 1800h
        if (TC) goto start      ; restart if out buffer is at 1fffh
        goto bufull

;       —————————dummy bsend return————————————
bsend   return_enable           ;this is also a dummy return to define bsend
                                ;in vector table file BVECTORS.ASM
;      ——————————— end ISR ——————————————

        .copy “c:\dskplus\1403\s2k14ini.asm”    ;initialize buffered serial port
        .space 16*32            ;clear a chunk at the end to mark the end

;======================================================================
;
;  VECTORS
;
;======================================================================
        .sect “vectors”                 ;The vectors start here
        .copy “c:\dskplus\1403\bvectors.asm”    ;get BSP vectors

        .sect “buffer”                ;Set address of BSP buffer for clearing
        .space 16*0x800
        .sect “result”                ;Set address of result for clearing
        .space 16*0x800

        .end

; ***************************************************************************
; File: BVECTORS.ASM -> Vector Table for the ‘C54x DSKplus           10.Jul.96
;                       BSP vectors and Debugger vectors
;                       TDM vectors just return
; ***************************************************************************
; The vectors in this table can be configured for processing external and
; internal software interrupts. The DSKplus debugger uses four interrupt
; vectors. These are RESET, TRAP2, INT2, and HPIINT.
;   *  DO NOT MODIFY THESE FOUR VECTORS IF YOU PLAN TO USE THE DEBUGGER  *
;
; All other vector locations are free to use. When programming always be sure
; the HPIINT bit is unmasked (IMR=200h) to allow the communications kernel and
; host PC interact. INT2 should normally be masked (IMR(bit 2) = 0) so that the
; DSP will not interrupt itself during a HINT. HINT is tied to INT2 externally.
;
;
;
```

APPLICATIONS INFORMATION

```
        .title "Vector Table"
        .mmregs

reset   goto #80h       ;00; RESET  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
nmi     return_enable   ;04; non-maskable external interrupt
        nop
        nop
        nop
trap2   goto #88h       ;08; trap2  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
        .space 52*16    ;0C-3F: vectors for software interrupts 18-30
int0    return_enable   ;40; external interrupt int0
        nop
        nop
        nop
int1    return_enable   ;44; external interrupt int1
        nop
        nop
        nop
int2    return_enable   ;48; external interrupt int2
        nop
        nop
        nop
tint    return_enable   ;4C; internal timer interrupt
        nop
        nop
        nop
brint   goto breceive   ;50; BSP receive interrupt
        nop
        nop
        nop
bxint   goto bsend      ;54; BSP transmit interrupt
        nop
        nop
        nop
trint   return_enable   ;58; TDM receive interrupt
        nop
        nop
        nop
txint   return_enable   ;5C; TDM transmit interrupt
        nop
        nop
int3    return_enable   ;60; external interrupt int3
        nop
        nop
        nop
hpiint  dgoto #0e4h     ;64; HPIint  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
```

APPLICATIONS INFORMATION

```
         .space  24*16    ;68-7F; reserved area
**********************************************************************
*       (C) COPYRIGHT TEXAS INSTRUMENTS, INC. 1996                   *
**********************************************************************
*                                                                    *
* File: s2k14ini.ASM  BSP initialization code for the 'C54x DSKplus  *
*       for use with 1407 in buffered mode                           *
*       BSPC and SPC are the same in the 'C542                       *
*       BSPCE and SPCE seem the same in the 'C542                    *
**********************************************************************
         .title "Buffered Serial Port Initialization Routine"
ON       .set 1
OFF      .set !ON
YES      .set 1
NO       .set !YES
BIT_8    .set 2
BIT_10   .set 1
BIT_12   .set 3
BIT_16   .set 0
GO       .set 0x80

**********************************************************************
* This is an example of how to initialize the Buffered Serial Port (BSP).
* The BSP is initialized to require an external CLK and FSX for
* operation. The data format is 16-bits, burst mode, with autobuffering
* enabled.
*
*******************************************************************************************
*LTC1407 timing from board with 10MHz crystal.
*
*10MHz, divided from 40MHz, forced to CLKIN by 1407 board.
*
*Horizontal scale is 25ns/chr or 100ns period at BCLKR
*
*Timing measured at DSP pins. Jxx pin labels for jumper cable.
*
*BFSR  Pin J1-20 ~~\____/~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~\____/
~~~~~~~~~~~*
*BCLKR Pin J1-14 _/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/
~\_/~\_/~*
*BDR   Pin J1-26 _—_—_—<B13-B12-B11-B10-B09-B08-B07-B06-B05-B04-B03-B02-B01-B00>—_—<B13-
B12*
*CLKIN Pin J5-09 ~~~~~\_______/~~~~~~~\_______/~~~~~~~\_______/~~~~~~~\_______/
~~~~~~~\_______/~~~~~*
*C542 read                0  B13 B12 B11 B10 B09 B08 B07 B06 B05 B04 B03 B02 B01 B00  0   0
B13 B12*
*
*
* negative edge BCLKR
* negative BFSR pulse
* no data shifted
* 1' cable from counter to CONV at DUT
```

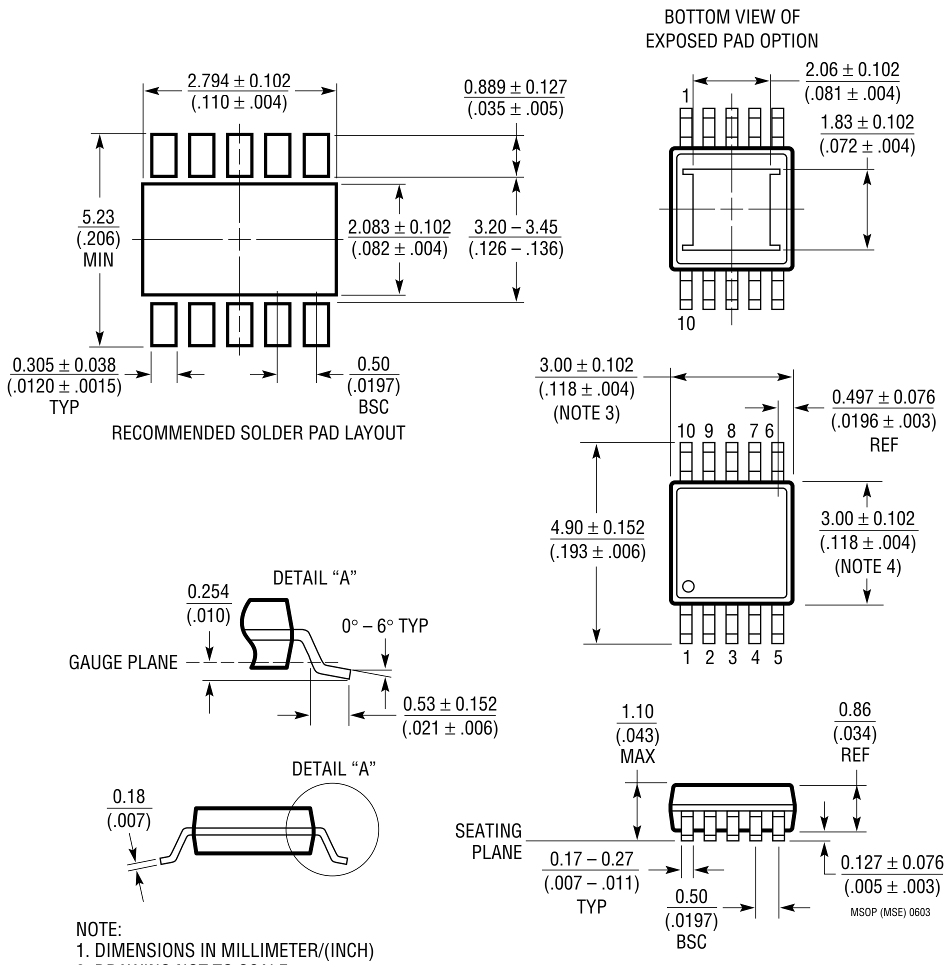
APPLICATIONS INFORMATION

```
* 2' cable from counter to CLK at DUT
*No right shift is needed to right justify the input data in the main program
*
*the two msbs should also be masked
*
*********************************************************************************************
*
Loopback        .set    NO        ;(digital looback mode?)           DLB bit
Format          .set    BIT_16    ;(Data format? 16,12,10,8)          FO bit
IntSync         .set    NO        ;(internal Frame syncs generated?)  TXM bit
IntCLK          .set    NO        ;(internal clks generated?)         MCM bit
BurstMode       .set    YES       ;(if BurstMode=NO, then Continuous) FSM bit
CLKDIV          .set    3         ;(3=default value, 1/4 CLOCKOUT)
PCM_Mode        .set    NO        ;(Turn on PCM mode?)
FS_polarity     .set    YES       ;(change polarity)YES=^^^\_/^^^, NO=___/^\___
CLK_polarity    .set    NO        ;(change polarity)for BCLKR YES=_/^, NO=~\_
Frame_ignore    .set    !YES      ;(inverted  !YES -ignores frame)
XMTautobuf      .set    NO        ;(transmit autobuffering)
RCVautobuf      .set    YES       ;(receive autobuffering)
XMThalt         .set    NO        ;(transmit buff halt if XMT buff is full)
RCVhalt         .set    NO        ;(receive buff halt if RCV buff is full)
XMTbufAddr      .set    0x800     ;(address of transmit buffer)
XMTbufSize      .set    0x000     ;(length of transmit buffer)
RCVbufAddr      .set    0x800     ;(address of receive buffer)
RCVbufSize      .set    0x800     ;(length of receive buffer)works up to 800
*
* See notes in the 'C54x CPU and Peripherals Reference Guide on setting up
* valid buffer start and length values. Page 9-44
*
*
**********************************************************************
        .eval ((Loopback >> 1)|((Format & 2)<<1)|(BurstMode <<3)|(IntCLK <<4)|(IntSync
<<5)) ,SPCval
        .eval ((CLKDIV)|(FS_polarity <<5)|(CLK_polarity<<6)|((Format &
1)<<7)|(Frame_ignore<<8)|(PCM_Mode<<9)), SPCEval
        .eval (SPCEval|(XMTautobuf<<10)|(XMThalt<<12)|(RCVautobuf<<13)|(RCVhalt<<15)),
SPCEval

sineinit:
        bspc = #SPCval          ; places buffered serial port in reset
        ifr = #10h              ; clear interrupt flags
        imr = #210h             ; Enable HPINT,enable BRINT0
        intm = 0                ; all unmasked interrupts are enabled.
        bspce = #SPCEval        ; programs BSPCE and ABU
        axr = #XMTbufAddr       ; initializes transmit buffer start address
        bkx = #XMTbufSize       ; initializes transmit buffer size
        arr = #RCVbufAddr       ; initializes receive buffer start address
        bkr = #RCVbufSize       ; initializes receive buffer size
        bspc = #(SPCval | GO)   ; bring buffered serial port out of reset
        return                  ;for transmit and receive because GO=0xC0
```

PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1663)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1608	16-Bit, 500ksps Parallel ADC	±5V Supply, ±2.5V Span, 90dB SINAD
LTC1609	16-Bit, 250ksps Serial ADC	5V Configurable Bipolar/Unipolar Inputs
LTC1403/LTC1403A	12-/14-Bit, 2.8Msps Serial ADC	3V, 15mW, Unipolar Inputs, MSOP Package
LTC1403-1/LTC1403A-1	12-/14-Bit, 2.8Msps Serial ADC	3V, 15mW, Bipolar Inputs, MSOP Package
LTC1407/LTC1407A	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V, 14mW, 2-Channel Unipolar Input Range
LTC1411	14-Bit, 2.5Msps Parallel ADC	5V, Selectable Spans, 80dB SINAD
LTC1420	12-Bit, 10Msps Parallel ADC	5V, Selectable Spans, 72dB SINAD
LTC1405	12-Bit, 5Msps Parallel ADC	5V, Selectable Spans, 115mW
LTC1412	12-Bit, 3Msps Parallel ADC	±5V Supply, ±2.5V Span, 72dB SINAD
LTC1402	12-Bit, 2.2Msps Serial ADC	5V or ±5V Supply, 4.096V or ±2.5V Span
LTC1864/LTC1865 LTC1864L/LTC1865L	16-Bit, 250ksps 1-/2-Channel Serial ADCs	5V or 3V (L-Version), Micropower, MSOP Package
DACs		
LTC1666/LTC1667 LTC1668	12-/14-/16-Bit, 50Msps DAC	87dB SFDR, 20ns Settling Time
LTC1592	16-Bit, Serial SoftSpan™ I_{OUT} DAC	±1LSB INL/DNL, Software Selectable Spans
References		
LT1790-2.5	Micropower Series Reference in SOT-23	0.05% Initial Accuracy, 10ppm Drift
LT1461-2.5	Precision Voltage Reference	0.04% Initial Accuracy, 3ppm Drift
LT1460-2.5	Micropower Series Voltage Reference	0.10% Initial Accuracy, 10ppm Drift

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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