Dual-Channel Hot Swap Controller/Power Sequencer

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Programmable Power Supply Sequencing**
- **Programmable Electronic Circuit Breaker**
- User-Programmable Supply Voltage Power-Up and Power-Down Rate
- High Side Drivers for External N-Channel FETs
- Controls Supply Voltages from 1.2V to 12V
- Ensures Proper Power-Up Behavior
- Undervoltage Lockout
- Glitch Filter Protects Against Spurious $\overline{\text{RESET}}$ Signals

APPLICATIONS

- Hot Board Insertion
- Power Supply Sequencing
- Electronic Circuit Breaker

DESCRIPTION

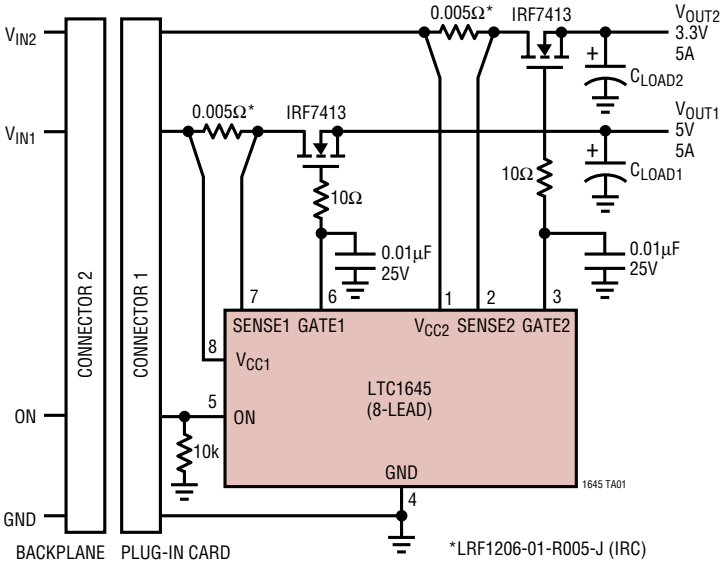
The LTC®1645 is a 2-channel Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. Using external N-channel pass transistors, the supply voltages can be ramped at a programmable rate. Two high side switch drivers control the N-channel gates for supply voltages ranging from 1.2V to 12V. The two channels can be set to ramp up and down separately, or they can be programmed to rise and fall simultaneously, ensuring power supply tracking at the two outputs.

Programmable electronic circuit breakers protect against shorts at either output. The $\overline{\text{RESET}}$ output can be used to generate a system reset when a supply voltage falls below a user-programmed voltage. An additional spare comparator is available for monitoring a second supply voltage.

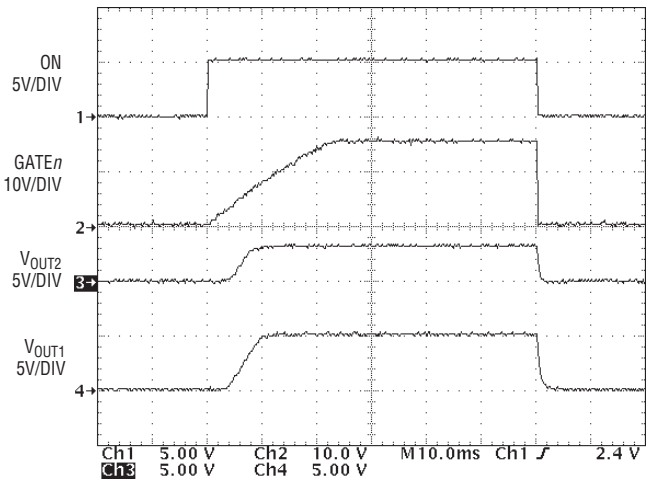
The LTC1645 is available in the 8- and 14-pin SO packages.

TYPICAL APPLICATION

5V and 3.3V Hot Swap



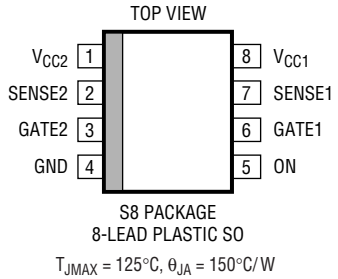
5V and 3.3V Hot Swap Waveforms



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC1}, V_{CC2}) 13.2V
Input Voltage
FB, ON, COMP+ ..... –0.3V to (V_{CC1} + 0.3V)
TIMER ..... –0.3V to 2.5V
SENSE1 ..... (V_{CC1} – 0.7V) to (V_{CC1} + 0.3V)
SENSE2 ..... (V_{CC1} – 0.7V) to (V_{CC2} + 0.3V)
Output Voltage
$\overline{RESET}$, COMPOUT, $\overline{FAULT}$ .....–0.3V to 16V
GATE1, GATE2 ..... Internally Limited (Note 3)
Output Current
GATE1, GATE2 ..... ±20mA
Operating Temperature Range
LTC1645C ..... 0°C to 70°C
LTC1645I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



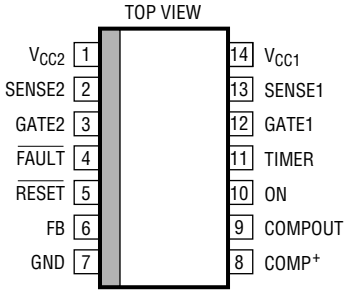
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LTC1645CS8
LTC1645IS8

S8 PART MARKING

1645
1645I



S PACKAGE
14-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1645CS
LTC1645IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.375V ≤ V_{CC1} ≤ 12V, 1.2V ≤ V_{CC2} ≤ 12V unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
I_{CC1}	V_{CC1} Supply Current	ON = V_{CC1} = 5V, V_{CC2} = 3.3V	●		1.1	2.0	mA
I_{CC2}	V_{CC2} Supply Current	ON = V_{CC1} = 5V, V_{CC2} = 3.3V	●		0.28	0.4	mA
V_{LKO1}	V_{CC1} Undervoltage Lockout	High to Low	●	2.16	2.23	2.3	V
V_{LKO2}	V_{CC2} Undervoltage Lockout	High to Low	●	1.06	1.12	1.18	V
V_{LKHn}	V_{CCn} Undervoltage Lockout Hysteresis				25		mV
V_{FB}	FB Pin Voltage Threshold	High to Low	●	1.226	1.238	1.250	V
ΔV_{FB}	FB Pin Threshold Line Regulation	High to Low, V_{CC1} = 2.375V to 12V	●		1	4	mV
V_{FBHST}	FB Pin Voltage Threshold Hysteresis				5		mV
V_{COMP}	COMP+ Pin Voltage Threshold	High to Low	●	1.226	1.238	1.250	V
ΔV_{COMP}	COMP+ Pin Threshold Line Regulation	High to Low, V_{CC1} = 2.375V to 12V	●		1	4	mV
$V_{COMPHST}$	COMP+ Pin Voltage Threshold Hysteresis				5		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.375V ≤ V_{CC1} ≤ 12V, 1.2V ≤ V_{CC2} ≤ 12V unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TM}	TIMER Pin Voltage Threshold		●	1.212	1.230	1.248	V
ΔV_{TM}	TIMER Pin Threshold Line Regulation	V_{CC1} = 2.375V to 12V	●		1	9	mV
I_{TM}	TIMER Pin Current	Timer On, V_{TIMER} = 0.6V, V_{CC1} = 5V Timer Off, V_{TIMER} = 1.5V	●	–2.3	–2 12	–1.7	µA mA
V_{CB1}	Circuit Breaker Trip Voltage 1	V_{CB1} = (V_{CC1} – V_{SENSE1})	●	46	50	56	mV
V_{CB2}	Circuit Breaker Trip Voltage 2	V_{CB2} = (V_{CC2} – V_{SENSE2})	●	46	50	56	mV
t_{CBDn}	Circuit Breaker Trip Delay	V_{CBn} = (V_{CCn} – V_{SENSEn}) > 60mV			1.5		µs
I_{CP}	GATE*n* Pin Output Current	ON = 2.2V, V_{GATEn} = V_{CCn}, V_{CC1} = 5V, V_{CC2} = 3.3V ON = 0.7V, V_{GATEn} = V_{CCn}, V_{CC1} = 5V, V_{CC2} = 3.3V ON = 0.3V, V_{GATEn} = V_{CCn}, V_{CC1} = 5V, V_{CC2} = 3.3V	● ● 	–12.5 30 	–10 40 12	–7.5 50 	µA µA mA
ΔV_{GATEn}	External N-Channel Gate Drive	ΔV_{GATEn} = (V_{GATEn} – V_{CCn})	●	4.5		16	V
V_{ONFPD}	ON Pin Fast Pull-Down Threshold	Low to High High to Low, Fast Pull-Down Engaged	● ●	0.375 0.35	0.4 0.375	0.425 0.4	V V
V_{ON1}	ON Pin Threshold #1	Low to High, GATE1 Turns On High to Low, GATE1 Turns Off	● ●	0.8 0.775	0.825 0.8	0.85 0.825	V V
V_{ON2}	ON Pin Threshold #2	Low to High, GATE2 Turns On High to Low, GATE2 Turns Off	● ●	2 1.975	2.025 2	2.050 2.025	V V
V_{ONHYST}	ON Pin Hysteresis				25		mV
I_{ON}	ON Pin Input Current	V_{CC1} = 5V, V_{CC2} = 3.3V	●		±0.01	±2	µA
V_{OL}	Output Low Voltage	$\overline{RESET}$, $\overline{FAULT}$, COMPOUT, I_{OUT} = 1.6mA, V_{CC1} = 5V	●		0.16	0.4	V

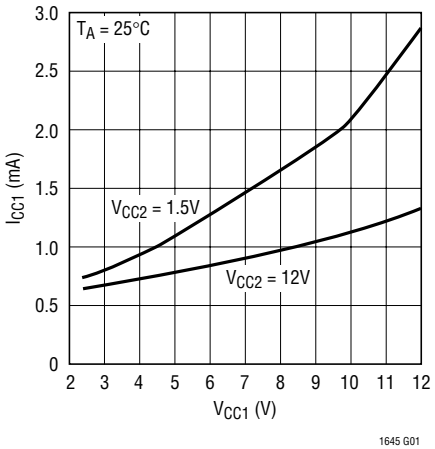
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

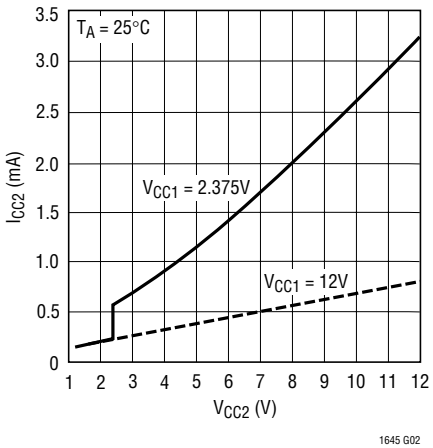
Note 3: An internal zener on the GATE*n* pins clamps the charge pump voltage to a typical maximum operating voltage of 22V. External overdrive of a GATE pin (for example, from capacitive coupling of V_{CCn} glitches) beyond the internal zener voltage may damage the device. If a lower GATE*n* pin clamp voltage is desired, use an external zener diode.

TYPICAL PERFORMANCE CHARACTERISTICS

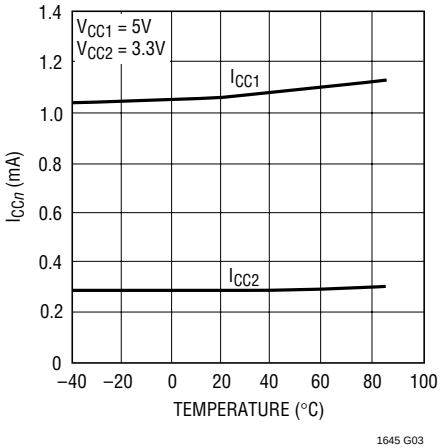
V_{CC1} Supply Current vs Voltage



V_{CC2} Supply Current vs Voltage

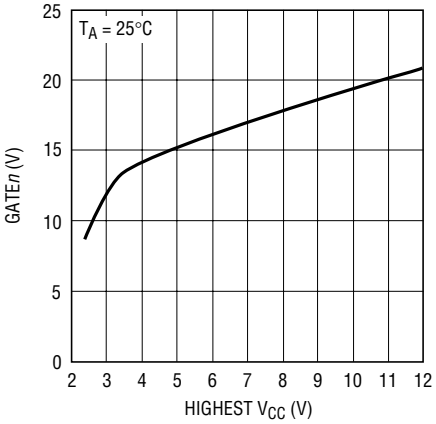


Supply Current vs Temperature

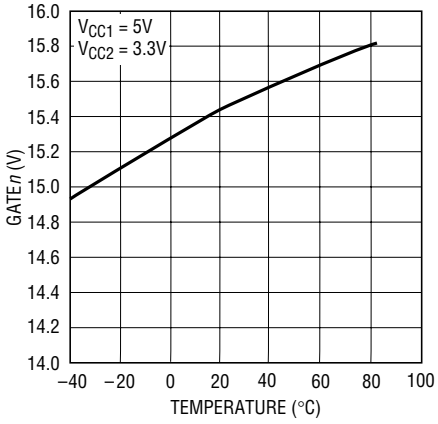


TYPICAL PERFORMANCE CHARACTERISTICS

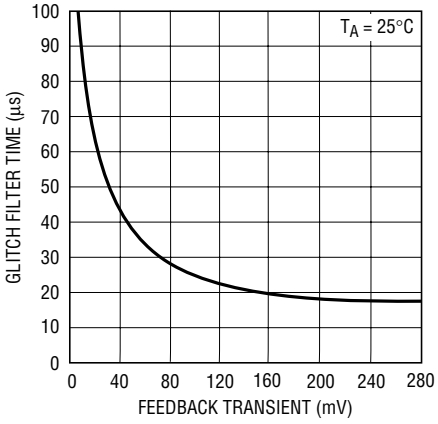
GATE Voltage vs Supply Voltage



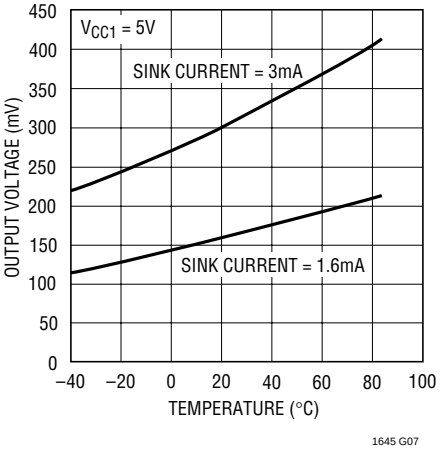
GATE Voltage vs Temperature



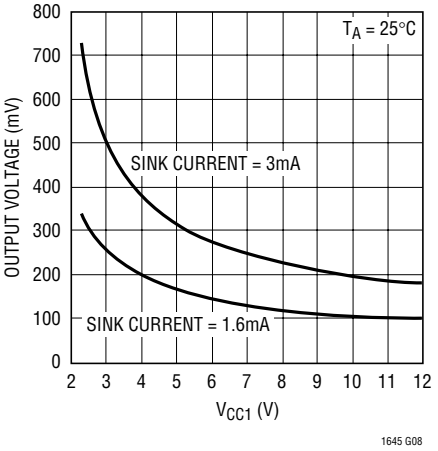
Glitch Filter Time vs Feedback Transient



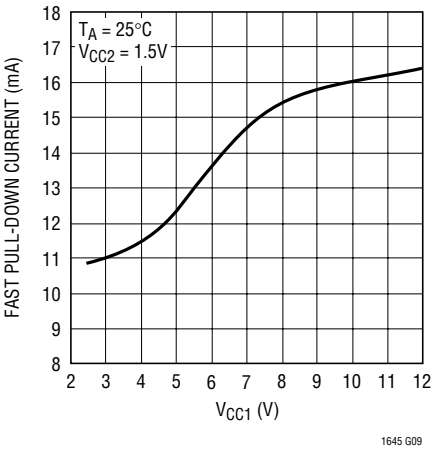
$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, COMPOUT Output Voltage vs Temperature



$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, COMPOUT Output Voltage vs V_{CC1}



Fast Pull-Down Current vs V_{CC1}



PIN FUNCTIONS (14-Lead Package/8-Lead Package)

V_{CC2} (Pin 1/Pin 1): Positive Supply Input. V_{CC2} can range from 1.2V to 12V for normal operation. I_{CC2} is typically 0.2mA. An undervoltage lockout circuit disables the LTC1645 whenever the voltage at V_{CC2} is less than 1.12V.

SENSE2 (Pin 2/Pin 2): V_{CC2} Circuit Breaker Set Pin. With a sense resistor placed in the supply path between V_{CC2} and SENSE2, the circuit breaker trips when the voltage across the resistor exceeds 50mV for more than 1.5µs. If the circuit breaker trip current is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the circuit breaker, short V_{CC2} and SENSE2 together.

GATE2 (Pin 3/Pin 3): Channel 2 High Side Gate Drive. Connect to the gate of an external N-channel MOSFET. An internal charge pump guarantees at least 4.5V of gate drive. The charge pump is powered by the higher of V_{CC1} and V_{CC2}. When the ON pin exceeds 2V, GATE2 is turned on by connecting a 10µA current source from the charge pump output to the GATE2 pin and the voltage starts to ramp up with a slope dv/dt = 10µA/C_{GATE2}. While the ON pin is below 2V but above 0.4V, a 40µA current source pulls GATE2 toward ground. If the ON pin is below 0.4V, the circuit breaker trips or the undervoltage lockout circuit trips, the GATE2 pin is immediately pulled to ground with a 12mA (typ) current source.

$\overline{\text{FAULT}}$ (Pin 4/NA): Circuit Breaker Fault. $\overline{\text{FAULT}}$ is an open-drain output that pulls low when the circuit breaker function trips. The circuit breaker is reset by pulling the ON pin below 0.4V. An external pull-up is required to generate a logic high at the $\overline{\text{FAULT}}$ pin. When the ON pin is low, $\overline{\text{FAULT}}$ will release.

The circuit breaker can be programmed to automatically reset by connecting the $\overline{\text{FAULT}}$ pin to the ON pin. In this circuit configuration, if a logic device is driving the ON pin, use a series resistor between the logic output and the ON pin to prevent large currents from flowing.

$\overline{\text{RESET}}$ (Pin 5/NA): Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ pin is pulled low when the voltage at the FB pin goes below 1.238V or V_{CC1} is below the undervoltage lockout threshold. The $\overline{\text{RESET}}$ pin goes high one timing cycle after the voltage at the FB pin goes above the FB pin threshold. The ON pin must remain above 0.8V during this timing cycle. An external pull-up is required to generate a logic high at the $\overline{\text{RESET}}$ pin.

FB (Pin 6/NA): $\overline{\text{RESET}}$ Comparator Input. The FB pin is used to monitor the output supply voltage with an external resistive divider. When the voltage on the FB pin is lower than 1.238V, the $\overline{\text{RESET}}$ pin is pulled low. A glitch filter on the FB pin prevents fast transients from forcing $\overline{\text{RESET}}$ low. When the voltage on the FB pin rises above the trip point, the $\overline{\text{RESET}}$ pin goes high after one timing cycle.

GND (Pin 7/Pin 4): Ground. Connect to a ground plane for optimum performance.

COMP^+ (Pin 8/NA): Spare Comparator Noninverting Input. When the voltage on COMP^+ is lower than 1.238V, COMPOUT pulls low.

COMPOUT (Pin 9/NA): Open-Drain Spare Comparator Output. COMPOUT pulls low when the voltage on COMP^+ is below 1.238V or V_{CC1} is below the undervoltage lockout threshold. An external pull-up is required to generate a logic high at the COMPOUT pin.

ON (Pin 10/Pin 5): Analog Control Input. If the ON pin voltage is below 0.4V, both GATE1 and GATE2 are immediately pulled to ground. While the voltage is between 0.4V and 0.8V, both GATE1 and GATE2 are each pulled to ground with a 40µA current source. While the voltage is between 0.8V and 2V, the GATE1 pull-up is turned on after one timing cycle, but GATE2 continues to be pulled to ground with a 40µA current source. When the voltage exceeds 2V, both the GATE1 and GATE2 pull-ups are turned on one timing cycle after the voltage exceeds 0.8V.

The ON pin is also used to reset the electronic circuit breaker. If the ON pin is brought below and then above 0.4V following the trip of the circuit breaker, the circuit breaker resets, and a normal power-up sequence occurs.

TIMER: (Pin 11/NA): System Timing Pin. The TIMER pin requires an external capacitor to ground to generate a timing delay. The pin is used to set the delay before the $\overline{\text{RESET}}$ pin goes high after the output supply voltage is good as sensed by the FB pin. It is also used to set the delay between the ON pin exceeding 0.8V and the GATE1 and GATE2 pins turning on (GATE2 turns on only if the ON pin exceeds 2V).

PIN FUNCTIONS (14-Lead Package/8-Lead Package)

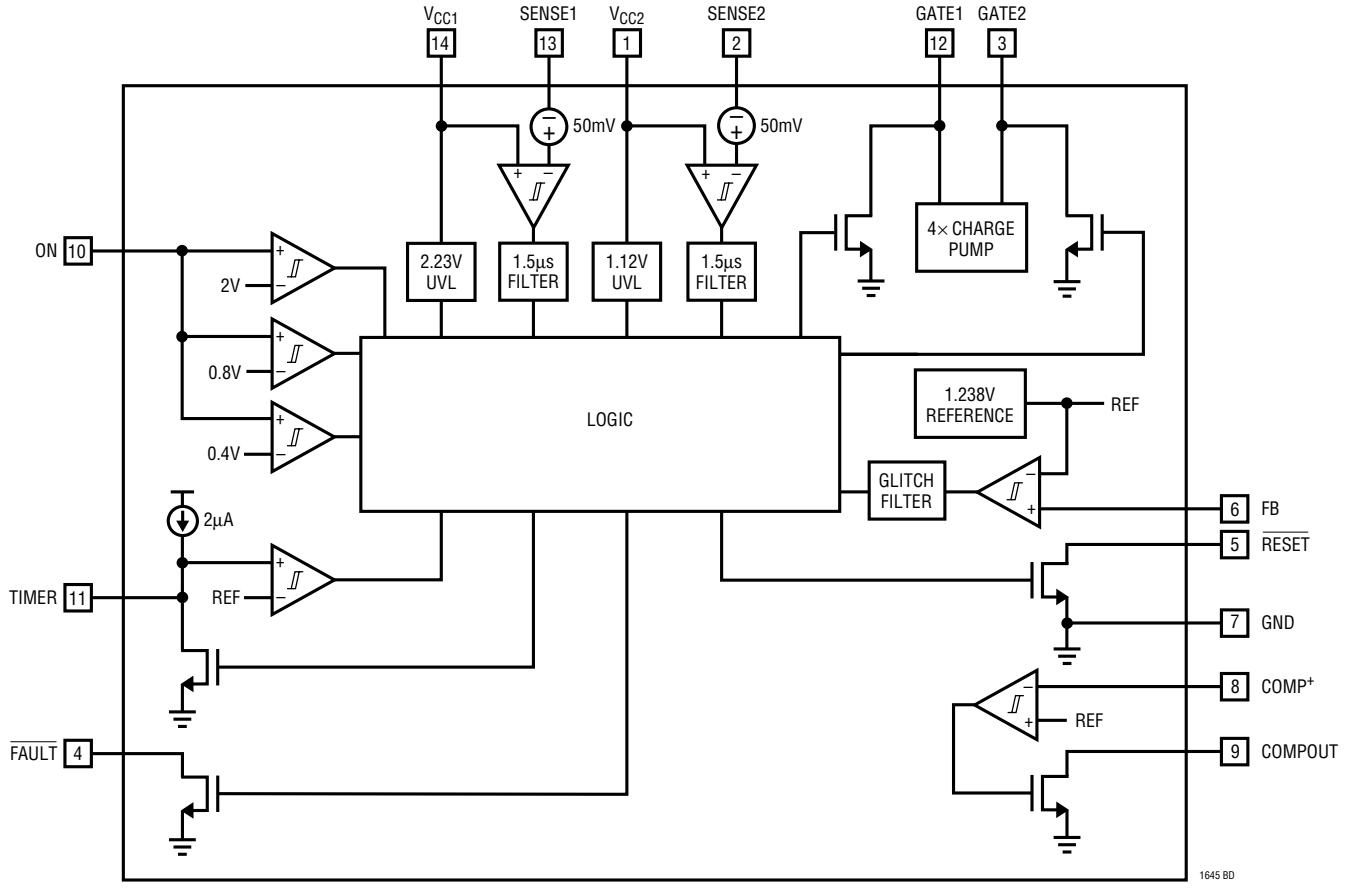
Whenever the timer is inactive, an internal N-channel FET shorts the TIMER pin to ground. Activating the timer connects a 2μA current source from V_{CC1} to the TIMER pin and the voltage starts to ramp up with a slope dv/dt = 2μA/C_{TIMER}. When the voltage reaches the trip point (1.23V), the timer is reset by pulling the TIMER pin back to ground. The timer period is (1.23V • C_{TIMER})/2μA.

GATE1 (Pin 12/Pin 6): Channel 1 High Side Gate Drive. Connect to the gate of an external N-channel MOSFET. An internal charge pump guarantees at least 4.5V of gate drive. The charge pump is powered by the higher of V_{CC1} and V_{CC2}. When the ON pin exceeds 0.8V, GATE1 is turned on by connecting a 10μA current source from the charge pump output to the GATE1 pin and the voltage starts to ramp up with a slope dv/dt = 10μA/C_{GATE1}. While the ON pin is below 0.8V but above 0.4V, a 40μA current source pulls GATE1 toward ground. If the ON pin is below 0.4V, the circuit breaker trips or the undervoltage lockout circuit trips, the GATE1 pin is immediately pulled to ground with a 12mA (typ) current source.

SENSE1 (Pin 13/Pin 7): V_{CC1} Circuit Breaker Set Pin. With a sense resistor placed in the supply path between V_{CC1} and SENSE1, the circuit breaker trips when the voltage across the resistor exceeds 50mV for more than 1.5μs. If the circuit breaker trip current is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the circuit breaker, short V_{CC1} and SENSE1 together.

V_{CC1} (Pin 14/Pin 8): Positive Supply Input. V_{CC1} can range from 2.375V to 12V for normal operation. I_{CC1} is typically 1mA. An undervoltage lockout circuit disables the chip whenever the voltage at V_{CC1} is less than 2.23V. All internal logic is powered by V_{CC1}.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When a circuit board is inserted into a live backplane, the supply bypass capacitors on the board can draw huge transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to the connector pins and produce glitches on the system supply, resetting other boards in the system.

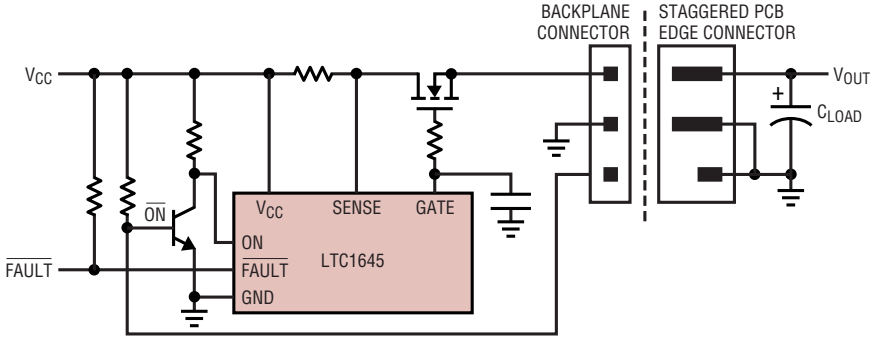
The LTC1645 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip provides a system reset signal and a spare comparator to indicate when board supply voltages drop below user-programmable voltages, and a fault signal to indicate if an overcurrent condition has occurred.

The LTC1645 can be located before or after the connector as shown in Figure 1. A staggered PCB connector can sequence pin connections when plugging and unplugging circuit boards. Alternatively, the control signal can be generated by processor control.

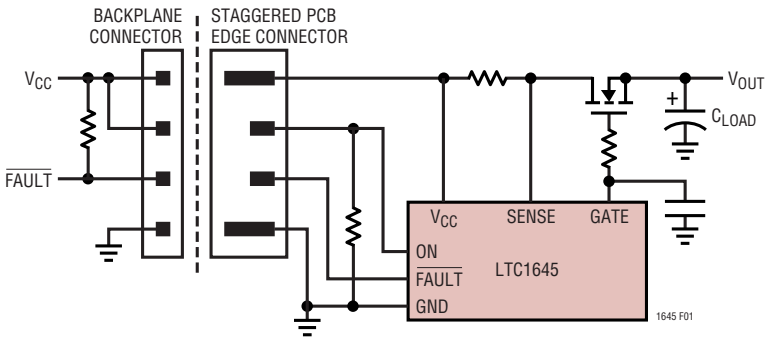
Power Supply Tracking and Sequencing

Some applications require that the potential difference between two power supplies not exceed a certain voltage. This requirement applies during power-up and power-down as well as during steady state operation, often to prevent latch-up in a dual supply ASIC. Other systems require one supply to come up after another, for example, if a system clock needs to start before a block of logic. Typical dual supplies or backplane connections may come up at arbitrary rates depending on load current, capacitor size, soft-start rates, etc. Traditional solutions are cumbersome and require complex circuitry to meet the power supply requirements.

The LTC1645 provides a simple solution to power supply tracking and sequencing needs. The LTC1645 guarantees supply tracking by ramping the supplies up and down together (see Figure 15). The sequencing capabilities of the LTC1645 allow nearly any combination of supply ramping (e.g., see Figure 17) to satisfy various sequencing specifications. See the Power Supply Tracking and Sequencing Applications section for more information.



(a) Hot Swap Controller on Motherboard



(b) Hot Swap Controller on Daughterboard

Figure 1. Staggered Pins Connection

APPLICATIONS INFORMATION

Power Supply Ramping

The power supplies on a board are controlled by placing external N-channel pass transistors in the power paths as shown in Figure 2. Consult Table 1 for a selection of N-channel FETs suitable for use with the LTC1645. R_{SENSE1} and R_{SENSE2} provide current fault detection and R1 and R2 prevent high frequency oscillation. By ramping the gates of the pass transistors up and down at a controlled rate, the transient surge current (I = C • dv/dt) drawn from the main backplane supply is limited to a safe value when the board makes connection.

When power is first applied to the chip, the gates of the N-channels (GATE1 and GATE2 pins) are pulled low. After the ON pin is held above 0.8V for at least one timing cycle, the voltage at GATE1 begins to rise with a slope equal to dv/dt = 10µA/C1 (Figure 3), where C1 is the external capacitor connected between the GATE1 pin and GND. If the ON pin is brought above 2V (and the ON pin has been held above 0.8V for at least one timing cycle), the voltage at GATE2 begins to rise with a slope equal to dv/dt = 10µA/C2.

The ramp time for each supply is t = (V_{CCn} • C*n*)/10µA. If the ON pin is pulled below 2V for GATE2 or 0.8V for GATE1 (but above 0.4V), a 40µA current source is connected from GATE*n* to GND, and the voltage at the GATE*n* pin will ramp down, as shown in Figure 4.

Ringing

Good engineering practice calls for bypassing the supply rail of any circuit. Bypass capacitors are often placed at the supply connection of every active device, in addition to one or more large value bulk bypass capacitors per supply rail. If power is connected abruptly, the bypass capacitors slow the rate of rise of voltage and heavily damp any parasitic resonance of lead or trace inductance working against the supply bypass capacitors.

The opposite is true for LTC1645 Hot Swap circuits on a daughterboard. In most cases, on the powered side of the N-channel FET switches (V_{CCn}) there is no supply bypass capacitor present. An abrupt connection, produced by plugging a board into a backplane connector, results in a fast rising edge applied to the V_{CCn} line of the LTC1645.

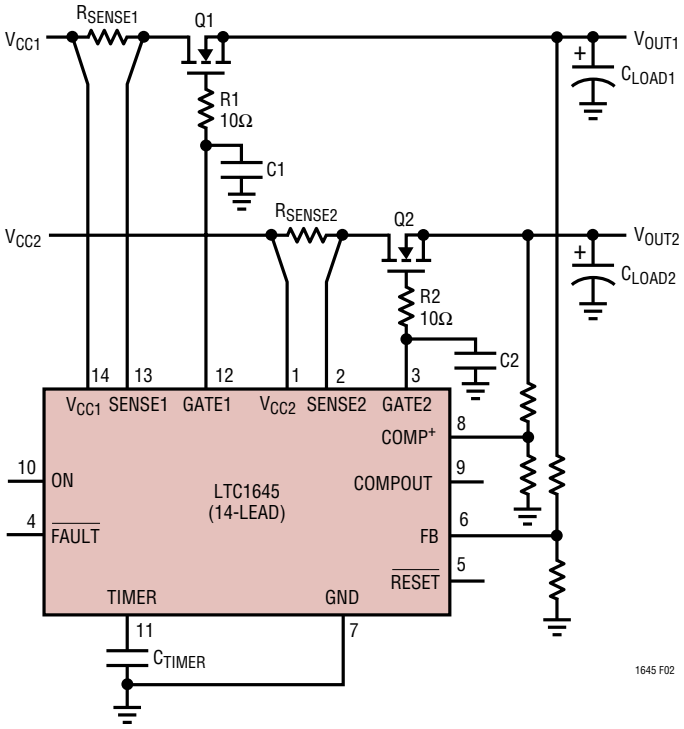


Figure 2. Typical Hot Swap Connection

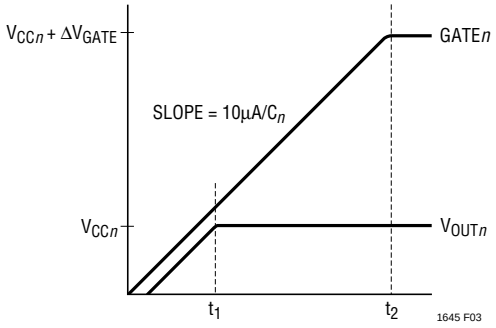


Figure 3. Supply Turning On

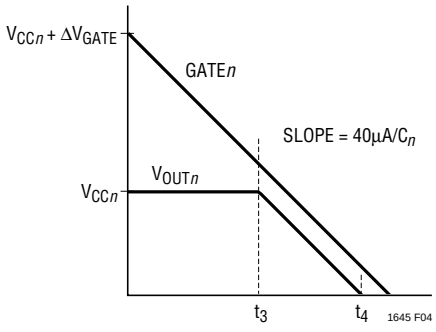


Figure 4. Supply Turning Off

APPLICATIONS INFORMATION

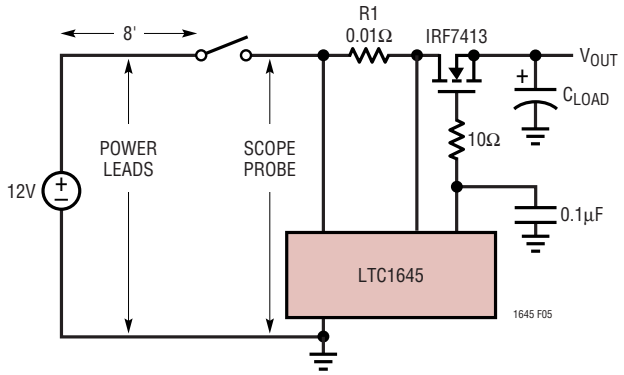
No bulk capacitance is present to slow the rate of rise and heavily damp the parasitic resonance. Instead, the fast edge shock excites a resonant circuit formed by a combination of wiring harness, backplane and circuit board parasitic inductances and FET capacitance. In theory, the peak voltage should rise to 2X the input supply, but in practice the peak can reach 2.5X, owing to the effects of voltage dependent FET capacitance.

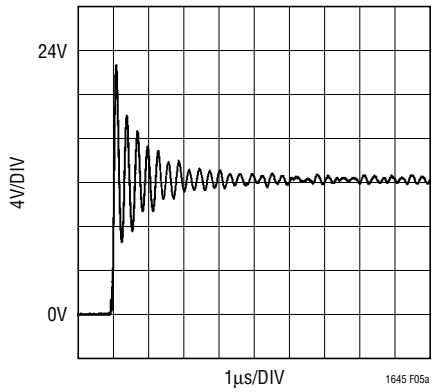
The absolute maximum V_{CC}*n* potential for the LTC1645 is 13.2V; any circuit with an input of 5V or greater should be scrutinized for ringing. A well-bypassed backplane should not escape suspicion: circuit board trace inductances of as little as 10nH can produce sufficient ringing to overvoltage V_{CC}.

Check ringing with a fast storage oscilloscope (such as a LECROY 9314AL DSO) by attaching coax or a probe to V_{CC} and GND, then repeatedly inserting the circuit board into the backplane. Figures 5a and 5b show typical results in a 12V application with different V_{CC} lead lengths. The peak amplitude reaches 22V, breaking down the ESD protection diode in the process.

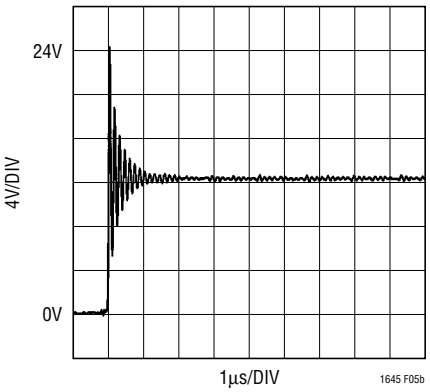
There are two methods for eliminating ringing: clipping and snubbing. A transient voltage suppressor is an effective means of limiting peak voltage to a safe level. Figure 6 shows the effect of adding an ON Semiconductor, 1SMA12CAT3, on the waveform of Figure 5.

Figures 7a and 7b show the effects of snubbing with different RC networks. The capacitor value is chosen as 10X to 100X the FET C_{OSS} under bias and R is selected for best damping—1Ω to 50Ω depending on the value of parasitic inductance.





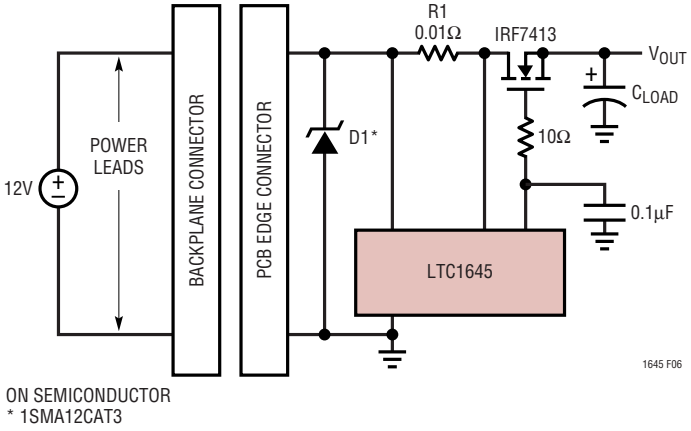
(a) Undamped V_{CC} Waveform (48" Leads)

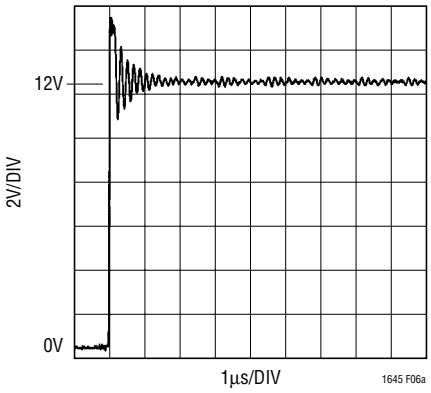


(b) Undamped V_{CC} Waveform (8" Leads)

Figure 5. Ring Experiment

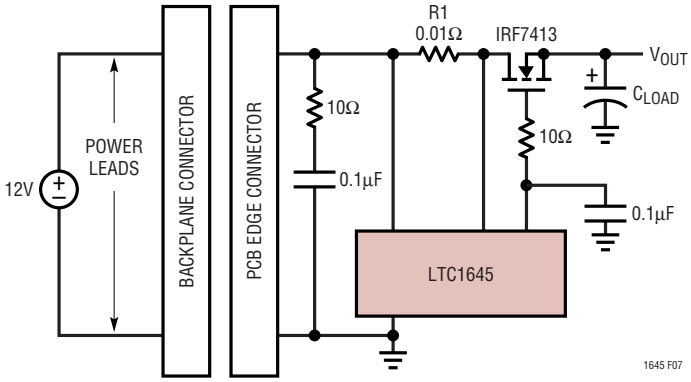
APPLICATIONS INFORMATION

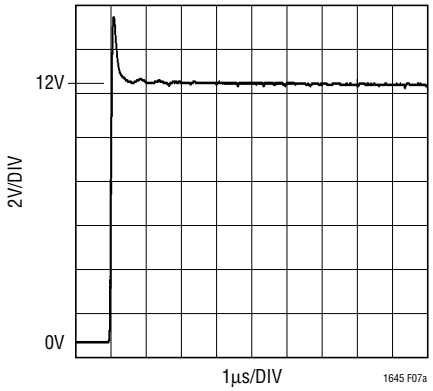




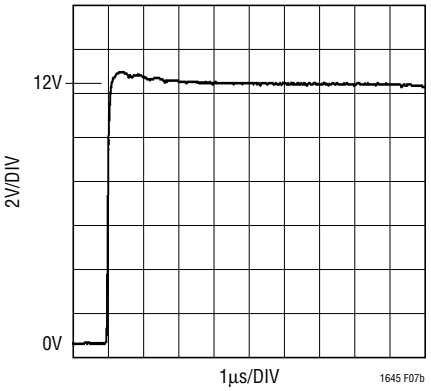
V_{CC} Waveform Clamped by a Transient Suppressor

Figure 6. Transient Suppressor Clamp





(a) V_{CC} Waveform Damped by a Snubber (15Ω, 6.8nF)



(b) V_{CC} Waveform Damped by a Snubber (10Ω, 0.1µF)

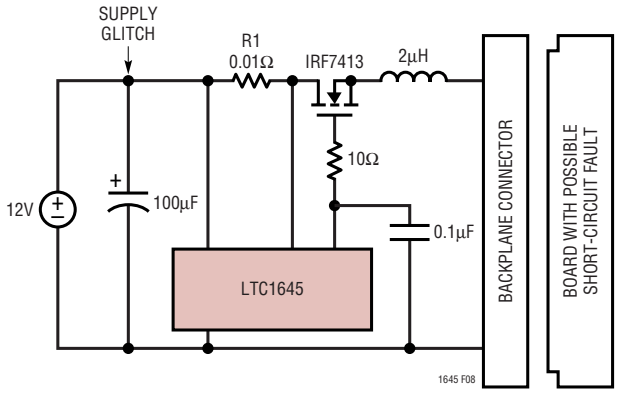
Figure 7. Snubber "Fixes"

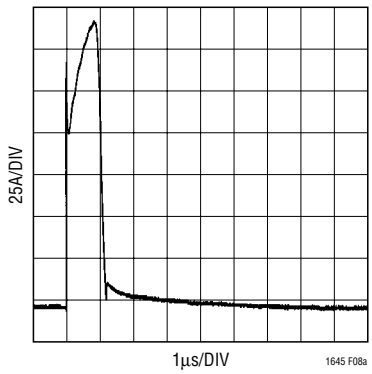
APPLICATIONS INFORMATION

Supply Glitching

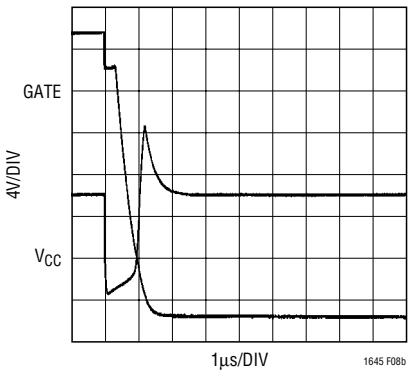
LTC1645 Hot Swap circuits on the backplane are generally used to provide power-up/down sequence at insertion/removal as well as overload/short-circuit protection. If a short-circuit occurs at supply ramp-up, the circuit breaker trips. The partially enhanced FET is easily disconnected without any supply glitch.

If a dead short occurs after a supply connection is made (Figure 8), the sense resistor R1 and the $R_{DS(ON)}$ of the fully enhanced FET provide a low impedance path for

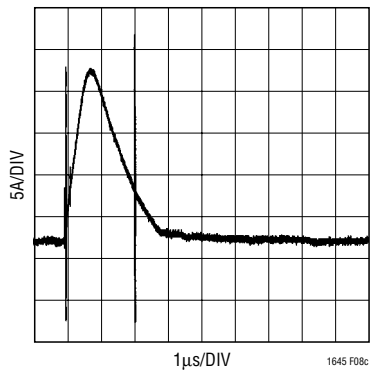




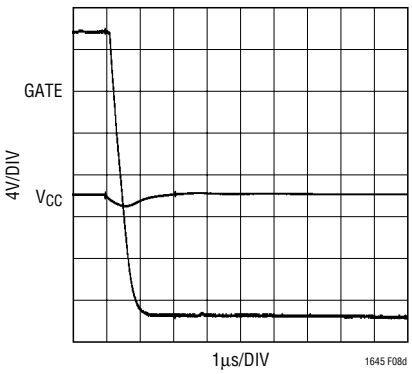
(a) V_{CC} Short-Circuit Supply Current Glitch Without Any Limiting



(b) V_{CC} Supply Glitch Without Any Limiting



(c) V_{CC} Short-Circuit Supply Current Glitch with 2µH Series Inductor



(d) V_{CC} Supply Glitch with 2µH Series Inductor

Figure 8. Supply Glitch

APPLICATIONS INFORMATION

nearly unlimited current flow. The LTC1645 discharges the GATE pin in a few microseconds, but during this discharge time current on the order of 150 amperes flows from the V_{CC} power supply. This current spike glitches the power supply, causing V_{CC} to dip (Figure 8a and 8b).

On recovery from overload, some supplies may overshoot. Other devices attached to this supply may reset or malfunction and the overshoot may also damage some components. An inductor (1μH to 10μH) in series with the FET's source limits the short-circuit di/dt, thereby limiting the peak current and the supply glitch (Figure 8c and 8d). Additional power supply bypass capacitance also reduces the magnitude of the V_{CC} glitch.

Reset

The LTC1645 uses an internal 1.238V bandgap reference, a precision voltage comparator, and a resistive divider to monitor the output supply voltage (Figure 9).

Whenever the voltage at the FB pin rises above its reset threshold (1.238V), the comparator output goes high, and a timing cycle starts (see Figure 10, time points 1 and 4). After a complete timing cycle, $\overline{\text{RESET}}$ is released. An external pull-up is required for the $\overline{\text{RESET}}$ pin to rise to a logic high.

When the voltage at the FB pin drops below its reset threshold, the comparator output goes low. After passing through a glitch filter, $\overline{\text{RESET}}$ is pulled low (time point 2). If the FB pin rises above the reset threshold for less than a timing cycle, the $\overline{\text{RESET}}$ output remains low (time point 3).

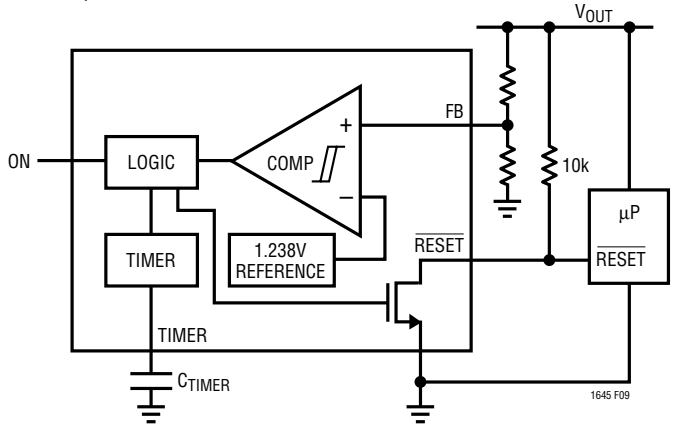


Figure 9. Supply Monitor Block Diagram

Glitch Filter

The LTC1645 has a glitch filter to prevent $\overline{\text{RESET}}$ from generating a spurious system reset in the presence of transients on the FB pin. The filter is 20μs for large transients (greater than 150mV) and up to 80μs for smaller transients. The relationship between glitch filter time and the transient voltage is shown in Typical Performance Characteristics: Glitch Filter Time vs Feedback Transient.

Timer

The system timing for the LTC1645 is generated by the circuitry shown in Figure 11. The timer is used to set the turn-on delay after the ON pin goes high. It also sets the delay before the $\overline{\text{RESET}}$ pin goes high after the FB pin exceeds 1.238V.

Whenever the timer is off, the internal N-channel shorts the TIMER pin to ground (Figure 11). Activating the timer connects a 2μA current from V_{CC1} to the TIMER pin and the

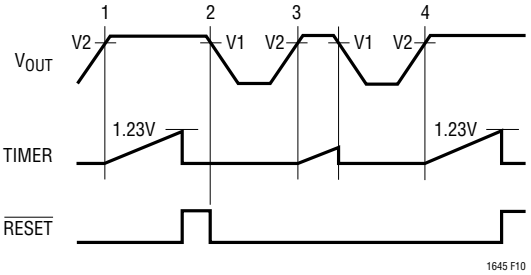


Figure 10. Supply Monitor Waveforms

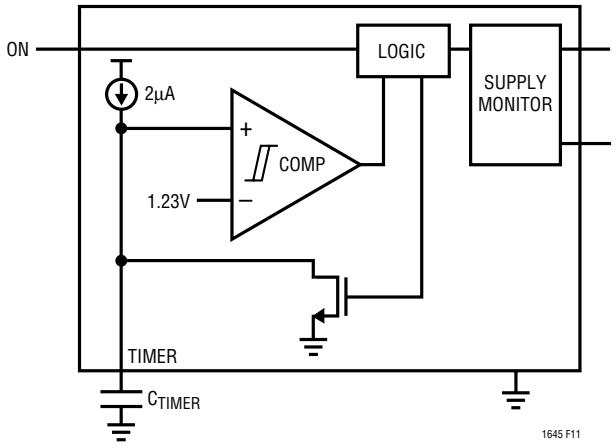


Figure 11. System Timing Block Diagram

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voltage on the external capacitor C_{TIMER} starts to ramp up with a slope dv/dt = 2µA/C_{TIMER}. When the voltage reaches the trip point (1.23V), the timer is reset by pulling the TIMER pin back to ground. The timer period is t = (1.23V • C_{TIMER})/2µA. For a 200ms delay, use a 0.33µF capacitor.

Electronic Circuit Breaker

The LTC1645 features an electronic circuit breaker function that protects against short circuits or excessive output currents. By placing sense resistors between the supply inputs and sense pins of the supplies, the circuit breaker trips whenever the voltage across either sense resistor is greater than 50mV for more than 1.5µs. If the circuit breaker trips, both GATE pins are immediately pulled to ground and the external N-channels FETs are quickly turned off (time point 6 in Figure 12). The circuit breaker resets and another timing cycle starts by taking the ON pin below 0.4V and then high as shown at time point 7.

At the end of the timer cycle (time point 8), the charge pump turns on again. If the circuit breaker feature is not required, short the SENSE*n* pin to V_{CCn}.

If the 1.5µs response time is too fast to reject supply noise, add external resistors and capacitors R_F and C_F to the sense circuit as shown in Figure 13.

The ON Pin

The ON pin is used to control system operation as shown in Figure 14. At time point 1, the board makes connection and the supplies power up the chip. At time point 2, the ON pin goes high and a timer cycle starts as long as both V_{CC} pins are higher than the undervoltage lockout trip point (2.23V for V_{CC1} and 1.12V for V_{CC2}) and an overcurrent fault is not detected. At the end of the timer cycle (time point 3), the charge pump is turned on and the GATE*n* pin voltages start to ramp up with the output supply voltages, V_{OUTn}, following one gate-to-source voltage drop lower. At time point 4, V_{OUT2} reaches its power-good trip level (this example assumes the FB pin resistive divider is connected to V_{OUT2}) and a timing cycle starts. At the end of the timing cycle (time point 5), $\overline{RESET}$ goes high and the power-up process is complete.

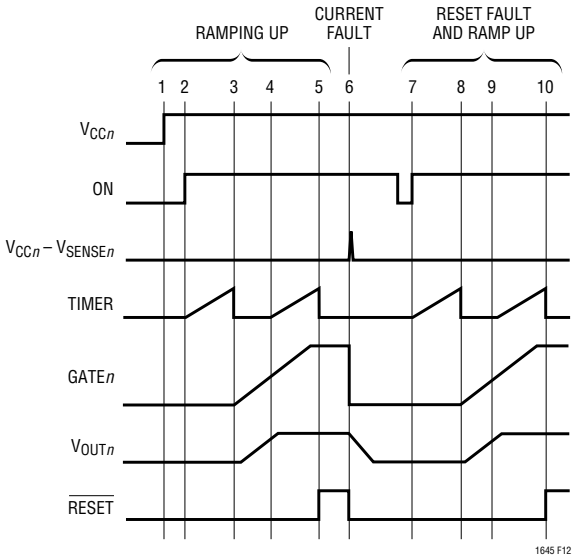

Figure 12. Current Fault Timing

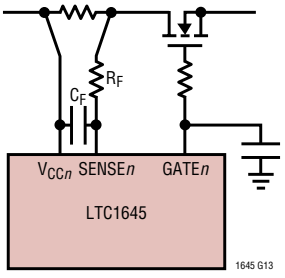

Figure 13. Extending the Short-Circuit Protection Delay

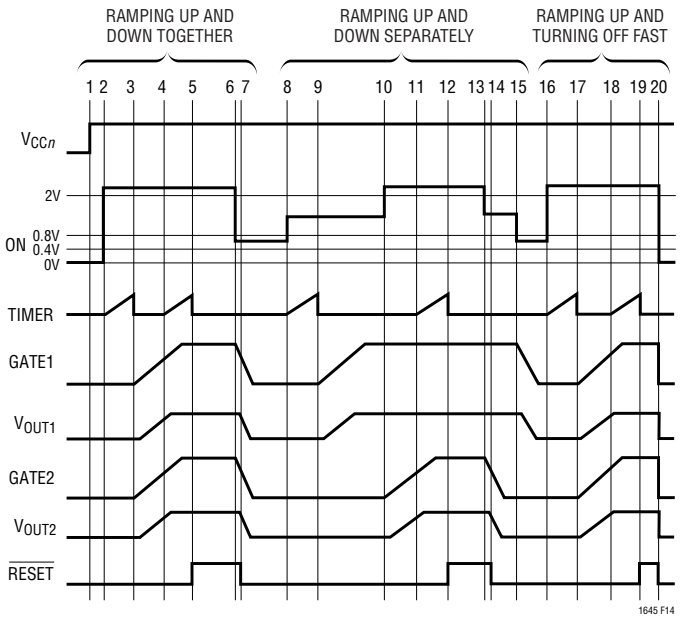

Figure 14. ON Pin Waveforms

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An external hard reset is initiated at time point 6. The ON pin is forced below 0.8V but above 0.4V, and the GATE*n* pin voltages start to ramp down. V_{OUTn} also starts to ramp down, and $\overline{RESET}$ goes low when V_{OUT2} drops below the power-good trip level at time point 7.

Time points 8 to 15 are similar to time points 1 to 7, except the ON pin's different voltage thresholds are used to ramp V_{OUT1} and V_{OUT2} separately. At time point 8, the ON pin goes above 0.8V but below 2V, and one timing cycle later (time point 9) GATE1 begins to ramp up with V_{OUT1} following one gate-to-source voltage drop lower. At time point 10, the ON pin goes above 2V and GATE2 immediately begins ramping up with V_{OUT2} following one gate-to-source voltage drop lower. As soon as V_{OUT2} reaches its power-good trip level at time point 11, a timing cycle starts. At the end of the timing cycle (time point 12), $\overline{RESET}$ goes high and the power-up process is complete.

The ON pin is forced below 2V but above 0.8V at time point 13 and the GATE2 pin voltage starts to ramp down. V_{OUT2} also starts to ramp down and $\overline{RESET}$ goes low when V_{OUT2} drops below the power-good trip level at time point 14. When the ON pin goes below 0.8V but above 0.4V at time point 15, GATE1 and V_{OUT1} ramp down.

Time points 16 to 19 show the same power-up sequence as time points 2 to 5, while time point 20 demonstrates the GATE*n* pins being pulled immediately to ground (instead of ramping down) by the ON pin going below 0.4V.

Power Supply Tracking and Sequencing Applications

The LTC1645 is able to sequence V_{OUTn} in a number of ways, including ramping V_{OUT1} up first and down last; ramping V_{OUT1} up first and down first; ramping V_{OUT1} up first and V_{OUT1} and V_{OUT2} down together; and ramping V_{OUT1} and V_{OUT2} up and down together.

Figure 15 shows an application ramping V_{OUT1} and V_{OUT2} up and down together. The ON pin must reach 0.8V to ramp up V_{OUT1} and V_{OUT2}. The spare comparator pulls the ON pin low until V_{CC2} is above 2.3V, and the ON pin cannot reach 0.8V before V_{CC1} is above 3V. Thus, both input supplies must be within regulation before a timing cycle can start. At the end of the timing cycle, the output voltages ramp up together. If either input supply falls out of regulation, the gates of Q1 and Q2 are pulled low together. Figure 16 shows an oscilloscope photo of the circuit in Figure 15.

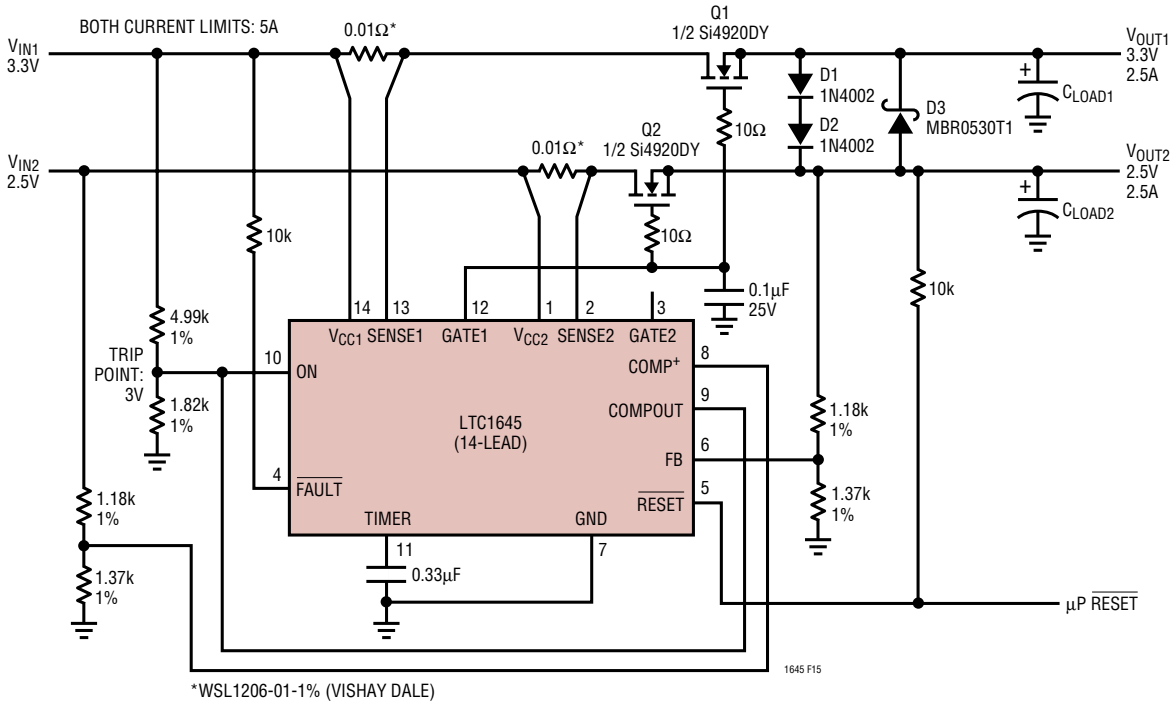

Figure 15. Ramping 3.3V and 2.5V Up and Down Together

APPLICATIONS INFORMATION

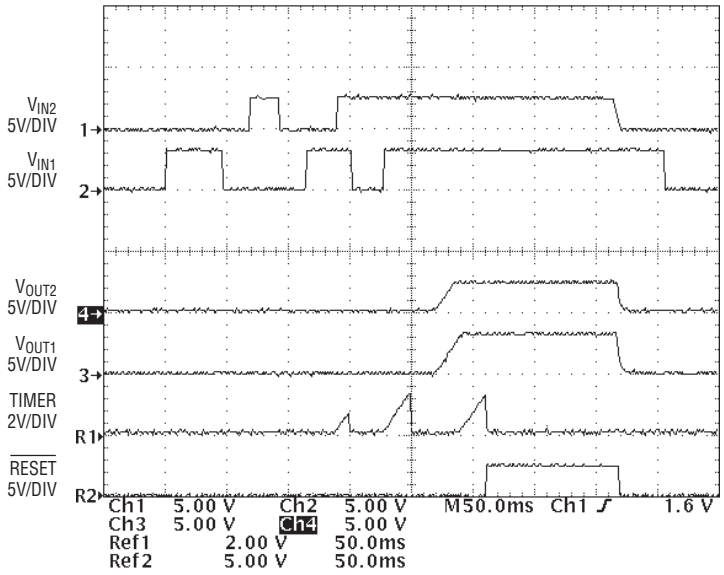

Figure 16. Ramping 3.3V and 2.5V Up and Down Together

This circuit guarantees that: (1) V_{OUT1} never exceeds V_{OUT2} by more than 1.2V, and (2) V_{OUT2} is never greater than V_{OUT1} by more than 0.4V. On power-up, V_{OUT1} and V_{OUT2} ramp up together. On power-down, the LTC1645 turns off Q1 and Q2 simultaneously. Charge remains stored on C_{LOAD1} and C_{LOAD2} and the output voltages will vary depending on the loads. D1 and D2 turn on at ≈1V (≈0.5V each), ensuring condition 1 is satisfied, while D3 prevents violations of condition 2. Different diodes may be necessary for different output voltage configurations. Barring an overvoltage condition at the input(s), the only time these diodes might conduct current is during a power-down event, and then only to discharge C_{LOAD1} or C_{LOAD2}. In the case of an input overvoltage condition that causes excess current to flow, the circuit breaker will trip if the current limit level is set appropriately.

Figure 17 shows an application circuit where V_{OUT1} ramps up before V_{OUT2}. V_{OUT1} is initially discharged and D1 is reverse-biased, thus the voltage at the ON pin is determined only by V_{CC1} through the resistor divider R1 and R2. The voltage at the ON pin exceeds 0.8V if V_{CC1} is above 4.6V and V_{OUT1} begins to ramp up after a timing cycle. As V_{OUT1} ramps up, D1 becomes forward-biased and pulls the ON pin above 2V when V_{OUT1} ≈ 4.5V. This turns on GATE2 and V_{OUT2} ramps up. The FB comparator monitors V_{OUT2}, and the spare comparator monitors V_{OUT1} with R_{HYST} creating ≈50mV of hysteresis.

Power Supply Multiplexer

Using back-to-back FETs, the LTC1645 can Hot Swap two supplies to the same output, automatically selecting the primary supply if present or the secondary supply if the primary supply is not available. Referring to Figure 18, a diode-or circuit provides power to the LTC1645 if either supply is up. Schottky diodes are used to prevent the voltage at V_{CC1} from approaching the undervoltage lockout threshold. This application assumes that if a supply is not present, the supply input is floating.

If only the 3.3V supply is present, the voltage at the $COMP^+$ pin is below the trip point and COMPOUT pulls the base of Q3 low, allowing the GATE1 pin to ramp up normally. The voltage at the ON pin exceeds 0.8V if the 3.3V supply is greater than 3V, ramping up GATE1 and turning on Q1A and Q1B. The ON pin does not exceed 2V (unless the 3.3V supply exceeds 7.5V!), keeping GATE2 low and Q2A and Q2B off.

If only the 5V supply is present or if both supplies are present, the $COMP^+$ pin is above 1.238V and COMPOUT allows the base of Q3 to be pulled high by R2. This turns Q3 on, keeping GATE1 low and Q1A and Q1B off. The voltage at the ON pin is pulled above 2V by R1 and GATE2 turns Q2A and Q2B on.

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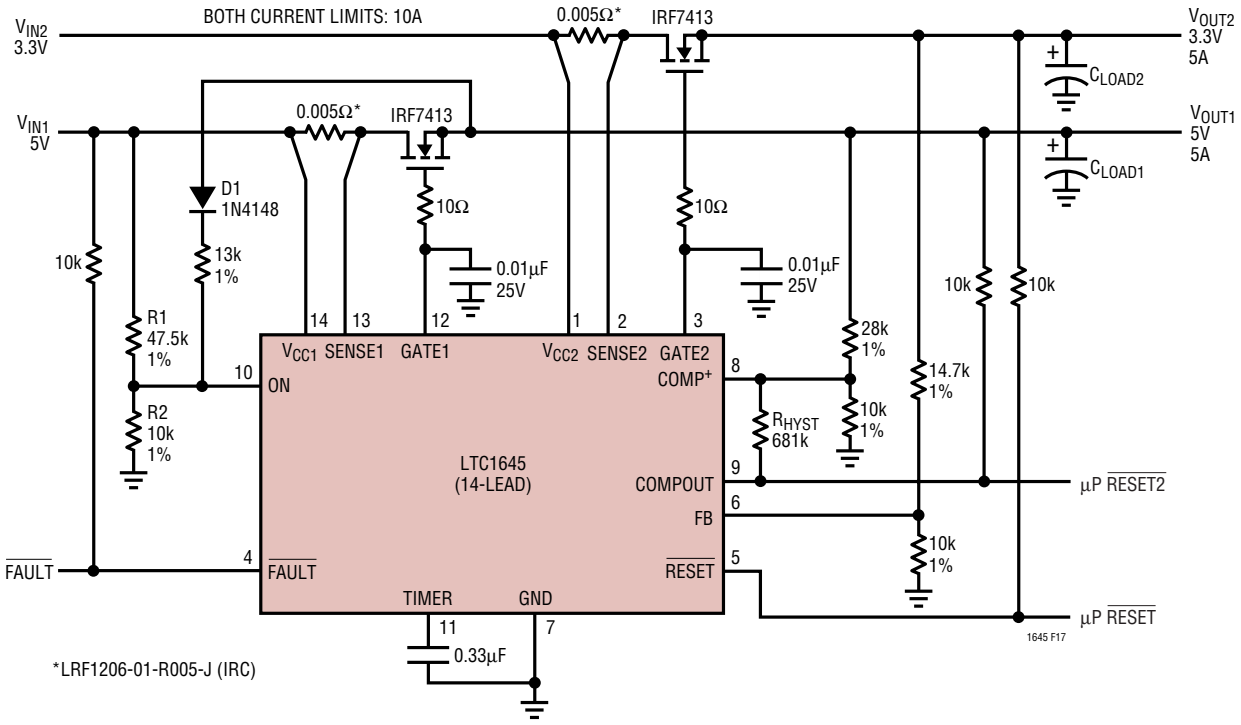

Figure 17. Ramping Up 5V Followed by 3.3V

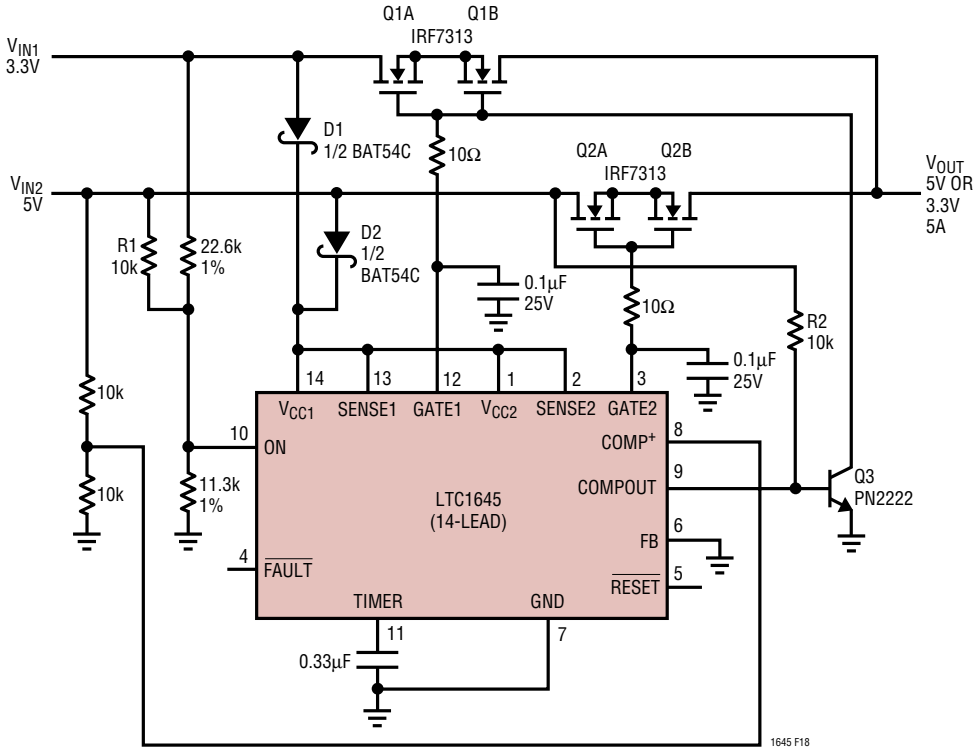

Figure 18. Power Supply Multiplexer

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Using the LTC1645 as a Linear Regulator

This application uses the LTC1645 to Hot Swap one primary supply and generate a secondary low dropout regulated supply. Figure 19 shows how to switch a 5V supply and create a 3.3V supply using the spare comparator and one additional transistor. The COMP+ pin is used to monitor the 3.3V output. As the voltage on the gate of Q2 increases, the 3.3V output increases. At the 3.3V threshold the spare comparator trips. The COMPOUT pin goes high which turns on Q3. This lowers the voltage on the gate of Q2. This feedback loop is compensated by capacitors C1 and C2 and resistor R1. When power is first applied, the FB pin is low and $\overline{\text{RESET}}$ holds one side of C2 low, slowing the ramp-up of V_{OUT2}. As V_{OUT2} exceeds 2.75V, $\overline{\text{RESET}}$ releases to allow improved loop transient response. Figure 20 shows the load transient response and voltage ripple of the generated supply.

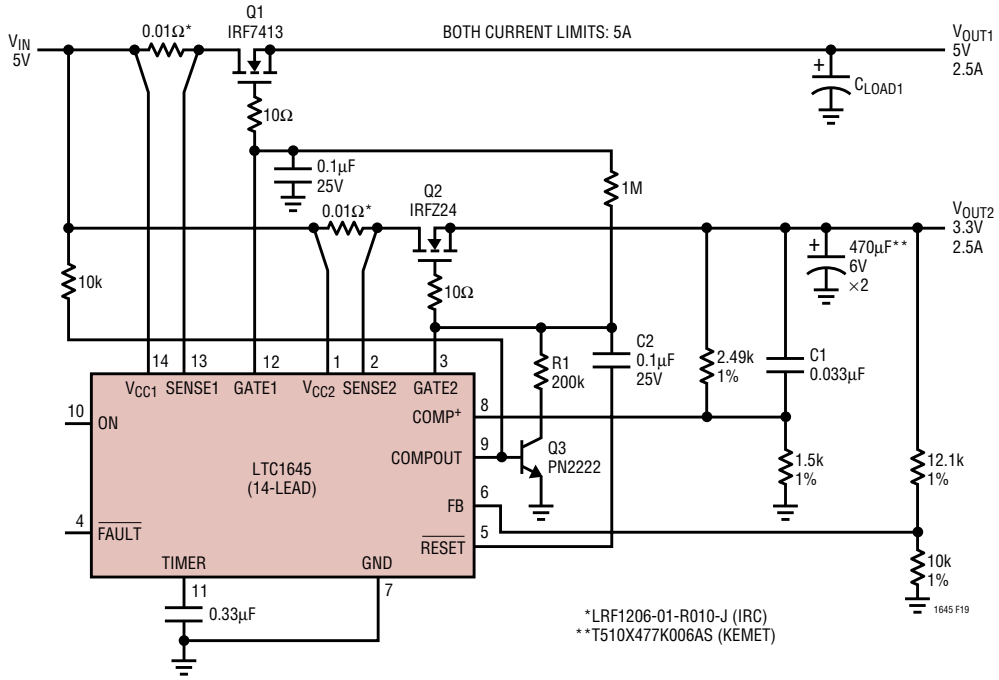

Figure 19. Switching 5V and Generating 3.3V

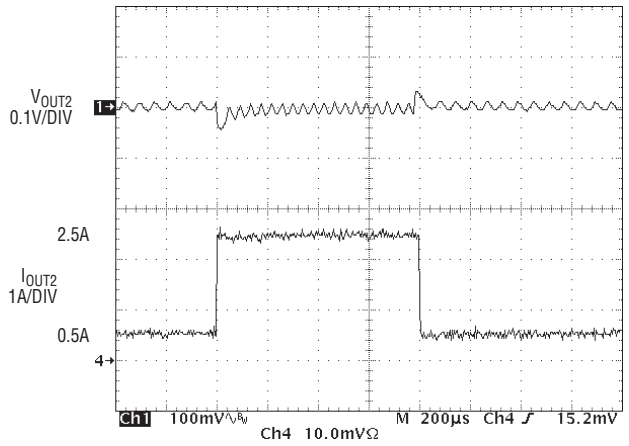

Figure 20. Load Transient Response and Voltage Ripple

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Switching Regulator Supply Sequencing

Figure 21 shows the LTC1645 sequencing two power supplies, the lower of which is generated by the LTC1430A switching regulator. Connecting the regulator's FB pin resistor divider (R1 and R2) to the other side of the pass FET (Q1) allows the LTC1430A to compensate for the voltage drop across R_{SENSE1} and Q1, assuring an accurate voltage output. The spare comparator holds the LTC1645's ON pin low until the LTC1430A's output is at least 3V, and shuts both channels off if it drops below 3V. When the ON/OFF signal is taken high to 5V (turn-on), the voltage at the ON pin rises with an RC exponential characteristic, reaching 0.8V first. This starts a timing cycle, and GATE1 begins to rise. GATE2 starts to ramp up after the ON pin reaches 2V. As long as the timing cycle is shorter than the time for the ON pin to rise from 0.8V to 2V, V_{OUT2} ramps up after V_{OUT1}. $\overline{RESET}$ goes high one timing cycle after V_{OUT1} exceeds 3V. When the ON/OFF signal is brought low, the voltage at the ON pin exponentially decays and GATE2 ramps down before GATE1. $\overline{RESET}$ goes low as soon as V_{OUT1} falls below 3V. Figure 22 shows the power-up and power-down sequences of the circuit in Figure 21.

Switching Regulator Hot Swapping

High current switching regulators usually require large bypass capacitors on both input and output for proper operation. The application in Figure 23 controls the inrush current to the LTC1649's input bypass capacitors and ramps the two output voltages up and down together. As with the previous application, connecting the regulator's FB pin resistor divider to the other side of the output pass FET (Q2) allows the LTC1649 to compensate for the voltage drop across Q2, assuring an accurate voltage output. The voltage at the LTC1645's ON pin reaches 0.8V when V_{IN} exceeds 3V, and GATE1 begins to ramp up one timing cycle later. As the regulator's output rises, D2 pulls the ON pin above 2V and GATE2 begins to rise, ramping V_{OUT1} and V_{OUT2} up together. $\overline{RESET}$ goes high one timing cycle after V_{OUT1} exceeds 3V and V_{OUT2} exceeds 2.35V. Figure 24 shows the circuit in Figure 23 powering up.

Care should be taken connecting a switching regulator's FB or SENSE pins to a node other than its output. Depending on the regulator's internal architecture, unusual behavior may occur as it tries in vain to raise the voltage at

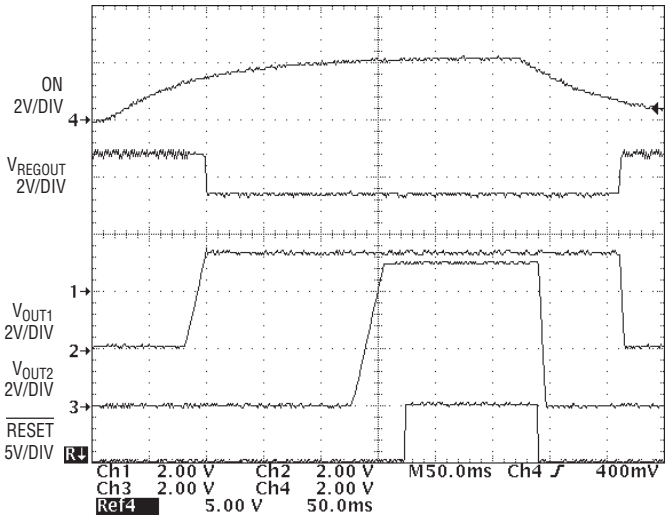


Figure 22. Switching Regulator Supply Sequencing

APPLICATIONS INFORMATION

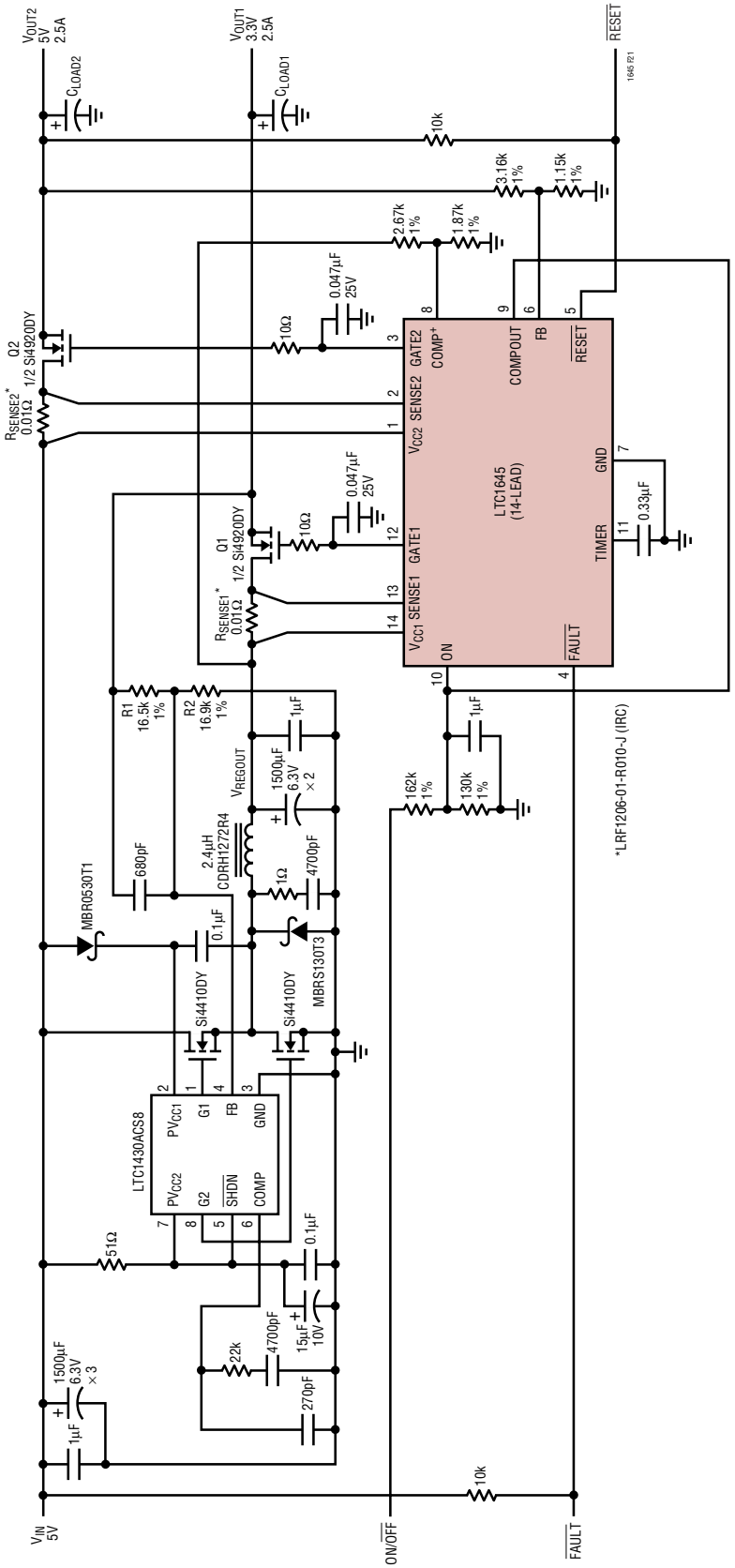


Figure 21. Switching Regulator Supply Sequencing

APPLICATIONS INFORMATION

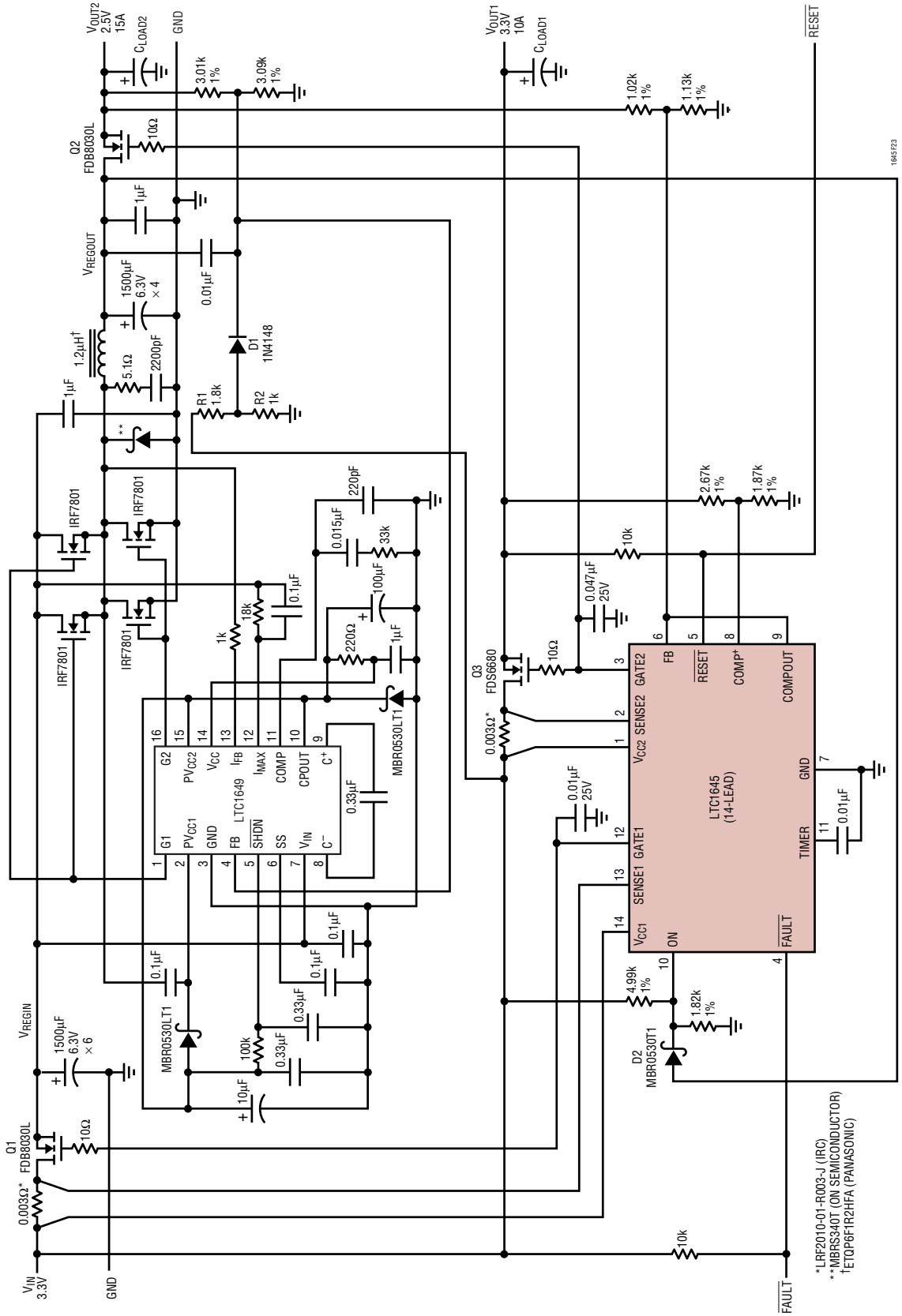


Figure 23. Switching Regulator Hot Swap

APPLICATIONS INFORMATION

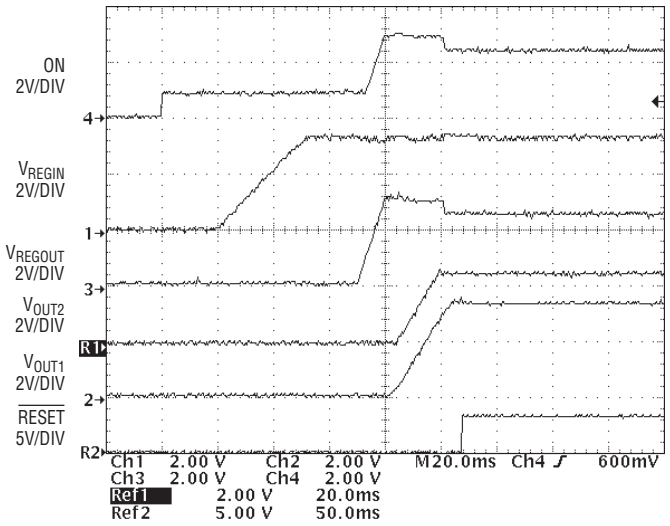


Figure 24. Switching Regulator Hot Swap

its FB or SENSE pin. In the case of the LTC1649, large peak currents result if the FB pin is at ground and not connected directly to the output inductor and capacitors. To keep the peak currents under control, R1, R2 and D1 hold the FB pin above ground but below its normal regulated value until V_{OUT2} ramps up and D1 reverse-biases.

Power N-Channel Selection

The $R_{DS(ON)}$ of the external pass transistors must be low enough so that the voltage drop across them is 100mV or less at full current. If the $R_{DS(ON)}$ is too high, the voltage drop across the transistor can cause the output voltage to trip the reset circuit. The transistors listed in Table 1 or other similar transistors are recommended for use with the LTC1645.

Low voltage applications may require the use of logic-level FETs; ensure their maximum V_{GS} rating is sufficient for the application. GATE voltage as a function of V_{CC} is illustrated in the Typical Performance curves. If lower GATE drive is desired, connect a diode in series with a zener between GATE and V_{CC} or between GATE and V_{OUT} as shown in Figure 25.

Table 1. N-Channel Selection Guide

CURRENT LEVEL	PART NUMBER	MANUFACTURER	DESCRIPTION
1A to 2A	NDH8503N	Fairchild	Dual N-Channel $R_{DS(ON)}$ = 0.033 SuperSOT-8
1A to 2A	Si6928DQ	Siliconix	Dual N-Channel $R_{DS(ON)}$ = 0.035 TSSOP-8
2A to 5A	Si4920DY	Siliconix	Dual N-Channel $R_{DS(ON)}$ = 0.025 SO-8
2A to 5A	IRF7313	International Rectifier	Dual N-Channel $R_{DS(ON)}$ = 0.029 SuperSOT-8
5A to 10A	Si4420	Siliconix	Single N-Channel $R_{DS(ON)}$ = 0.009 SO-8
5A to 10A	FDS6680	Fairchild	Single N-Channel $R_{DS(ON)}$ = 0.01 SO-8
5A to 10A	IRF7413	International Rectifier	Single N-Channel $R_{DS(ON)}$ = 0.011 SO-8
5A to 10A	MMSF3300	ON Semiconductor	Single N-Channel $R_{DS(ON)}$ = 0.0125 SO-8
10A to 20A	FDB8030L	Fairchild	Single N-Channel $R_{DS(ON)}$ = 0.0035 TO-263AB
10A to 20A	SUD75N03-04	Siliconix	Single N-Channel $R_{DS(ON)}$ = 0.004 D^2PAK

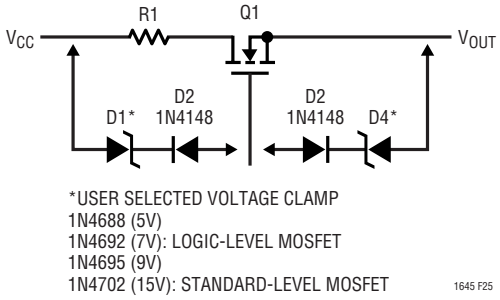
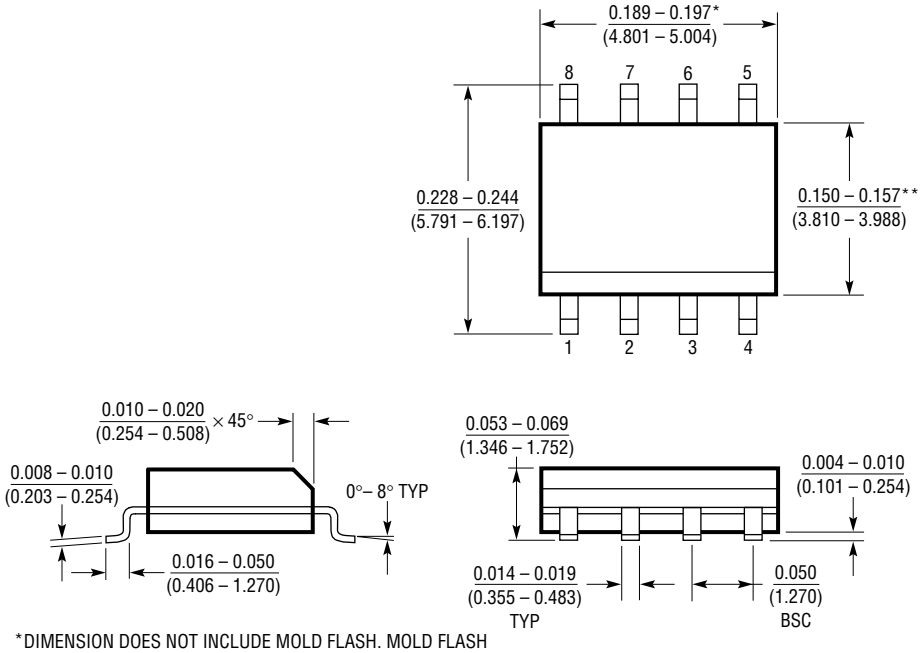


Figure 25. Optional Gate Clamp

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

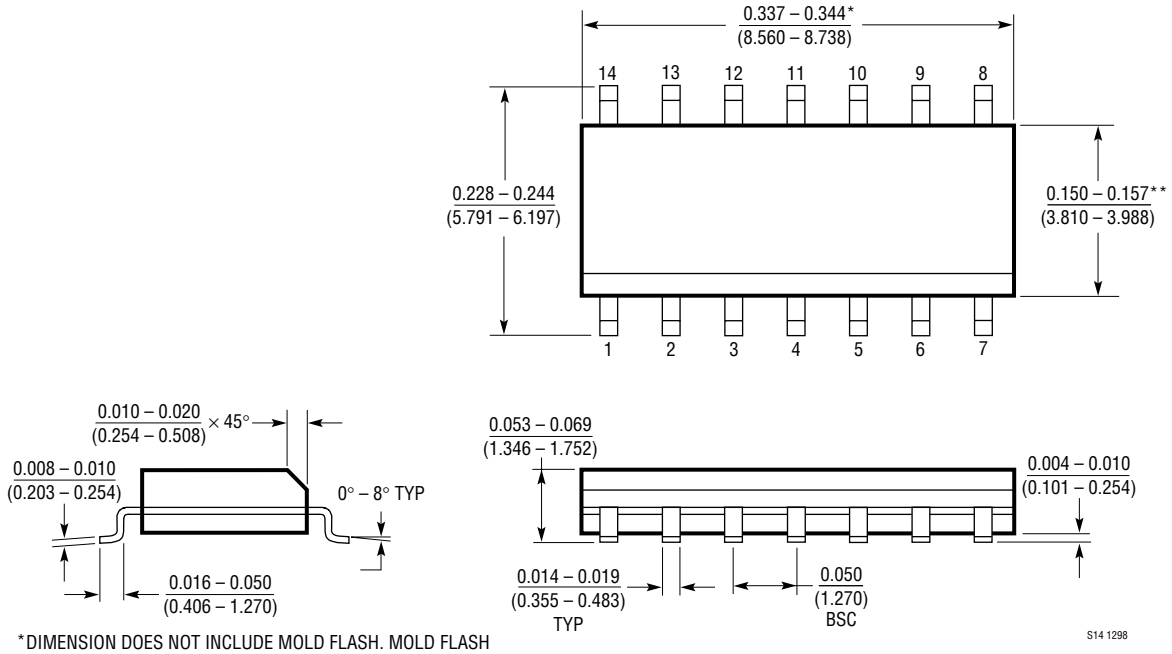
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 1298

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

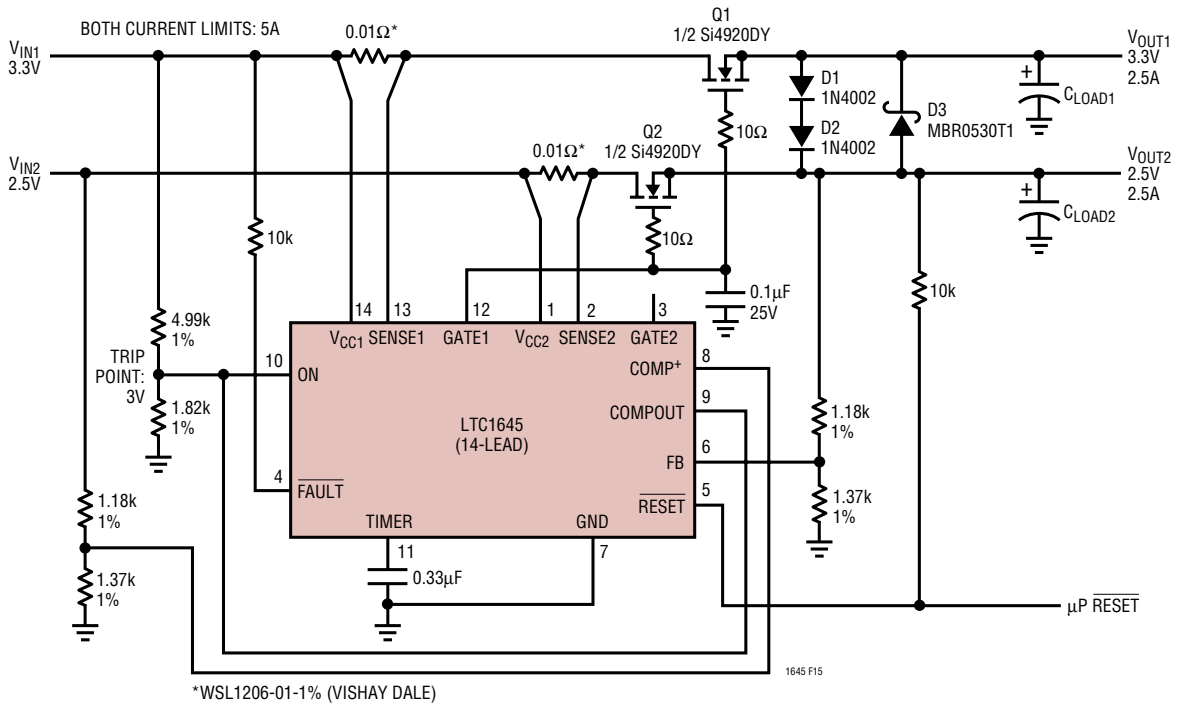


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Dual Supply Hot Swap with Tracking Outputs



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	Dual Supplies from 3V to 12V, Additionally –12V
LTC1422	Hot Swap Controller	Single Supply Hot Swap in SO-8 from 3V to 12V
LT1640L/LT1640H	Negative Voltage Hot Swap Controllers	Negative High Voltage Supplies from –10V to –80V
LT1641	Positive Voltage Hot Swap Controller	Positive High Voltage Supplies From 9V to 80V
LTC1642	Fault Protected Hot Swap Controller	3V to 15V, Overvoltage Protection Up to 33V
LTC1643L/LTC1643L-1/ LTC1643H	PCI-Bus Hot Swap Controllers	3.3V, 5V, 12V, –12V Supplies for PCI Bus
LTC1647	Dual Hot Swap Controller	Dual ON Pins for Supplies from 3V to 15V

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