LTC4056-4.2

Linear Li-Ion Charger with Termination in ThinSOT

February 2003

FEATURES

- **Standalone Li-Ion Charger with Termination**
- **Programmable Termination Timer**
- **No Sense Resistor or Blocking Diode Required**
- **Suitable for USB-Powered Charging**
- **Undervoltage Charge Current Limiting**
- **Preset Charge Voltage with ±0.6% Accuracy**
- Programmable Charge Current: 200mA to 700mA
- Automatic Recharge
- Self-Protection for Overcurrent/Overtemperature
- 40μA Supply Current in Shutdown Mode
- Negligible Battery Drain Current in Shutdown
- Low Battery Charge Conditioning (Trickle Charging)
- $\overline{\text{CHRG}}$ Status Output including AC Present Sense
- Low Profile (1mm) ThinSOT™ Package
- PCB Total Solution Area only 75mm^2 (700mA)

APPLICATIONS

- Cellular Telephones
- Handheld Computers
- Digital Cameras
- Charging Docks and Cradles
- Low Cost and Small Size Chargers

DESCRIPTION

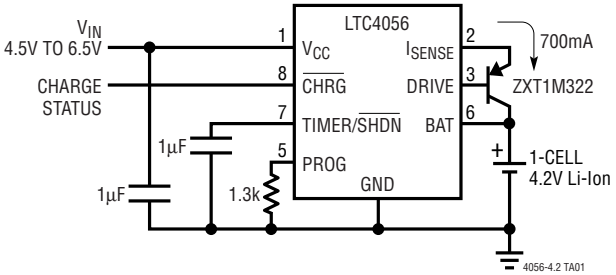
The LTC®4056 is a low cost, single-cell, constant-current/constant-voltage Li-Ion battery charger controller with a programmable termination timer. When combined with a few external components, the LTC4056 forms a very small standalone charger for single cell lithium-ion batteries.

Charge current and charge time are set externally with a single resistor and capacitor, respectively. The LTC4056 charges to a final float voltage accurate to ±0.6%. Manual shutdown is accomplished by grounding the TIMER/$\overline{\text{SHDN}}$ pin, while removing input power automatically puts the LTC4056 into a sleep mode. Both the shutdown and sleep modes drain near zero current from the battery and the shutdown mode reduces supply current to 40μA.

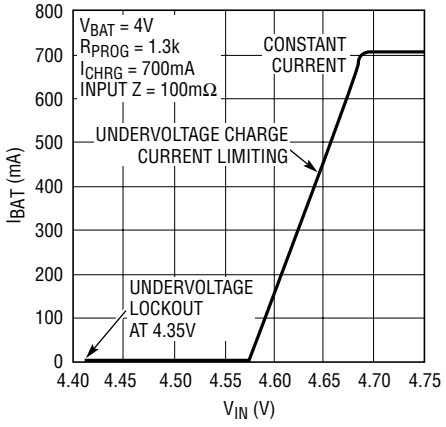
The output driver is both current limited and thermally protected to prevent operating outside of safe limits. No external blocking diode or sense resistor is required. The LTC4056 also includes low battery charge conditioning (trickle charging), undervoltage charge current limiting, automatic recharge and a charge status output.

The LTC4056 is available in a low profile (1mm) 8-lead ThinSOT package.

TYPICAL APPLICATION



V_{IN} Undervoltage Charge Current Limiting

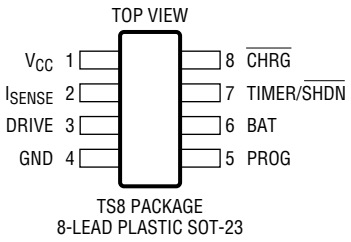


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{CC}) .....–0.3V to 10V
BAT, $\overline{CHRG}$ .....–0.3V to 10V
DRIVE, PROG, TIMER/$\overline{SHDN}$ ..... –0.3V to (V_{CC} + 0.3V)
Output Current (I_{SENSE}) 900mA
Short-Circuit Duration (BAT, I_{SENSE}) .....Continuous
Junction Temperature.....125°C
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



TS8 PACKAGE
8-LEAD PLASTIC SOT-23

T_{JMAX} = 125°C, θ_{JA} = 120°C/W TO 200°C/W
DEPENDING ON PC BOARD LAYOUT

ORDER PART NUMBER
LTC4056ETS8-4.2
TS8 PART MARKING
LTG5

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Supply							
V_{CC}	Input Supply Voltage (Note 3)		●	4.5		6.5	V
I_{CC}	Quiescent V_{CC} Supply Current	V_{BAT} = 4.5V (Forces I_{DRIVE} = 0) I_{PROG} = 200µA (R_{PROG} = 5k)	 ●		 400	 600	 µA
$I_{\overline{SHDN}}$	V_{CC} Supply Current in Manual Shutdown	$V_{TIMER/\overline{SHDN}}$ = 0V			40	60	µA
I_{BMS}	Battery Drain Current in Manual Shutdown (Note 4)	$V_{TIMER/\overline{SHDN}}$ = 0V	●	–1	0	1	µA
I_{BSL}	Battery Drain Current in Sleep Mode (Note 5)	V_{CC} = 0V	●	–1	0	1	µA
V_{UVLOI}	Undervoltage Rising Threshold	V_{CC} Increasing	●	4.325	4.40	4.475	V
V_{UVLOD}	Undervoltage Falling Threshold	V_{CC} Decreasing	●	4.275	4.35	4.425	V
V_{UVHYS}	Undervoltage Hysteresis	V_{UVLOI}-V_{UVLOD}			50		mV
V_{UVCL}	Undervoltage Charge Current Limit Threshold				4.575		V
V_{UVCL}-V_{UVLOI}	UV Charge Current to UVLO Threshold Margin		●	90	170	250	mV
Charging Performance							
V_{FLOAT}	Output Float Voltage in Constant Voltage Mode	I_{BAT} = 10mA I_{BAT} = 10mA, 4.75V ≤ V_{CC} ≤ 6.5V	 ●	4.175 4.158	4.200 4.200	4.225 4.242	V V
I_{BAT}	Output Full-Scale Current in Constant Current Mode	R_{PROG} = 5k, 4.75V ≤ V_{CC} ≤ 6.5V, Pass PNP Beta > 50, 0°C ≤ T_A ≤ 85°C		137	183	228	mA
		R_{PROG} = 1.43k, 4.75V ≤ V_{CC} ≤ 6.5V, Pass PNP Beta > 50, 0°C ≤ T_A ≤ 85°C		590	640	690	mA
I_{DSINK}	Drive Output Current	V_{DRIVE} = 3V	●	30			mA
I_{TRIKL}	Trickle Charge Current	V_{BAT} = 2V, R_{PROG} = 5k V_{BAT} = 2V, R_{PROG} = 1.43k		5 12	7 20	10 28	mA mA
V_{TRIKL}	Trickle Charge Threshold	V_{BAT} Falling	●	2.73	2.80	2.87	V
ΔV_{TRIKL}	Trickle Charge Hysteresis			45	70	95	mV
V_{PROG1}	PROG Pin Voltage	R_{PROG} = 5k (I_{PROG} = 200µA)	●	0.98	1	1.02	V
V_{PROG2}	PROG Pin Voltage	R_{PROG} = 1.43k (I_{PROG} = 700µA)	●	0.98	1	1.02	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{RECHRG}	Recharge Voltage Threshold	$V_{FLOAT} - V_{RECHRG}$, $V_{BAT} > V_{TRIKL}$, Charge Termination Timer Expired		100	150	200	mV
T_{TIMER}	TIMER/$\overline{SHDN}$ Accuracy	C_{TIMER} = 1µF R_{PROG} = 1.43k	●		10	12	%
Charger Manual Control							
V_{MSDT}	Manual Shutdown Threshold	$V_{TIMER/\overline{SHDN}}$ Increasing	●	0.6	0.82	1	V
V_{MSHYS}	Manual Shutdown Hysteresis	$V_{TIMER/\overline{SHDN}}$ Decreasing		50	75	125	mV
$I_{\overline{SHDN}}$	TIMER/$\overline{SHDN}$ Pin Pull-up Current	$V_{TIMER/\overline{SHDN}}$ = 0V		–10	–7	–4	µA
Protection							
I_{DSHRT}	Drive Output Short-Circuit Current Limit	$V_{DRIVE} = V_{CC}$	●	30	65	130	mA
I_{PSHRT}	PROG Pin Short-Circuit Current Limit	V_{PROG} = 0V			1.4		mA
Status Output							
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Weak Pull-Down Current	$V_{\overline{CHRG}}$ = 1V, $V_{TIMER/\overline{SHDN}}$ = 0V		6	12	18	µA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Output Low Voltage	$I_{\overline{CHRG}}$ = 10mA	●		0.2	0.4	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC4056E is guaranteed to meet performance specifications from 0°C to 70°C ambient temperature range. Specifications over the –40°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Although the LTC4056 will operate with input voltages as low as 4.5V, charging will not begin until V_{CC} exceeds V_{UVCL}.

Note 4: Assumes that the external PNP pass transistor has negligible B-C reverse-leakage current when the collector is biased at 4.2V (V_{BAT}) and the base is biased at 5V (V_{CC}).

Note 5: Assumes that the external PNP pass transistor has negligible B-E reverse-leakage current when the emitter is biased at 0V (V_{CC}) and the base is biased at 4.2V (V_{BAT}).

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Input Supply Voltage. This pin supplies power to the internal control circuitry and external PNP transistor through the internal current sense resistor. This pin should be bypassed to ground with a capacitor in the range of 1µF to 10µF.

I_{SENSE} (Pin 2): Sense Node for Charge Current. Current from V_{CC} passes through the internal current sense resistor and out of the I_{SENSE} pin to supply current to the emitter of the external PNP transistor. The collector of the PNP provides charge current to the battery.

DRIVE (Pin 3): Base Drive Output for the External PNP Pass Transistor. Provides a controlled sink current that drives the base of the PNP. This pin has current limiting protection.

GND (Pin 4): Ground. Provides a reference for the internal voltage regulator and a return for all internal circuits. When in the constant voltage mode, the LTC4056 will precisely regulate the voltage between the BAT and GND pins. The battery ground should connect close to the GND pin to avoid voltage drop errors.

BAT (Pin 5): Battery Voltage Sense Input. A precision internal resistor divider sets the final float voltage on this pin. This divider is disconnected in the manual shutdown or sleep mode. No bypass capacitance is needed on this pin for stable operation when a battery is present. However, any low ESR capacitor exceeding 22µF on this pin should be decoupled with 0.2Ω to 1Ω resistor. Without a battery, a minimum bypass capacitance of 4.7µF with 0.5Ω series resistance is required.

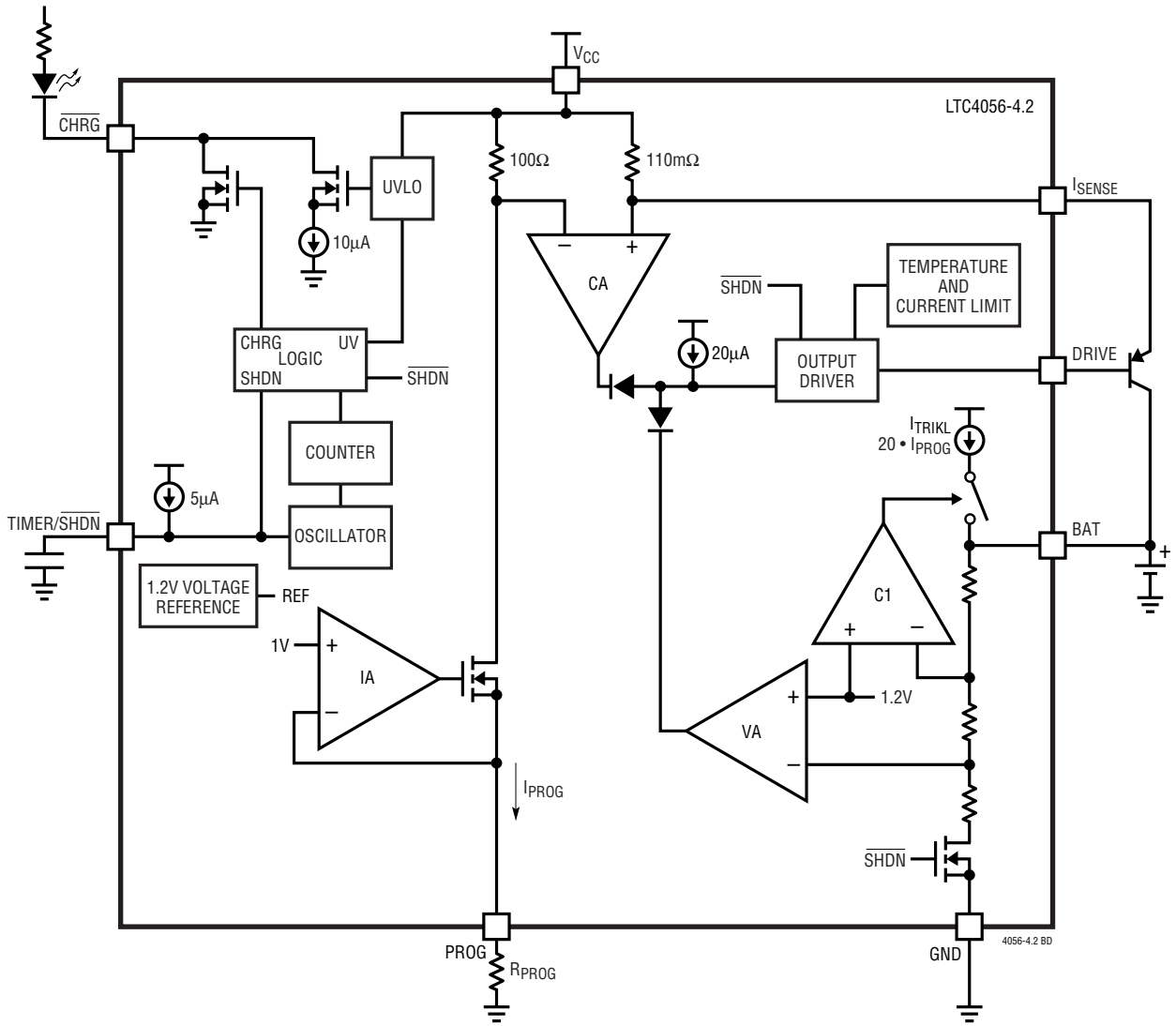
PROG (Pin 6): Charge Current Programming Pin. Provides a virtual reference voltage of 1V for an external resistor (R_{PROG}) connected between this pin and ground to program the battery charge current. The typical charge current is 915 times the current through this resistor (I_{BAT} = 915V/R_{PROG}). Current is limited to approximately 1.4mA (I_{BAT} of approximately 1.4A).

PIN FUNCTIONS

$\overline{\text{TIMER}}$/SHDN (Pin 7): Programmable Charge Termination Timer and Shutdown Input. Pulling this pin below the shutdown threshold voltage will shut down the charger reducing the supply current to approximately 40µA and the battery drain current to near 0µA. A capacitor on this pin programs the charge termination timer.

$\overline{\text{CHRG}}$ (Pin 8): Open-Drain Charge Status Output. When the battery is being charged, the $\overline{\text{CHRG}}$ pin is pulled low by an internal N-channel MOSFET. When the timer has timed out (terminating the charge cycle) or when the LTC4056 is in shutdown, but power is applied to the IC (i.e., $V_{CC} > V_{UVLOI}$), a 12µA current source is connected from the $\overline{\text{CHRG}}$ pin to ground. The $\overline{\text{CHRG}}$ pin is forced to a high impedance state when input power is not present (i.e., $V_{CC} < V_{UVLOD}$).

BLOCK DIAGRAM



OPERATION

The LTC4056 is a linear battery charger controller with a programmable charge termination timer. Operation can be understood by referring to the Block Diagram. A charge cycle begins when V_{CC} rises above the UVLO (undervoltage lockout) threshold V_{UVLOI} (nominally 4.4V), an external current programming resistor is connected between the PROG pin and ground and the TIMER/$\overline{SHDN}$ pin is allowed to rise above the shutdown threshold V_{MSDT} (nominally 0.82V).

If the battery voltage is below V_{TRIKL} (2.8V) at the beginning of the charge cycle, the charger goes into trickle charge mode to bring the cell voltage up to a safe level for charging at full current. In this mode, an internal current source provides approximately 2% of the programmed charge current to the BAT pin. The charger goes into the full charge constant current mode once the voltage on the BAT pin rises above $V_{TRIKL} + \Delta V_{TRIKL}$ (2.9V).

During full current charging, the collector of the external PNP provides the charge current. The PNP emitter current flows through the I_{SENSE} pin and through the internal 110mΩ current sense resistor. This current is close in magnitude, but slightly more than the collector current since it includes base current. Amplifier A1 forces 1V on the PROG pin. Therefore, a current equal to $1V/R_{PROG}$ will flow through the internal 100Ω resistor. Amplifier CA will force the same voltage that appears across the 100Ω resistor to appear across the internal 110mΩ resistor. This amplifier ensures that the current flowing out of the I_{SENSE} pin is equal to 915 times the current flowing out of the PROG pin. Therefore, neglecting base current, the charge current will be $915V/R_{PROG}$. This region of operation is referred to as constant current mode.

As the battery accepts charge, its voltage rises. When it reaches the preset float voltage of 4.2V, a precisely divided down version of this voltage (1.2V) is compared to the 1.2V internal reference voltage by amplifier VA. If the battery voltage attempts to exceed 4.2V (1.2V at the input of amplifier VA), the amplifier will divert current away from the output driver thus limiting charge current to maintain 4.2V on the battery. This is the constant voltage mode.

An external capacitor on the TIMER/$\overline{SHDN}$ pin and the resistance between the PROG pin and ground set the total charge time. When this time elapses, the charge cycle terminates and the $\overline{CHRG}$ pin transitions from a strong pull-down to a weak 12μA pull-down. To restart the charge cycle, simply remove the input voltage and reapply it or momentarily force the TIMER/$\overline{SHDN}$ pin to ground. The charge cycle will also restart if the BAT pin voltage falls below the recharge threshold (V_{RECHRG} is nominally 4.05V).

When V_{CC} is applied, pulling the TIMER/$\overline{SHDN}$ pin to ground will manually shut down the charger and reset the timer. When this pin is released an internal 7μA current source pulls the TIMER/$\overline{SHDN}$ pin above the 0.82V shutdown threshold to resume charging.

Fault conditions such as overheating of the die or excessive DRIVE pin or PROG pin current are monitored and limited.

When input power is removed or manual shutdown is entered, the charger will drain only tiny leakage currents (<1μA) from the battery, thus maximizing battery standby time. With V_{CC} removed the external PNP base is connected to the battery by the charger. In manual shutdown the base is connected to V_{CC} by the charger.

APPLICATIONS INFORMATION

Undervoltage Lockout

An internal undervoltage lockout (UVLO) circuit monitors the input voltage and keeps the charger in shutdown mode until V_{CC} rises above the UVLO threshold (V_{UVLOI} is typically 4.4V). Approximately 50mV of hysteresis is built in to prevent oscillation around the threshold level. In undervoltage lockout, battery drain current is very low (<1μA) and supply current is approximately 40μA.

Undervoltage Charge Current Limiting

The LTC4056 includes undervoltage charge current limiting that prevents full charge current until the input supply voltage reaches a threshold value (V_{UVCL}). This feature is particularly useful if the LTC4056 is powered from a supply with long leads (or any relatively high output impedance).

For example, USB powered systems tend to have highly variable source impedances (due primarily to cable quality and length). A transient load combined with such an impedance can easily trip the UVLO threshold and turn the charger off unless undervoltage charge current limiting is implemented.

Consider a situation where the LTC4056 is operating under normal conditions and the input supply voltage begins to sag (e.g. an external load drags the input supply down). If the input voltage reaches V_{UVCL} (approximately 170mV above the rising undervoltage lockout threshold, V_{UVLOI}), undervoltage charge current limiting will begin to reduce the charge current in an attempt to maintain V_{UVCL} at the V_{CC} input of the IC. The LTC4056 will continue to operate at the reduced charge current until the input supply voltage is increased or voltage mode reduces the charge current further.

Trickle Charge and Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is low (below V_{TRIKL} of about 2.8V) the charger goes into trickle charge mode reducing the charge current to approximately 2% of the full-scale current. If the low battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated and the $\overline{CHRG}$ pin output transitions from a strong pull-down to a 12μA pull-down. To restart the charge cycle, simply remove the input voltage and reapply it or momentarily force the TIMER/$\overline{SHDN}$ pin to ground.

Programming Charge Current

When in the constant current mode, the full-scale charge current is programmed using a single external resistor between the PROG pin and ground, R_{PROG}. The current delivered to the I_{SENSE} pin (flowing from V_{CC} through the internal 110mΩ sense resistor) will be 915 times the current in R_{PROG}. Because the LTC4056 provides a virtual 1V source at the PROG pin, the charge current is given by:

$$I_{CHRG} = \left(I_{PROG}\right) \bullet 915 = \left(\frac{1V}{R_{PROG}}\right) \bullet 915 \text{ or}$$

$$R_{PROG} = \left(\frac{1V}{I_{CHRG}}\right) \bullet 915$$

Under trickle charge conditions, this current is reduced to approximately 2% of the full-scale value. The actual battery charge current (I_{BAT}) is slightly lower than the expected charge current because the charger forces the emitter current and the battery charge current will be reduced by the base current. In terms of β (I_C/I_B), I_{BAT} can be calculated as follows:

$$I_{BAT}\left(A\right) = 915 \bullet I_{PROG}\left(\frac{\beta}{\beta+1}\right) = \frac{915V}{R_{PROG}} \bullet \left(\frac{\beta}{\beta+1}\right)$$

If β = 50, then I_{BAT} is 2% low. If desired, reducing R_{PROG} by 2% can compensate for the 2% loss.

For example, if 700mA charge current is required, calculate:

$$R_{PROG} = \left(\frac{1V}{700mA}\right) \bullet 915 = 1.3k$$

If a low β needs to be compensated for, say β = 50, calculate:

$$R_{PROG} = \frac{915V}{700mA} \bullet \left(\frac{50}{50+1}\right) = 1.27k$$

For best stability over temperature and time, 1% metal-film resistors are recommended.

APPLICATIONS INFORMATION

Termination Timer

The programmable timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER/$\overline{SHDN}$ pin and the external PROG resistor. The total charge time is:

$$Time(Hours) = 2.1 \bullet R_{PROG}(k) \bullet C_{TIMER}(\mu F) \text{ or}$$

$$C_{TIMER}(\mu F) = Time(Hours)/2.1 \bullet R_{PROG}(k)$$

For example, to program a three hour timer with a 640mA charge current (i.e., R_{PROG} = 1.43k), calculate:

$$C_{TIMER} = \frac{3}{2.1 \bullet 1.43} = 1\mu F$$

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied, a program resistor is connected to ground and the TIMER/$\overline{SHDN}$ pin is allowed to rise above the shutdown threshold. After a time-out occurs, the charge current stops and the $\overline{CHRG}$ output transitions from a strong pull-down to a 12µA pull-down to indicate charging has stopped. As long as the input supply remains above V_{UVLOD} and the battery voltage remains above V_{RECHRG} the charger will remain in this standby mode.

If the battery voltage remains below V_{TRIKL} for 25% of the programmed time, the charger will enter standby mode. Furthermore, if the battery voltage is above the recharge threshold (V_{RECHRG} is typically 4.05V) at the beginning of a charge cycle or if a falling battery voltage triggers a recharge cycle (following a previous time-out), the charger will enter standby mode after 50% of the programmed time. This feature reduces the charge time for batteries that are near full capacity. Connecting the TIMER/$\overline{SHDN}$ pin to V_{CC} disables the timer function.

Manual Shutdown

Pulling the TIMER/$\overline{SHDN}$ pin below $V_{MSDT} - V_{MSHYS}$ (typically 0.745V) will put the charger into shutdown mode. In this mode, the LTC4056 consumes 40µA of supply current and drains a negligible leakage current from the battery (I_{BMS}).

A 7µA current source pulls up on the TIMER/$\overline{SHDN}$ pin while in shutdown to ensure that the IC will start up once the TIMER/$\overline{SHDN}$ pin is released. Given the low magnitude of this current, it is a simple matter for an external open-drain (or open-collector) output to pull the TIMER/$\overline{SHDN}$ pin to ground for shutdown and release the pin for normal operation.

Sleep Mode

When the input supply is disconnected, the IC enters the sleep mode. In this mode, the battery drain current (I_{BSL}) is a negligible leakage current, allowing the battery to remain connected to the charger for an extended period of time without discharging the battery. The leakage current is due to the reverse-biased B-E junction of the external PNP transistor. Furthermore, the $\overline{CHRG}$ pin assumes a high impedance state.

$\overline{CHRG}$ Status Output Pin

When the charge cycle starts, the $\overline{CHRG}$ pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. Upon termination, the strong pull-down transitions to a 12µA pull-down on the $\overline{CHRG}$ pin as long as the input supply remains above the UVLO threshold (V_{UVLOD}) and the battery voltage remains above V_{RECHRG}. If the input supply falls below V_{UVLOD}, the $\overline{CHRG}$ pin assumes a high impedance state. Figure 1 shows a flow diagram for a typical charge cycle. This diagram indicates the status of the $\overline{CHRG}$ pin in each charger state.

A microprocessor can be used to distinguish the three states of the $\overline{CHRG}$ pin (see Figure 2). To detect whether the LTC4056 is in trickle charge, charge, or short charge mode (i.e., strong pull-down), force the digital output pin (OUT) high and measure the voltage at the $\overline{CHRG}$ pin. The internal N-channel MOSFET will pull the pin voltage low even with the 2k pull-up resistor. Once the charge cycle terminates, the strong pull-down transitions to a 12µA pull-down. The IN pin will then be pulled high by the 2k pull-up resistor. To determine whether sufficient input voltage is present for charging (i.e., high impedance), the OUT pin should be forced to a high impedance state. If $V_{CC} > V_{UVLOI}$ then the 12µA $\overline{CHRG}$ pull-down will pull the IN pin low through the 800k resistor; otherwise, the 800k resistor will pull the IN pin high, indicating that $V_{CC} < V_{UVLOD}$.

APPLICATIONS INFORMATION

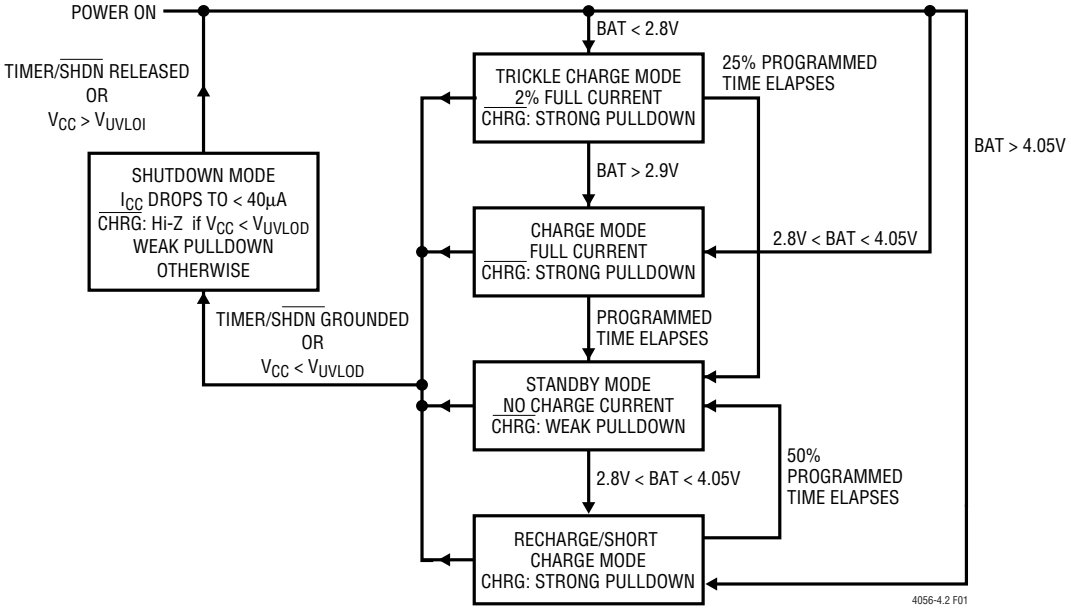


Figure 1. State Diagram for a Typical Charge Cycle

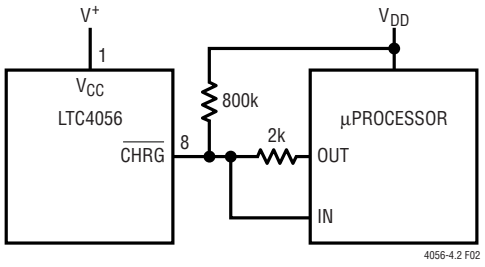


Figure 2. Using a Microprocessor to Determine $\overline{CHRG}$ State

Recharge

If the battery voltage drops below V_{RECHRG} (typically 4.05V) after a charge cycle has terminated, a new charge cycle will begin. The recharge circuit integrates the BAT pin voltage for approximately a millisecond to prevent a transient from restarting the charge cycle. During a recharge cycle the timer will terminate the charge cycle after one-half of the programmed time has elapsed.

If the battery voltage remains below V_{TRIKL} (typically 2.8V) during trickle charge for one-fourth of the programmed time, the battery may be defective and the charge cycle will end. In addition, the recharge comparator is disabled and a new charge cycle will not begin unless the input voltage is toggled off then on, or the TIMER/$\overline{SHDN}$ pin is momentarily pulled to ground.

External PNP Transistor

The external PNP pass transistor must have adequate beta, low saturation voltage and sufficient power dissipation capability (including any heat sinking, if required).

To provide 700mA of charge current with the minimum available base drive of approximately 30mA requires a PNP beta greater than 23. If lower beta PNP transistors are used, more base current is required from the LTC4056. This can result in the output drive current limit being reached, or thermal shutdown due to excessive power dissipation.

With low supply voltages, the PNP saturation voltage (V_{CESAT}) becomes important. The V_{CESAT} must be less than the minimum supply voltage minus the maximum voltage drop across the internal sense resistor and bond wires (0.20Ω) and battery float voltage. If the PNP transistor cannot achieve the low saturation voltage required, base current will dramatically increase. This is to be avoided for a number of reasons: output drive may reach current limit resulting in the charger characteristics to go out of specifications, excessive power dissipation may force the IC into thermal shutdown, or the battery could become discharged because some of the current from the

APPLICATIONS INFORMATION

DRIVE pin could be pulled from the battery through the forward biased collector base junction.

For example, to program a charge current of 500mA with a minimum supply voltage of 4.75V, the minimum operating V_{CE} is:

$$V_{CE(MIN)}(V) = 4.75 – (0.5) • (0.2) – 4.2 = 0.45V$$

Another important factor to consider when choosing the PNP pass transistor is the power handling capability. The transistor data sheet will usually give the maximum rated power dissipation at a given ambient temperature with a power derating for elevated temperature operation. The maximum power dissipation of the PNP when charging is:

$$P_{D(MAX)}(W) = I_{BAT} • (V_{CC(MAX)} – V_{BAT(MIN)})$$

$V_{CC(MAX)}$ is the maximum supply voltage and $V_{BAT(MIN)}$ is the minimum battery voltage when discharged.

Once the maximum power dissipation and $V_{CE(MIN)}$ are known, Table 1 can be used as a guide in selecting some PNPs to consider. In the table, very low V_{CESAT} is less than 0.25V, low V_{CESAT} is 0.25V to 0.5V and the others are 0.5V to 0.8V all depending on the current. See the manufacturer data sheet for details. All of the transistors are rated to carry at least 1A continuously as long as the power dissipation is within limits. In addition, the maximum supply voltage, minimum battery voltage and chosen charge current should be checked against the manufacturer's data sheet to ensure that the PNP transistor is operating within its safe operating area. The Stability section addresses caution in the use of very high beta PNPs.

Should overheating of the PNP transistor be a concern, protection can be achieved with a positive temperature coefficient (PTC) thermistor wired in series with the current programming resistor and thermally coupled to the transistor. The PTH9C chip series from Murata has a steep resistance increase at temperature thresholds from 85°C to 145°C making it behave somewhat like a thermostat switch. For example, the model PTH9C16TBA471Q thermistor is 470Ω at 25°C but abruptly increases its resistance to 4.7k at 125°C. Below 125°C, the device exhibits a small negative TC. The 470Ω thermistor can be added in series with a 976Ω resistor to form the current programming resistor for a 640mA charger. Should the thermistor reach 125°C, the charge current will drop to 160mA and inhibit any further increase in temperature.

Stability

The LTC4056 contains two control loops: constant voltage and constant current. The constant voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length,

Table 1. PNP Pass Transistor Selection Guide

MAXIMUM P_D(W) MOUNTED ON BOARD AT T_A = 25°C	PACKAGE STYLE	ZETEX PART NUMBER	ROHM PART NUMBER	COMMENTS
3	2 x 2MLP	ZXT1M322		Very Low V_{CESAT}
0.5	SOT-23	FMMT549		Low V_{CESAT}
0.625	SOT-23	FMMT720		Very Low V_{CESAT}, High Beta
1	SOT-89	FCX589 or BCX69		
1.1	SOT-23-6	ZXT13P12DE6		Very Low V_{CESAT}, High Beta, Small
1 to 2	SOT-89	FCX717		Very Low V_{CESAT}, High Beta
2	SOT-223	FZT589		Low V_{CESAT}
2	SOT-223	BCP69 or FZT549		
0.75	FTR		2SB822	Low V_{CESAT}
1	ATV		2SB1443	Low V_{CESAT}
2	SOT-89		2SA1797	Low V_{CESAT}
10 (T_C = 25°C)	TO-252		2SB1182	Low V_{CESAT}, High Beta

APPLICATIONS INFORMATION

however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to ground. Furthermore, a 4.7µF capacitor with a 0.2Ω to 1Ω series resistor from BAT to ground is required to keep ripple voltage low when the battery is disconnected.

High value capacitors with very low ESRs (especially ceramic) reduce the constant voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In the constant current mode, the PROG pin is in the feedback loop, not the battery. Because of the additional pole created by PROG capacitance, capacitance on this pin must be limited. Although higher charge current applications (i.e., lower program resistance) can tolerate more PROG capacitance, a good rule of thumb is to keep the capacitive loading on the PROG pin to less than 660pF.

If additional capacitance on this pin is required (e.g., to provide an accurate, filtered low current 1V reference to external circuitry) a 1k to 10k decoupling resistor may be needed (see Figure 3).

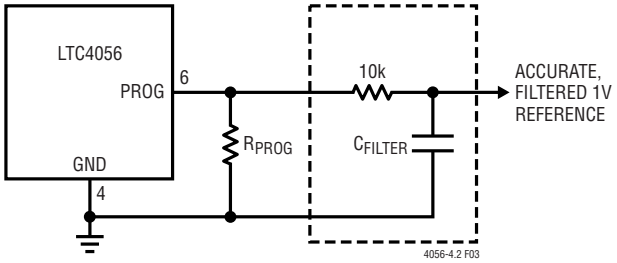


Figure 3. Isolating Capacitive Load on PROG Pin and Filtering

Reverse Polarity Input Voltage Protection

In some applications, protection from reverse polarity voltage on V_{CC} is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases, where the voltage drop must be kept low, a P-channel MOSFET can be used (as shown in Figure 4).

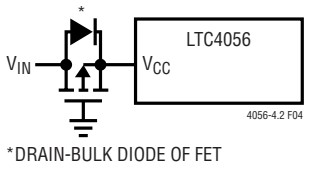


Figure 4. Low Loss Input Reverse Polarity Voltage Protection

V_{CC} Bypass Capacitor

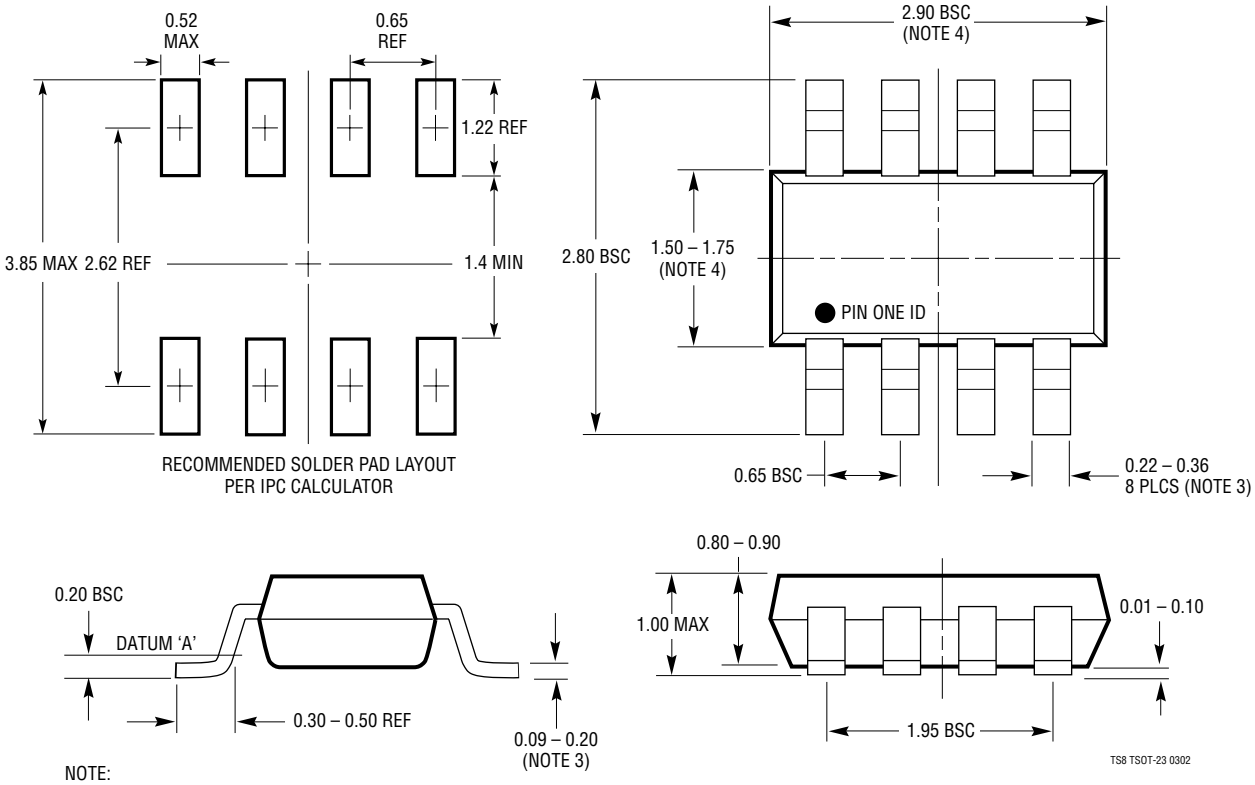
Many types of capacitors with values ranging from 1µF to 10µF located close to the LTC4056 will provide adequate input bypassing. However, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a hot power source. For more information refer to Application Note 88.

Internal Protection

Internal protection is provided to prevent excessive PROG pin currents (I_{PSHRT}), excessive DRIVE pin currents (I_{DSHRT}) and excessive self-heating of the LTC4056 during a fault condition. The faults can be generated from a shorted PROG pin, a shorted DRIVE pin or from excessive DRIVE pin current to the base of the external PNP transistor when it is in deep saturation from a very low V_{CE}. This protection is not designed to prevent overheating of the external pass transistor. However, thermal coupling between the external PNP and the LTC4056 will allow the internal thermal limit to deprive the PNP of base current when the junction temperature of the IC rises above about 135°C. The temperature of the PNP at that point, however, will be well in excess of 135°C. The exact temperature of the PNP depends on the thermal coupling between the LTC4056 and the PNP and on the θ_{JA} of the transistor. See the section titled "External PNP Transistor" for information on protecting the transistor from overheating.

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1571	200kHz/500kHz Switching Battery Charger	Up to 1.5A Charge Current; Preset and Adjustable Battery Voltages
LTC1729	Lithium-Ion Battery Charger Termination Controllers	Time or Charge Current Termination, Preconditioning 8-Lead MSOP
LTC1730	Lithium-Ion Battery Pulse Charger	No Blocking Diode Required, Current Limit for Maximum Safety
LTC1731	Lithium-Ion Linear Battery Charger Controller Charger Detection and Programmable Timer	Simple Charger uses External FET, Features Preset Voltages, C/10
LTC1732	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Features Preset Voltages, C/10 Charger Detection and Programmable Timer, Input Power Good Indication
LTC1733	Monolithic Lithium-Ion Linear Battery Charger	Standalone charger with Programmable Timer, Up to 1.5A Charge Current, Thermal Regulation Prevents Overheating
LTC1734	Lithium-Ion Linear Battery Charger in ThinSOT	200mA to 700mA, Simple ThinSOT Charger, No Blocking Diode, No Sense Resistor Needed
LTC1734L	Lithium-Ion Linear Battery Charger Controller	50mA to 180mA, No Blocking Diode, No Sense Resistor Needed
LTC4050	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Thermistor Input for Battery Temperature Sensing
LTC4052	Lithium-Ion Linear Battery Pulse Charger	Fully Integrated, Standalone Pulse Charger, Minimal Heat Dissipation, Over Current Protection
LTC4053	USB Compatible Lithium-Ion Battery Linear Monolithic Charger	Fully Integrated, Standalone Charger, 10-Lead MSOP, Thermal Regulation Prevents Overheating when Powered from Wall Adapter and ≥1A Charge Current
LTC4054	Standalone Lithium-Ion Linear Battery Charger in ThinSOT	Programmable Charge Current Up to 800mA; C/10 Charge Termination, Complete Charger; No External MOSFET, Diode or Sense Resistor
LTC4410	USB Power Manager	Manages Total Power Between a USB Peripheral and Battery Charger; Ensures Simultaneous Charging and use of Peripheral, ThinSOT Package

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