# LF2250
## 12 x 10-bit Matrix Multiplier

LOGIC DEVICES INCORPORATED

## FEATURES

- 50 MHz Data and Computation Rate
- Nine Multiplier Array with 12-bit Data and 10-bit Coefficient Inputs
- Separate 16-bit Cascade Input and Output Ports
- On-board Coefficient Storage
- Four User-Selectable Filtering and Transformation Functions:
  - 3 x 3 Matrix Multiplier
  - Cascadable 9-Tap FIR Filter
  - Cascadable 3 x 3 Convolver
  - Cascadable 4 x 2 Convolver
- Replaces TRW/Raytheon/Fairchild TMC2250
- 120-pin PQFP

## DESCRIPTION

The **LF2250** is a high-speed matrix multiplier consisting of an array of nine 12 x 10-bit multipliers. Internal summing adders are also included to provide the configurations needed to implement matrix multiplications, cascadable FIR filters, and pixel convolvers.

The 3 x 3 matrix multiplier (triple dot product) configuration of the LF2250 allows users to easily perform three-dimensional perspective translations or video format conversions at real-time video rates. By using the LF2250 in this configuration, conversions can be made from the RGB (color component) format to the YIQ (quadrature encoded chrominance) or YUV (color difference) formats and vice versa (YIQ or YUV to RGB).

In addition to color space conversions, the LF2250 offers a range of selectable configurations designed for filtering applications. When configured as a 9-tap FIR filter, the LF2250 automatically selects the necessary internal bus structure and inserts the appropriate data path delay elements. In addition, a 16-bit cascade input port allows for the creation of larger filters without a reduction in throughput.

Real-time video image filtering using the convolver modes of the LF2250 can provide edge detection, texture enhancement, and detail smoothing. Both pixel convolver configurations, 3 x 3 and 4 x 2, deliver high-speed data manipulation in a single chip solution. By using the 16-bit cascade input port to cascade two devices, cubic convolutions (4 x 4-pixel) can be easily accommodated with no decrease in throughput rates.

All inputs and outputs, as well as all control lines, are registered on the rising edge of clock. The LF2250 operates at clock rates up to 50 MHz over the full commercial temperature and supply voltage ranges.

## LF2250 Block Diagram

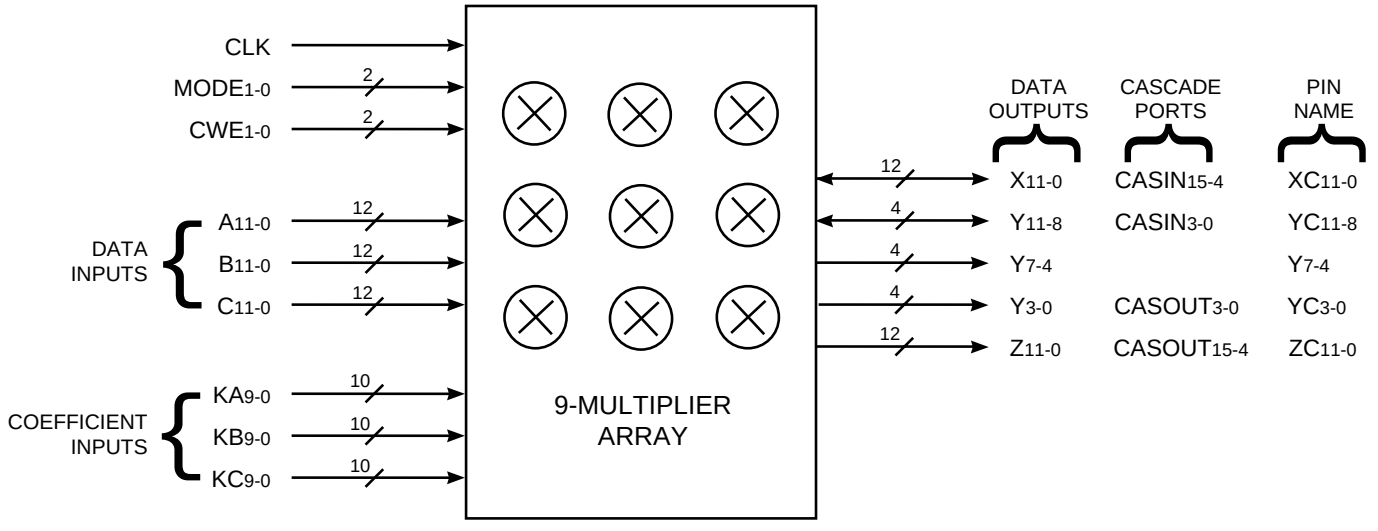


**TABLE 1. MODE SELECTION**

| MODE1-0 | OPERATING MODE |
|---|---|
| 00 | 3 x 3 Matrix Multiplier |
| 01 | 9-Tap FIR Filter |
| 10 | 3 x 3 Convolver |
| 11 | 4 x 2 Convolver |

## OPERATING MODES

The LF2250 can realize four different user-selectable digital filtering architectures as determined by the state of the mode (MODE1-0) inputs. Upon selection of the desired function, the LF2250 automatically chooses the appropriate internal data paths and input/output bus structure. Table 1 details the modes of operation.

## DATA FORMATTING

The coefficient input ports (KA, KB, KC) are 10-bit fractional two's complement format regardless of the operating mode. The data input ports (A, B, C) are 12-bit integer two's complement format regardless of the operating mode.

In the matrix multiplier mode (Mode 00), the data output ports (X, Y, Z) are 12-bit integer two's complement format. In the FIR filter and convolver modes (Modes 01, 10, 11), the X, Y, and Z ports are configured as the cascade-in (CASIN15-0) and cascade-out (CASOUT15-0) ports. These ports assume 16-bit (12-bit integer, 4-bit fractional) two's complement data on both the inputs and outputs. Table 2 shows the data port formatting for each of the four operating modes.

## BIT WEIGHTING

The internal sum of products of the LF2250 can grow to 23 bits. However, in order to keep the output format of the matrix multiply mode (Mode 00) identical to the input format, the X, Y, and Z outputs are truncated to 12-bit integer words. In the filter modes (Modes 01, 10, 11), the cascade output is always half-LSB rounded to 16 bits (12 integer bits and 4 fractional bits). The user may half-LSB round the output to any size less than 16 bits by simply forcing a "1" into the bit position of the cascade input immediately below the desired LSB. For example, if half-LSB rounding to 12 bits is desired, then a "1" must be forced into the CASIN3 bit position (CASOUT4 would then be the LSB).

In all four modes, the user may adjust the bit weighting, by applying an identical scaling correction factor to both the input and output data streams. If the coefficients are re-scaled, then the relative weightings of the cascade-in and cascade-out ports will differ accordingly. Figure 1 illustrates the input and output bit weightings for all four modes.

## DATA OVERFLOW

Because the LF2250's matched input and output data formats accommodate unity gain (0 dB), input conditions that could lead to numeric overflow may exist. To ensure that no overflow conditions occur, the user must be aware of the maximum input data and coefficient word sizes allowable for each specific algorithm being performed.

## SIGNAL DEFINITIONS

### Power

*VCC and GND*

+5 V power supply. All pins must be connected.

### Clock

*CLK — Master Clock*

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

### Inputs

*A11-0, B11-0, C11-0 — Data Inputs*

A, B, and C are the 12-bit registered data input ports. Data presented to these ports is latched into the multiplier input registers for the current operating mode (Table 1). In the filter modes (Modes 01, 10, 11), the rising edge of CLK internally right-shifts new data to the next filter tap.

*KA9-0, KB9-0, KC9-0 — Coefficient Inputs*

KA, KB, and KC are the 10-bit registered coefficient input ports. Data presented to these ports is latched into the corresponding internal coefficient register set defined by CWE1-0 (Table 4) on the next rising edge of CLK. Table 3 shows which coefficient registers are available for each coefficient input port.

**TABLE 2. DATA PORT FORMATTING**

| | PIN NAMES | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODE1-0 | A11-0 | B11-0 | C11-0 | KA9-0 | KB9-0 | KC9-0 | XC11-0 | YC11-8 | Y7-4 | YC3-0 | ZC11-0 |
| 00 | A11-0 | B11-0 | C11-0 | KA9-0 | KB9-0 | KC9-0 | X11-0 | Y11-8 | Y7-4 | Y3-0 | Z11-0 |
| 01 | A11-0 | A11-0 | NC | KA9-0 | KB9-0 | KC9-0 | CASIN15-4 | CASIN3-0 | NC | CASOUT3-0 | CASOUT15-4 |
| 10 | A11-0 | B11-0 | C11-0 | KA9-0 | KB9-0 | KC9-0 | CASIN15-4 | CASIN3-0 | NC | CASOUT3-0 | CASOUT15-4 |
| 11 | A11-0 | B11-0 | NC | KA9-0 | KB9-0 | KC9-0 | CASIN15-4 | CASIN3-0 | NC | CASOUT3-0 | CASOUT15-4 |

**FIGURE 1A. INPUT FORMATS**

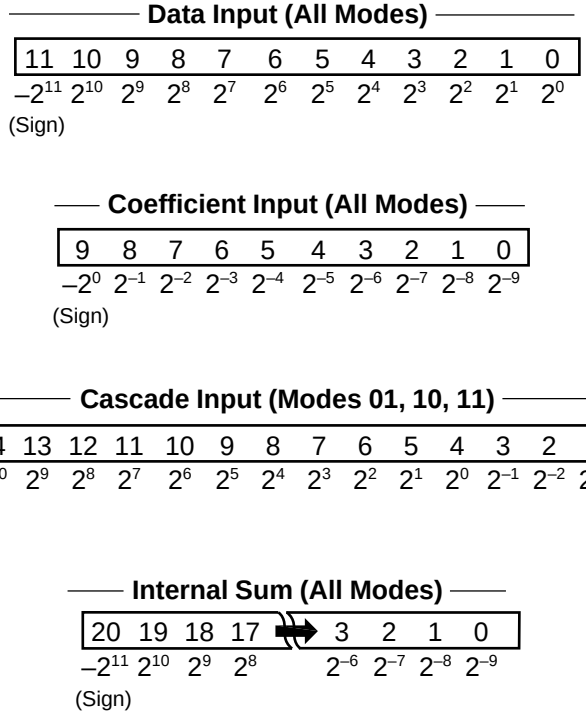
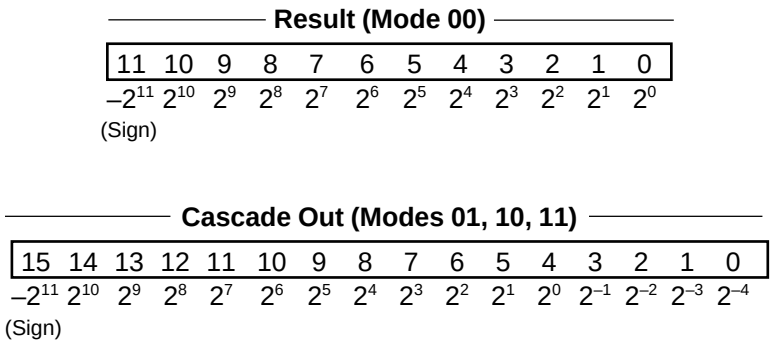



**FIGURE 1B. OUTPUT FORMATS**




*CASIN15-0 — Cascade Input*

In the filter modes (Modes 01, 10, 11), the 12-bit X port and four bits of the Y port are internally reconfigured as the 16-bit registered cascade input port. Data presented to this port will be added to the internal sum of products.

**Outputs**

*X11-0, Y11-0, Z11-0 — Data Outputs*

X, Y, and Z are the 12-bit registered output ports for the matrix multiply mode (Mode 00). These ports are automatically reconfigured for the filter modes (Modes 01, 10, 11) as the cascade-in and cascade-out ports.

*CASOUT15-0 — Cascade Output*

In the filter modes (Modes 01, 10, 11), the 12-bit Z port and four bits of the Y port are internally reconfigured as the 16-bit registered cascade output port.

***NOTE:*** *The X, Y, and Z ports are automatically reconfigured by the LF2250 as the cascade-in and cascade-out ports as required for each operating mode. Because both the X and Z ports are used for the cascade ports, all X port pins and all Z port pins are labelled as XC and ZC, respectively. All Y port pins that are used for the cascade ports are labelled as YC. Those Y port pins which are not used for the cascade ports are labelled as Y.*

**Controls**

*MODE1-0 — Mode Select*

The registered mode select inputs determine the operating mode of the LF2250 (Table 1) for data being input on the next clock cycle. When switching between modes, the internal pipeline latencies of the device must be observed. After switching operating modes, the user must allow enough clock cycles to pass to flush the internal registers before valid data will appear on the outputs.

*CWE1-0 — Coefficient Write Enable*

The registered coefficient write enable inputs determine which internal coefficient register set to update (Table 4) on the next clock cycle.

**TABLE 3. COEFFICIENT INPUTS**

| INPUT PORT | REG. AVAILABLE |
|---|---|
| KA | KA1, KA2, KA3 |
| KB | KB1, KB2, KB3 |
| KC | KC1, KC2, KC3 |

| TABLE 4. COEFF. REG. UPDATE | |
|---|---|
| **CWE1-0** | **COEFFICIENT SET** |
| 00 | Hold All Registers |
| 01 | KA1, KB1, KC1 |
| 10 | KA2, KB2, KC2 |
| 11 | KA3, KB3, KC3 |

## DETAILS OF OPERATION

*3 x 3 Matrix Multiplier — Mode 00*

In this mode, all three input ports (A, B, C) and all three output ports (X, Y, Z) are utilized to implement a 3 x 3 matrix multiplication (triple dot product). Each rounded 12-bit output is the sum of all three input words multiplied by the appropriate coefficients (Table 5). The pipeline latency for this mode is five clock cycles. Therefore, the sum of products will be output five clock cycles after the input data has been latched. New output data is subsequently available every clock cycle thereafter.

*9-Tap FIR Filter — Mode 01*

This mode utilizes the 12-bit A and B data input ports as well as the 16-bit CASIN port. The input data should be presented to the A and B ports simultaneously. The resulting 9-sample response, which is half-LSB rounded to 16 bits, begins after five clock cycles and ends after 13 clock cycles (Table 5). The pipeline latency from the input of an impulse response to the center of the output response is nine clock cycles. The latency from the CASIN port to the CASOUT port is four clock cycles. New output data is available every clock cycle.

*3 x 3-Pixel Convolver — Mode 10*

When configured in this mode, line delayed data is loaded through the A, B, and C input ports. During each cycle, a new rounded 16-bit output (comprising of the summation of the multiplications of the last nine data inputs with their related coefficients) becomes available (Table 5). The CASIN term is also added to each new output. The internal bus structure and pipeline delays allow new input data to be added every cycle while maintaining the structure of the filtering operation. This addition of new data every cycle produces the effect of the convolution window moving to the next pixel column.

*4 x 2-Pixel Convolver — Mode 11*

Using the A and B ports, input data is loaded and multiplied by the on-board coefficients. These products are then summed with the CASIN data and rounded to create the 16-bit output. The cascade ports allow multiple devices to be used together for use with larger kernels. As with Mode 10, each cycle results in a 16-bit output created from the products and summations performed.

**TABLE 5. LATENCY EQUATIONS**

**3 x 3 Matrix Multiplier — Mode 00**

$$X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)$$
$$Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)$$
$$Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)$$

**9-Tap FIR Filter — Mode 01**

$$CASOUT(n+12) = A(n+8)KA3(n+8) + A(n+7)KA2(n+7) + A(n+6)KA1(n+6) + B(n+5)KB3(n+8) + B(n+4)KB2(n+7) + B(n+3)KB1(n+6) + B(n+2)KC3(n+8) + B(n+1)KC2(n+7) + B(n)KC1(n+6) + CASIN(n+9)$$

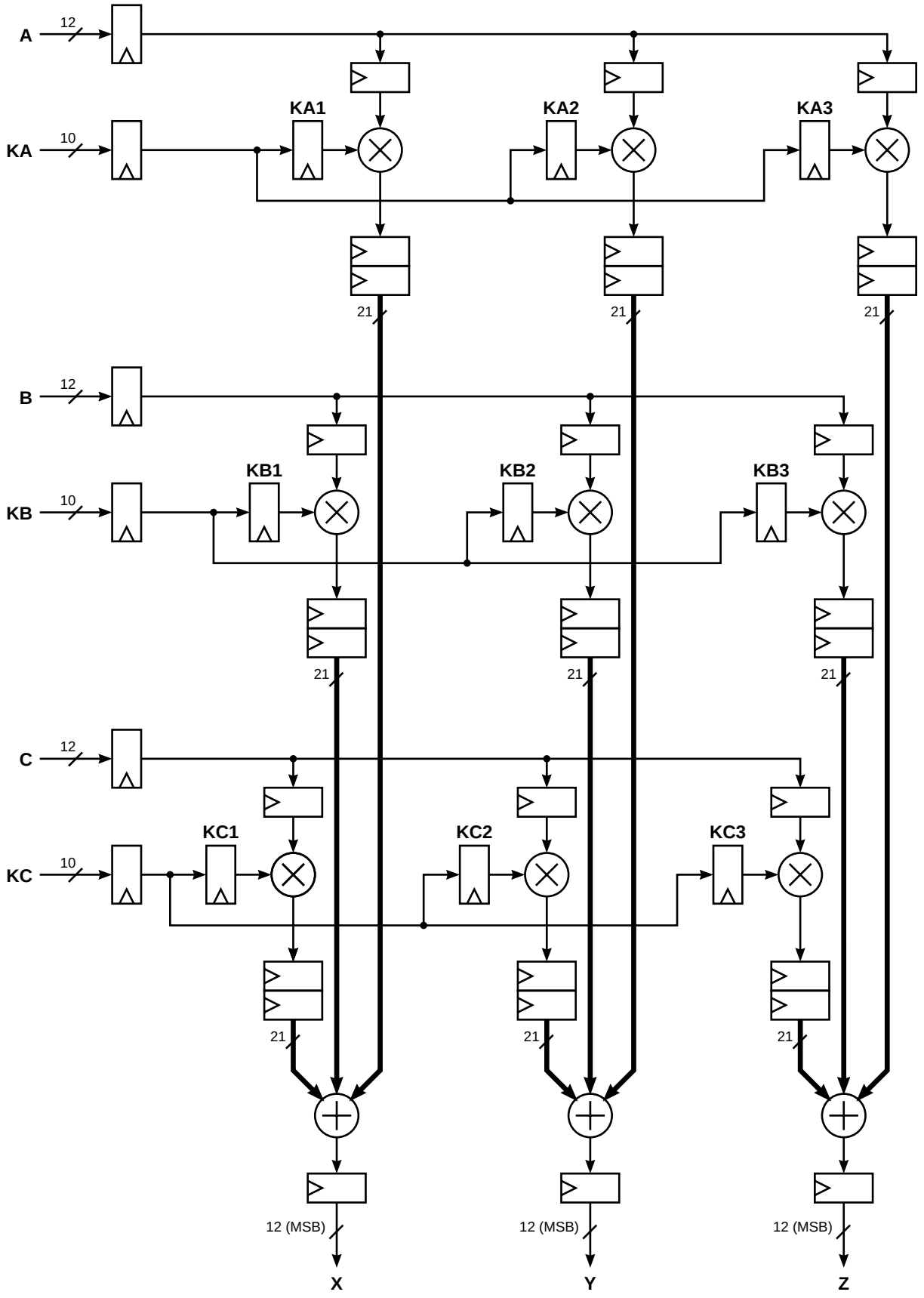
**3 x 3-Pixel Convolver — Mode 10**

$$CASOUT(n+6) = A(n+2)KA3(n+2) + A(n+1)KA2(n+1) + A(n)KA1(n) + B(n+2)KB3(n+2) + B(n+1)KB2(n+1) + B(n)KB1(n) + C(n+2)KC3(n+2) + C(n+1)KC2(n+1) + C(n)KC1(n) + CASIN(n+3)$$

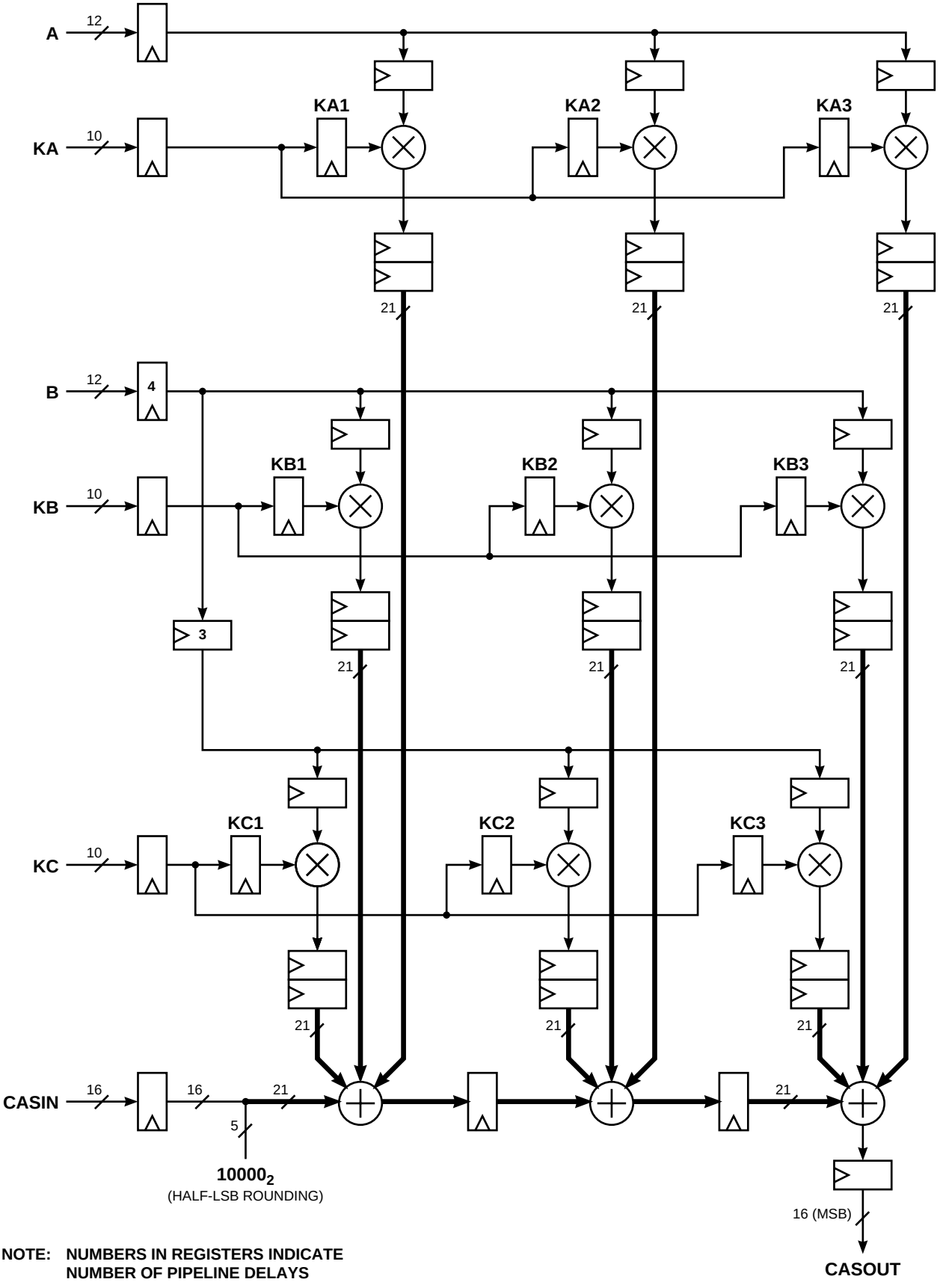
**4 x 2-Pixel Convolver — Mode 11**

$$CASOUT(n+7) = A(n+3)KA3(n+3) + A(n+2)KA2(n+2) + A(n+1)KA1(n+1) + A(n)KC3(n+3) + B(n+3)KB3(n+3) + B(n+2)KB2(n+2) + B(n+1)KB1(n+1) + B(n)KC1(n+1) + CASIN(n+4)$$

**FIGURE 2. 3 X 3 MATRIX MULTIPLIER — MODE 00**

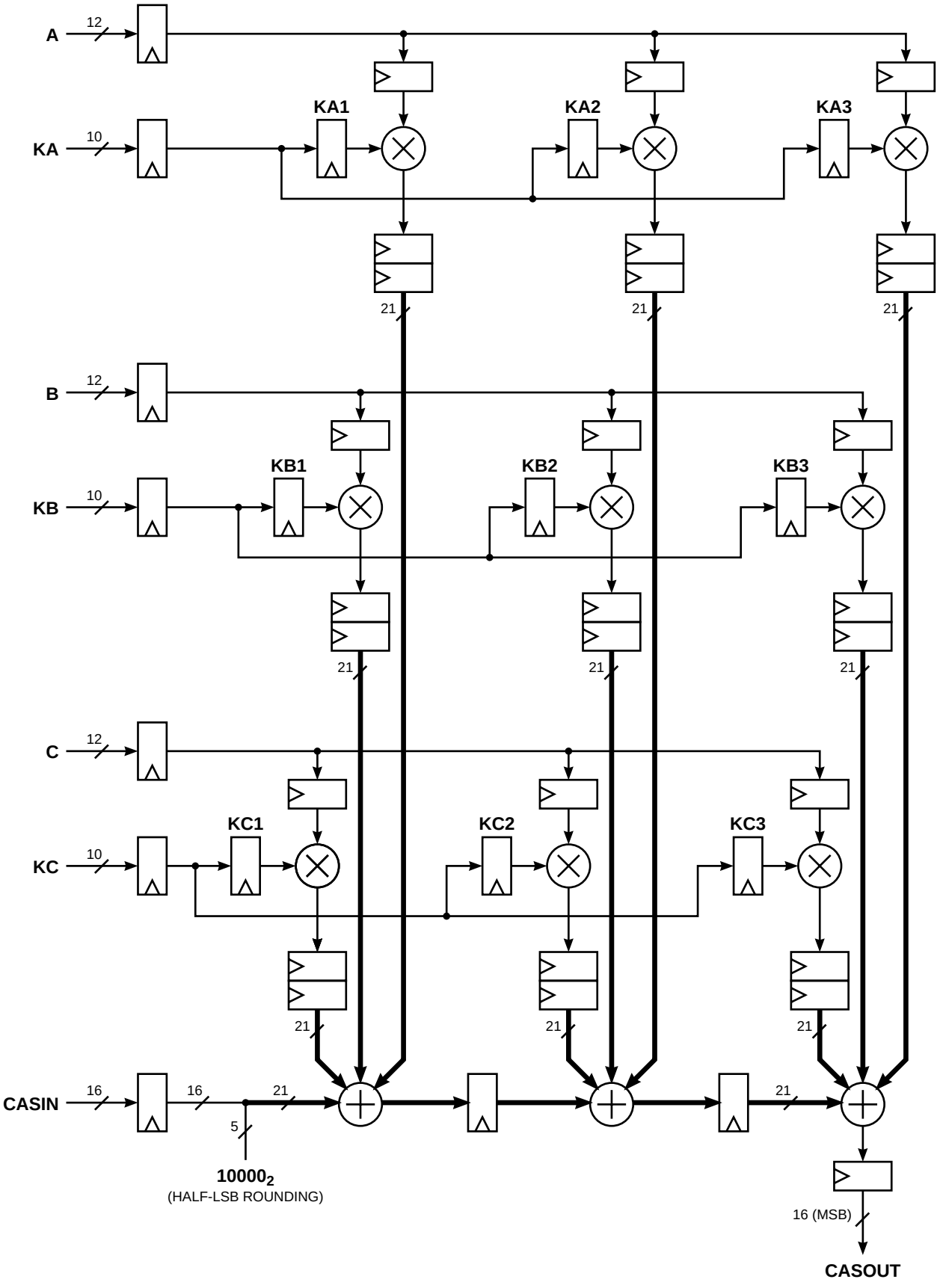


## FIGURE 3. 9-TAP FIR FILTER — MODE 01

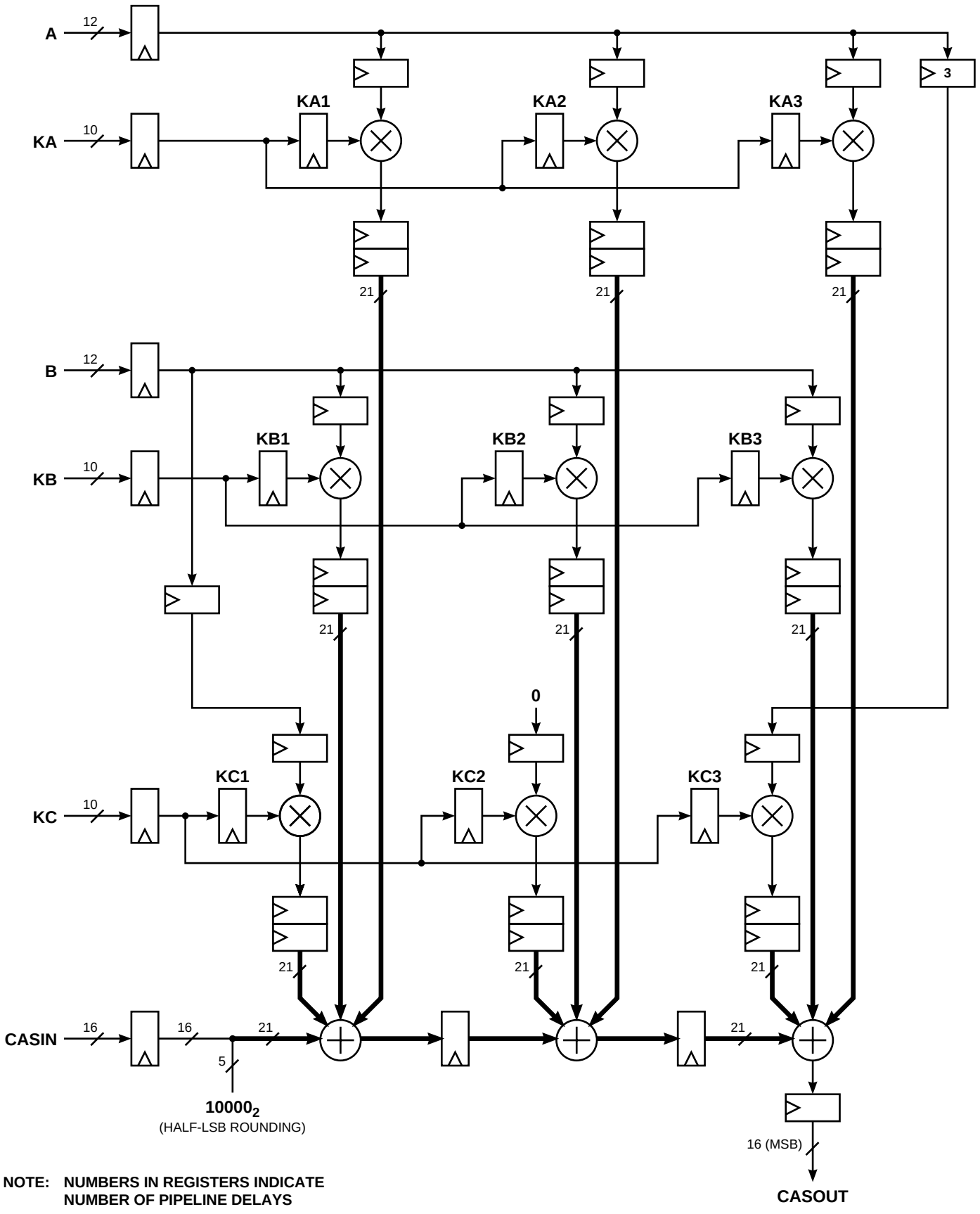



**NOTE: NUMBERS IN REGISTERS INDICATE NUMBER OF PIPELINE DELAYS**

## FIGURE 4. 3 x 3-PIXEL CONVOLVER — MODE 10



## FIGURE 5. 4 x 2-PIXEL CONVOLVER — MODE 11



## MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
**V**CC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

## OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

| Mode | **Temperature Range** (Ambient) | **Supply Voltage** |
|---|---|---|
| Active Operation, Commercial | 0°C to +70°C | 4.75 V ≤ **V**CC ≤ 5.25 V |
| Active Operation, Military | –55°C to +125°C | 4.50 V ≤ **V**CC ≤ 5.50 V |

## ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **V**OH | Output High Voltage | **V**cc = Min., **I**OH = –2.0 mA | 2.4 | | | V |
| **V**OL | Output Low Voltage | **V**cc = Min., **I**OL = 4.0 mA | | | 0.4 | V |
| **V**IH | Input High Voltage | | 2.0 | | **V**CC | V |
| **V**IL | Input Low Voltage | (Note 3) | 0.0 | | 0.8 | V |
| **I**IX | Input Current | Ground ≤ **V**IN ≤ **V**CC (Note 12) | | | ±10 | µA |
| **I**OZ | Output Leakage Current | (Note 12) | | | ±40 | µA |
| **I**CC1 | **V**CC Current, Dynamic | (Notes 5, 6) | | | 160 | mA |
| **I**CC2 | **V**CC Current, Quiescent | (Note 7) | | | 12 | mA |
| **C**IN | Input Capacitance | **T**A = 25°C, f = 1 MHz | | | 10 | pF |
| **C**OUT | Output Capacitance | **T**A = 25°C, f = 1 MHz | | | 10 | pF |

## SWITCHING CHARACTERISTICS

### COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

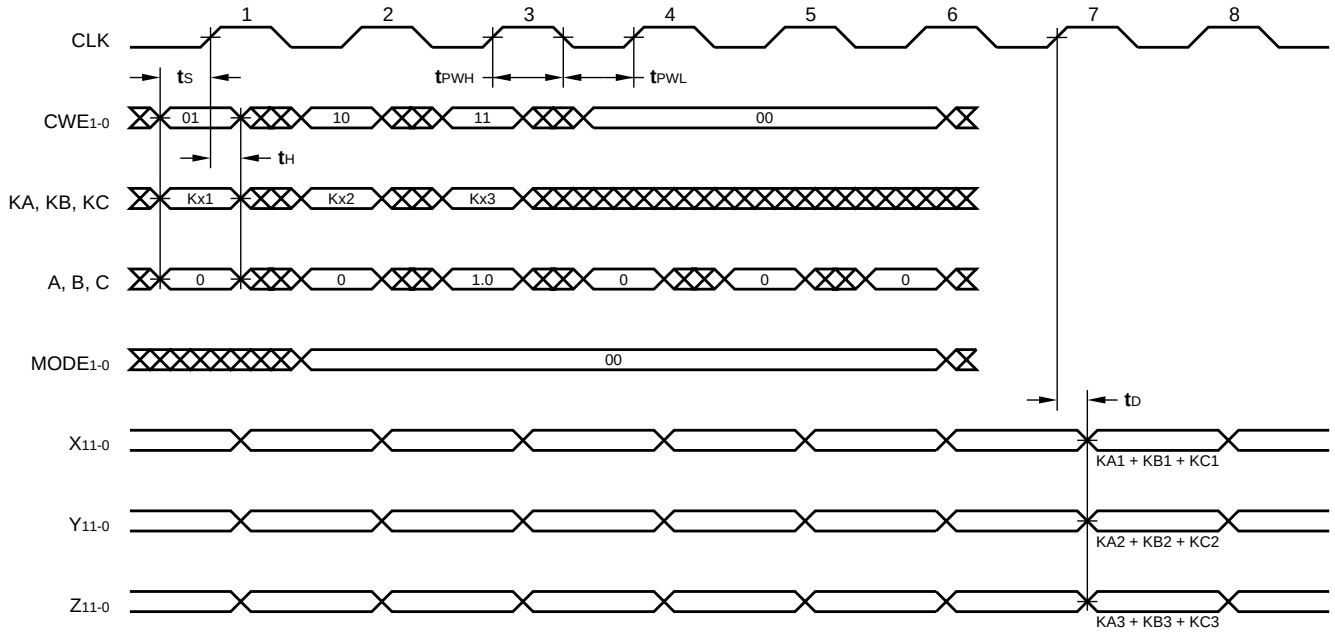
| | | LF2250– | | | | | |
|---|---|---|---|---|---|---|---|
| | | 33* | | 25 | | 20 | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max |
| $t_{CYC}$ | Cycle Time | 33 | | 25 | | 20 | |
| $t_{PWL}$ | Clock Pulse Width Low | 15 | | 10 | | 6 | |
| $t_{PWH}$ | Clock Pulse Width High | 10 | | 10 | | 8 | |
| $t_S$ | Input Setup Time | 8 | | 6 | | 6 | |
| $t_H$ | Input Hold Time | 0 | | 0 | | 0 | |
| $t_D$ | Output Delay | | 18 | | 16 | | 15 |

### MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

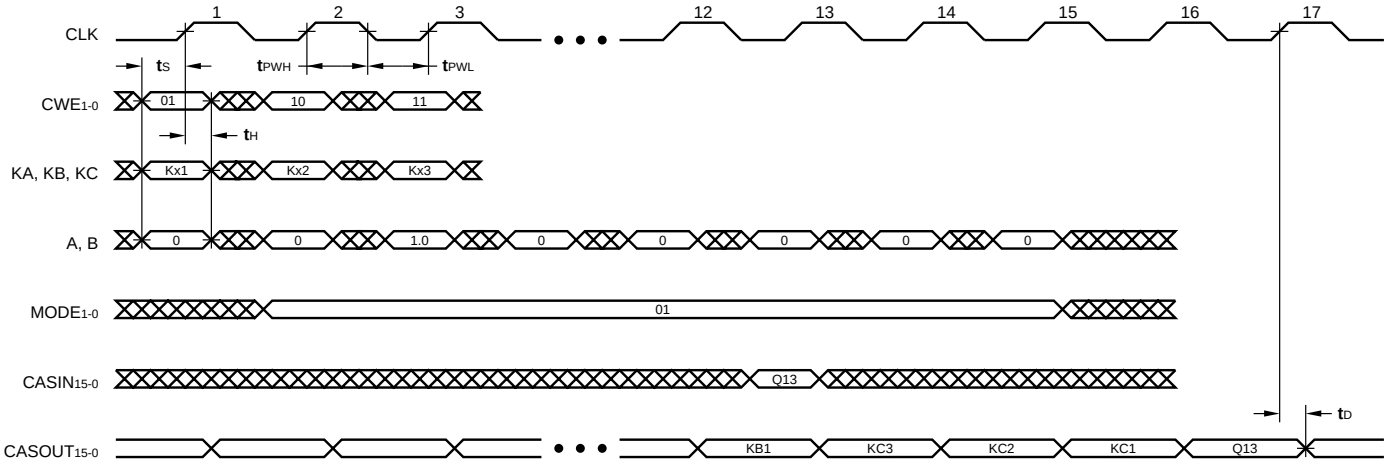
| | | LF2250– | | | |
|---|---|---|---|---|---|
| | | 33* | | 25* | |
| Symbol | Parameter | Min | Max | Min | Max |
| $t_{CYC}$ | Cycle Time | 33 | | 25 | |
| $t_{PWL}$ | Clock Pulse Width Low | 15 | | 10 | |
| $t_{PWH}$ | Clock Pulse Width High | 10 | | 10 | |
| $t_S$ | Input Setup Time | 12 | | 9 | |
| $t_H$ | Input Hold Time | 2 | | 2 | |
| $t_D$ | Output Delay | | 25 | | 20 |

*DISCONTINUED SPEED GRADE

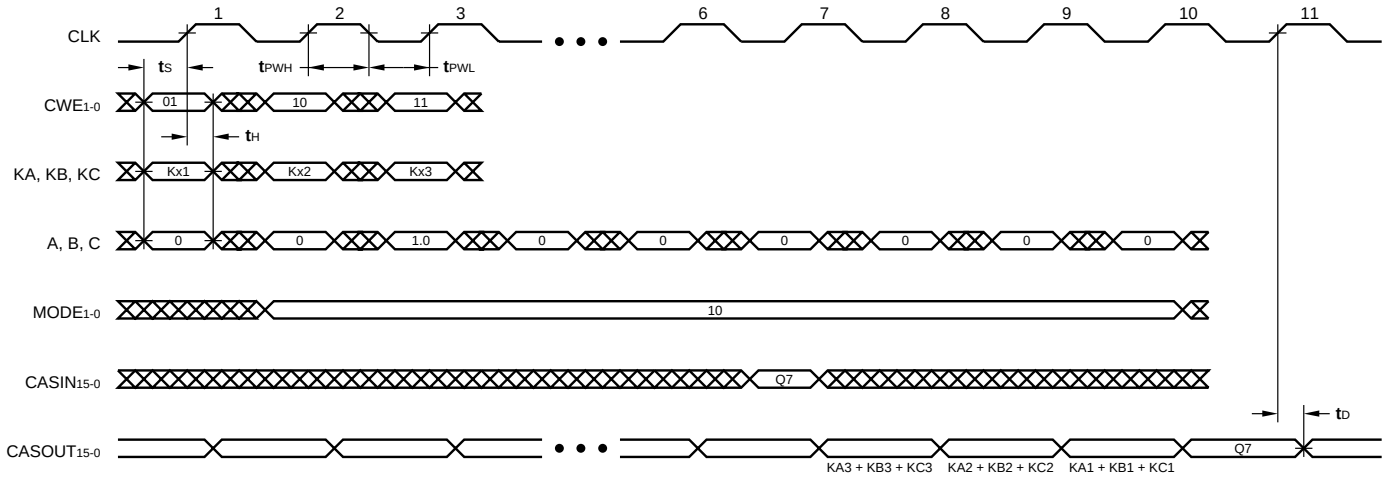
## SWITCHING WAVEFORMS: 3 x 3 MATRIX MULTIPLIER — MODE 00



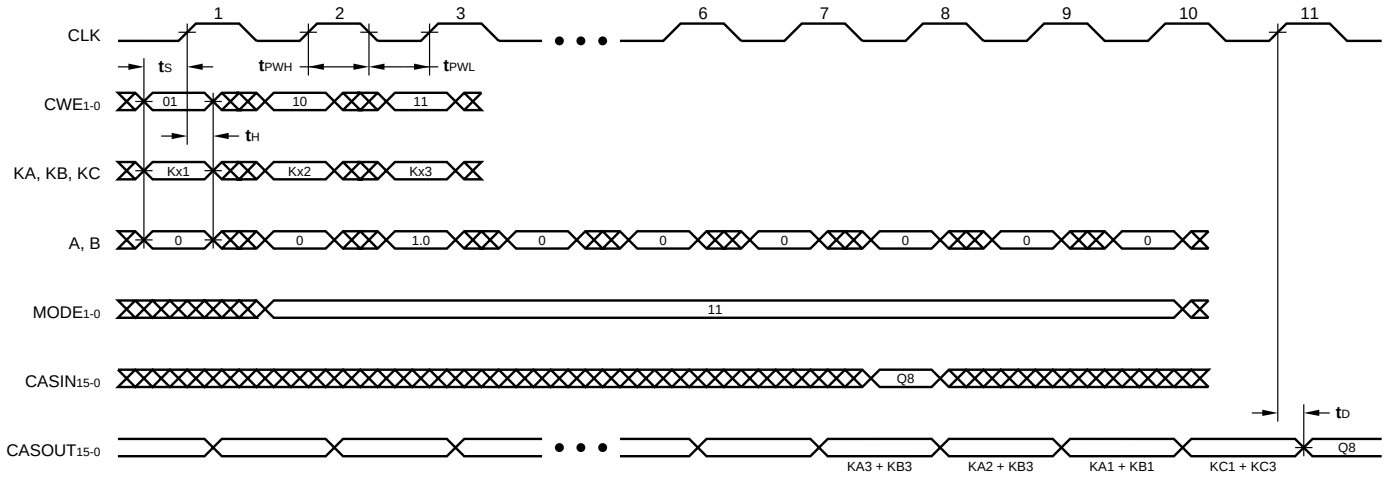

## SWITCHING WAVEFORMS: 9-TAP FIR FILTER — MODE 01



## Switching Waveforms: 3 x 3-Pixel Convolver — Mode 10




## Switching Waveforms: 4 x 2-Pixel Convolver — Mode 11



## NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above $V_{CC}$ will be clamped beginning at –0.6 V and $V_{CC}$ + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of $V_{CC}$ or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except $t_{DIS}$ test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified $I_{OH}$ and $I_{OL}$ at an output voltage of $V_{OH}$ min and $V_{OL}$ max respectively. Alternatively, a diode bridge with upper and lower current sources of $I_{OH}$ and $I_{OL}$ respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between $V_{CC}$ and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device $V_{CC}$ and the tester common, and device ground and tester common.

b. Ground and $V_{CC}$ supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and $V_{CC}$ noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the $t_{ENA}$ test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the $t_{DIS}$ test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, $V_{TH}$, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

**FIGURE A. OUTPUT LOADING CIRCUIT**

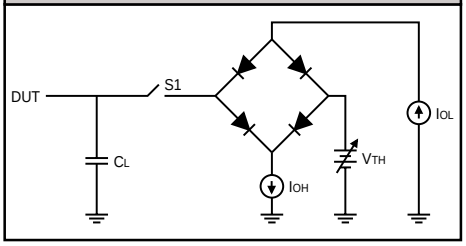
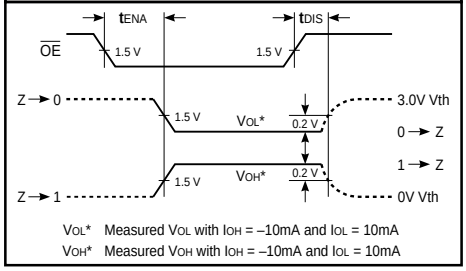
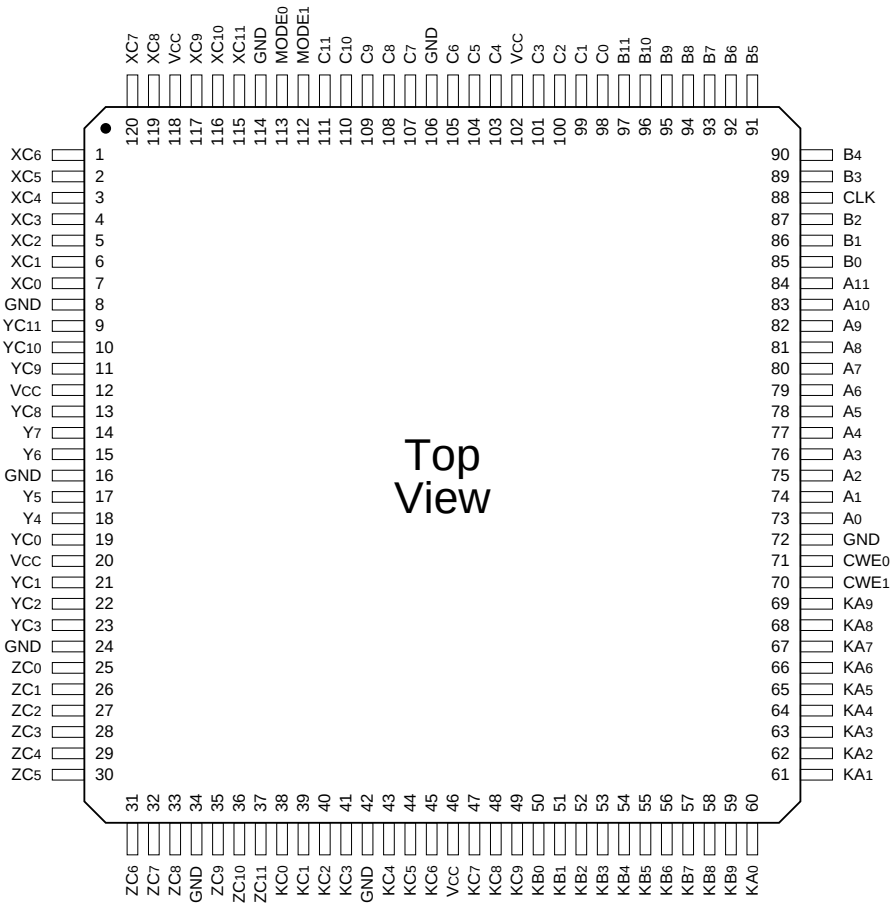



**FIGURE B. THRESHOLD LEVELS**



## ORDERING INFORMATION

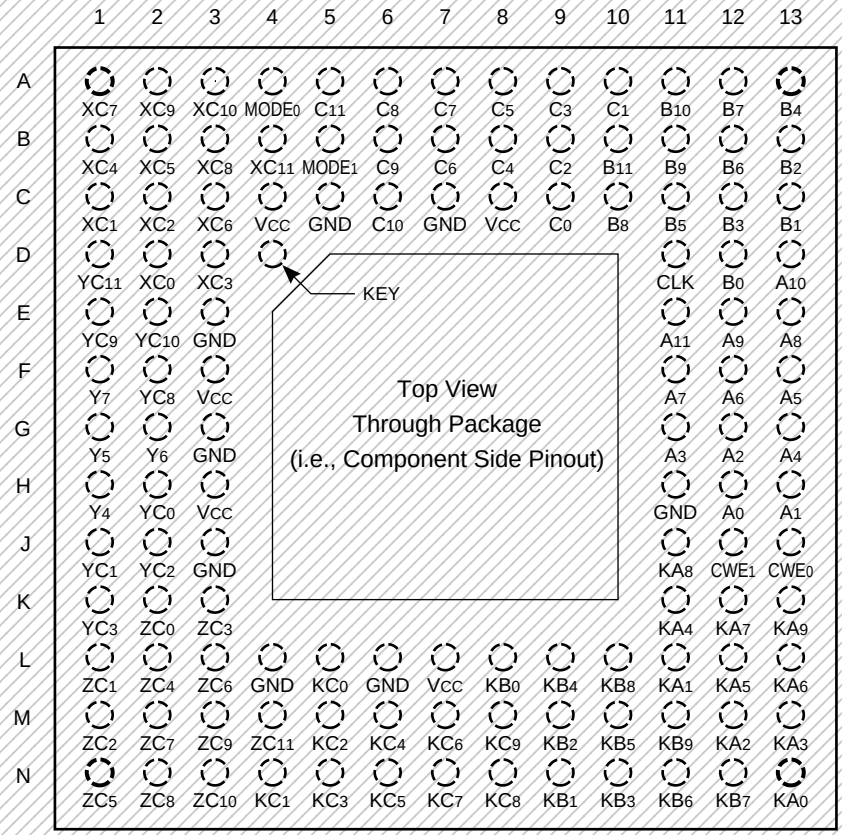
**120-pin**




| Speed | Plastic Quad Flatpack (Q1) |
|---|---|
| | **0°C to +70°C — COMMERCIAL SCREENING** |
| 25 ns | LF2250QC25 |
| 20 ns | LF2250QC20 |
| | **–40°C to +85°C — COMMERCIAL SCREENING** |
| | |
| | **–55°C to +125°C — MIL-STD-883 COMPLIANT** |
| | |

## ORDERING INFORMATION

**120-pin**




**Discontinued Package**

| Speed | Ceramic Pin Grid Array (G4) |
|---|---|
| | **0°C to +70°C — COMMERCIAL SCREENING** |
| | |
| | **–55°C to +125°C — COMMERCIAL SCREENING** |
| | |
| | **–55°C to +125°C — MIL-STD-883 COMPLIANT** |
| | |