

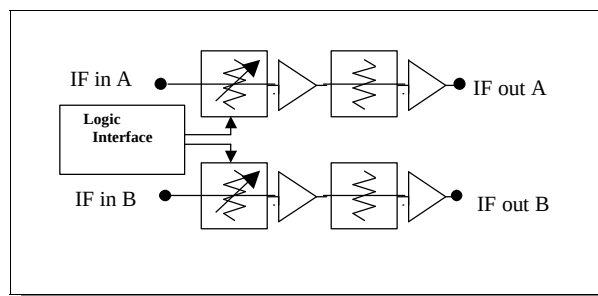
Features

- Attenuation: 0.5 dB steps to 31.5 dB
- 6 Bit Digital Gain Control
- CMOS Logic
- Serial Logic Interface
- Single Positive Voltage Supply
- 8 mm PBGA Package
- JEDEC MO-151 Footprint
- Single Package Solution for GSM,CDMA,PCS

Description

The M/A-COM AM55-0024 is a dual channel IF amplifier and digital attenuator packaged in a multi-layer multi-chip module (MCM). Gain control is via two separate serial logic interfaces. The part utilizes Plastic Ball Grid Array (PBGA) interconnect technology to achieve high circuit density and superior performance. This device is ideal for GSM/DCS/PCS digital base station applications where high dynamic range gain control functionality is required.

Functional Block Diagram



Absolute Maximum Ratings ¹

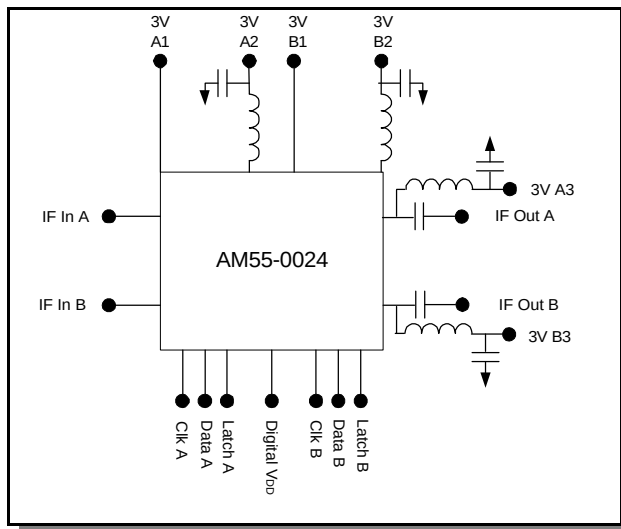
Parameter	Absolute Maximum
Input Power ²	+20 dBm
Operating Voltage ²	V _{DD} = +6 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage.
2. Ambient Temperature (T_A) = +25°C.

Electrical Specifications: T_A = 25°C, Z₀ = 50Ω ¹

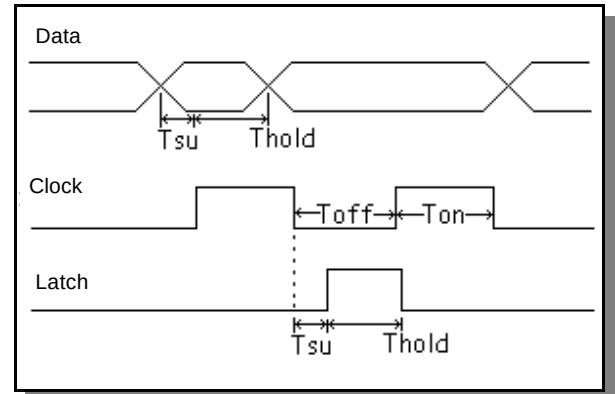
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	100 - 400 MHz	dB	19.5	21	22.5
Gain Control Range	100 - 400 MHz	dB		31.5	
Minimum Gain Control Step Size	100 - 400 MHz	dB		0.5	
Return Loss	100 - 400 MHz	dB	10	12	
Output IP ₃	100 - 400 MHz @ 5V	dBm		30	
Supply Voltage		V		3/5	
Supply Current	@ 3V / @ 5V	mA		300/400	
Switching Speed (50% TTL to 90% RF)		nS		50	
Isolation		dBc	50	60	
P1 dB		dBm	15	17.5	
Noise Figure	100 - 400 MHz	dB		4	

1. All measurements in a 50 Ohm system.

External Components ^{1, 2, 3}

1. All inductors are 470 nH
2. All Capacitors are 10000 pF
3. IF outputs must be supplied +3 Volts.

Component	Value
L	470 nH
C	10000 pF

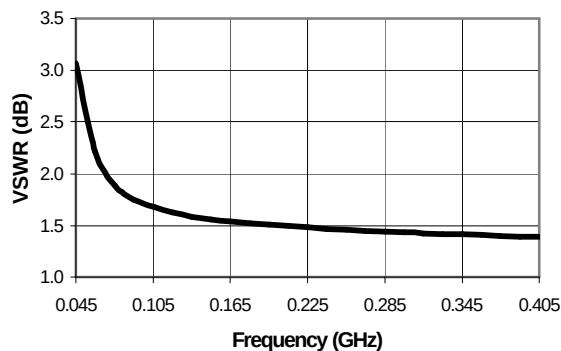
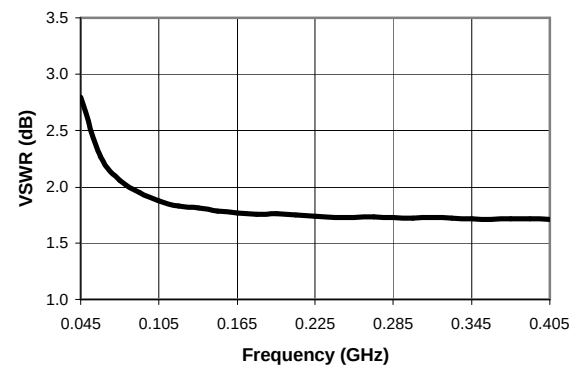
Clock Diagram ^{1, 2, 3, 4, 5}

1. Max Clock Speed = 40 MHz
2. $T_{on} = T_{off}$
3. $T_{su} > 3ns$
4. $T_{hold} > 7ns$
5. Data clocked in on rising clock edge

Serial Interface

Each channel in the AM55-0024 is independently controllable with a 3 wire serial interface: Clock, Data, and Latch Enable. These lines can be shared based on application requirements. The attenuator within the device is controlled with a 6 bit word, enabling the selection of 64 possible states. The highest gain state is '000000', and the lowest is '111111'. The sequence for shifting the data is as follows: Present data (MSB first), strobe clock, repeat until 6 bits have been presented and clocked, then strobe the latch enable line, which implements the state change.

Typical Performance Curves

Input V_{SWR} Output V_{SWR} 

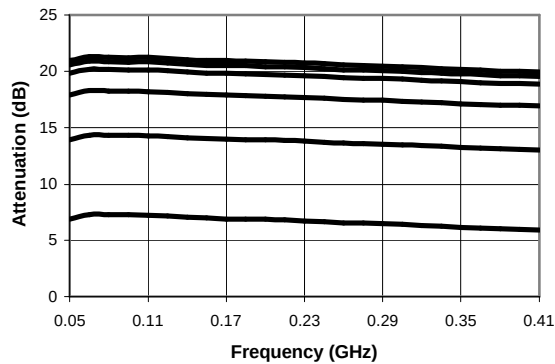
Specifications subject to change without notice.

- North America: Tel. (800) 366-2266
- Asia/Pacific: Tel. +81-44-844-8296, Fax +81-44-844-8298
- Europe: Tel. +44 (1344) 869 595, Fax +44 (1344) 300 020

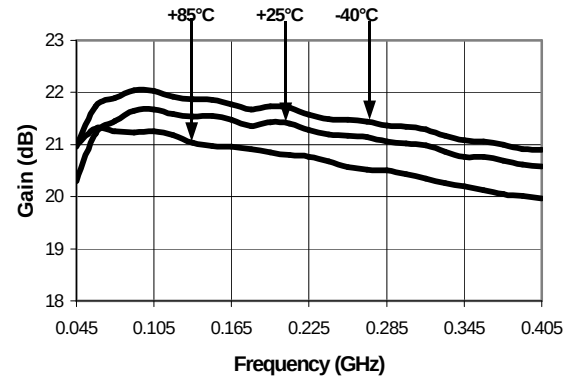
Visit www.macom.com for additional data sheets and product information.

Typical Performance Curves (Cont'd)

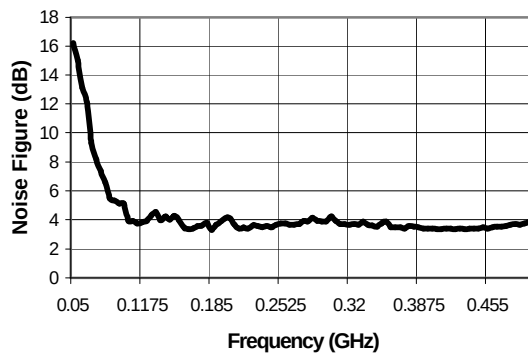
Attenuation (6 individual bits)



Gain



Noise Figure



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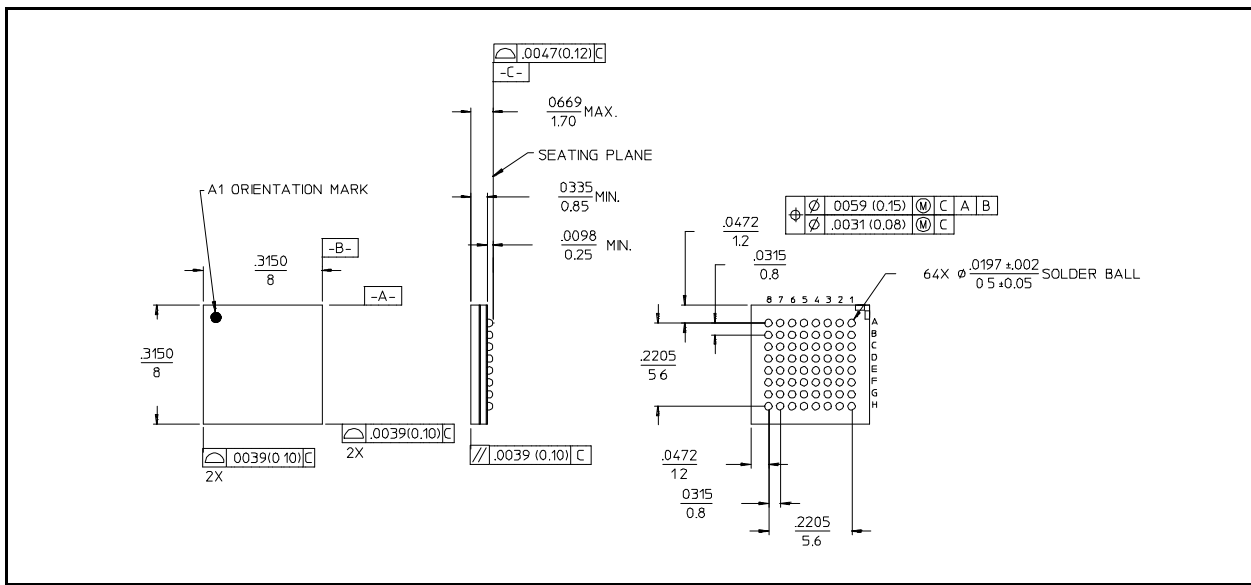
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8 mm PBGA



Pin Out

8	7	6	5	4	3	2	1	
+5V_A1	DAT_A	CLK_A	+5V_A2				RF_OUT_A	A
								B
RF_IN_A								C
LE_A								D
RF_IN_B								E
LE_B								F
CLK_B								G
DAT_B	+5V_B1			+5V_B2			RF_OUT_B	H

Ordering Information

Part Number	Package
AM55-0024	8-mm PBGA Package
AM55-0024TR	Forward Tape and Reel ¹
AM55-0024RTR	Reverse Tape and Reel

1. If specific reel size is required, consult factory for part number assignment.

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