19-1169; Rev 0; 12/96

EVALUATION KIT AVAILABLE

8-Bit, 500Msps Flash ADC

MAX1150

General Description

The MAX1150 is a parallel flash analog-to-digital converter (ADC) capable of digitizing full-scale (0V to -2V) inputs into 8-bit digital words at an update rate of 500Msps. The ECL-compatible outputs are demuxed into two separate output banks, each with differential data-ready outputs to ease the task of data capture. The MAX1150's wide input bandwidth and low capacitance eliminate the need for external track/hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to 1LSB. This device operates from a single -5.2V supply, with a nominal power dissipation of 5.5W.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1150AIZS	-20°C to +85°C	80 MQUAD
MAX1150BIZS	-20°C to +85°C	80 MQUAD

Features

- **1:2 Demuxed ECL-Compatible Outputs**
- **Wide Input Bandwidth: 900MHz**
- **Low Input Capacitance: 15pF**
- **Metastable Errors Reduced to 1LSB**
- **Single -5.2V Supply**

Applications

Digital Oscilloscopes

Data Acquisition

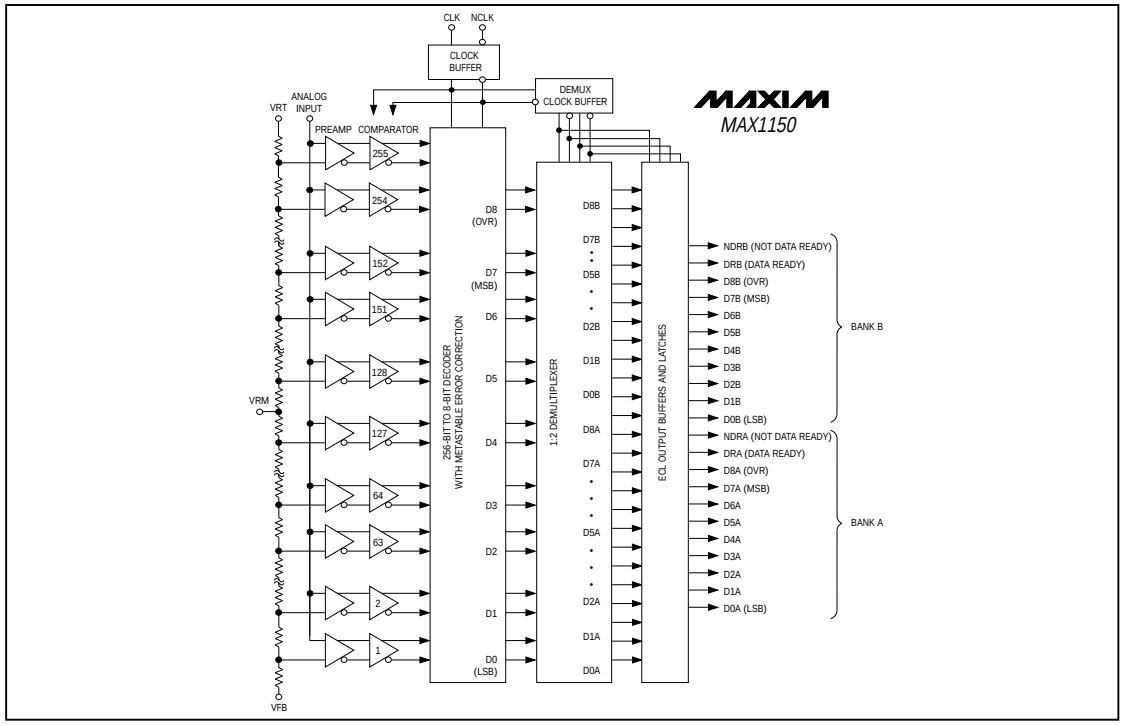
Transient-Capture Applications

Radar, EW, ECM

Direct RF/IF Downconversion

Pin Configuration appears on last page.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- Negative Supply Voltage (V_{EE} to GND) .....-7.0V to +0.5V
- Ground Voltage Differential .....-0.5V to +0.5V

Input Voltages
- Analog Input Voltage.....+0.5V to V_{EE}
- Reference Input Voltage .....+0.5V to V_{EE}
- Digital Input Voltage.....+0.5V to V_{EE}
- Reference Current (V_{RT} to V_{RB}) 35mA

Digital Output Current .....0mA to -28mA
Operating Temperature Range .....-20°C to +85°C
Case Temperature .....+125°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec) .....+300°C
Storage Temperature Range.....-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, V_{RB} = -2.00V, V_{RM} = -1.00V, V_{RT} = 0.00V, f_{CLK} = 500MHz, duty cycle = 50%, typical thermal impedance (θ_{JC}) = 4°C/W, $T_j = T_C = T_A$ = +25°C.) (Note 1)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1150A			MAX1150B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				8			8		Bits
DC ACCURACY									
Integral Nonlinearity	f_{CLK} = 100kHz	I	-1.0		1.0	-1.5		1.5	LSB
Differential Nonlinearity	f_{CLK} = 100kHz	I	-0.85		0.95	-0.95		1.5	LSB
No Missing Codes				Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN} = 0V	I		0.75	2.0		0.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance	Over full input range	V		15			15		pF
Input Bandwidth	Small signal	V		900			900		MHz
	Large signal	V		500			500		
Offset Error V_{RT}		IV	-30		30	-30		30	mV
Offset Error V_{RB}		IV	-30		30	-30		30	mV
Input Slew Rate		V		5			5		V/ns
REFERENCE INPUT									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
TIMING CHARACTERISTICS									
Maximum Sample Rate		I	500			500			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
CLK to DATA READY Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
Clock to Data Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, V_{RB} = -2.00V, V_{RM} = -1.00V, V_{RT} = 0.00V, f_{CLK} = 500MHz, duty cycle = 50%, typical thermal impedance (θ_{JC}) = 4°C/W, $T_j = T_C = T_A$ = +25°C.) (Note 1)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1150A			MAX1150B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC PERFORMANCE									
Signal-to-Noise Ratio (without harmonics)	f_{IN} = 50MHz	I	47			45			dB
	f_{IN} = 250MHz	I	44			42			
Total Harmonic Distortion	f_{IN} = 50MHz	I	-46			-44			dBc
	f_{IN} = 250MHz	I	-38			-36			
Signal-to-Noise and Distortion	f_{IN} = 50MHz	I	43			41			dB
	f_{IN} = 250MHz	I	37			35			
Spurious-Free Dynamic Range	f_{IN} = 50MHz	I	49			44			dB
	f_{IN} = 250MHz	I	41			36			
DIGITAL INPUTS									
Input High Voltage (CLK, NCLK)		I	-1.1	-0.7		-1.1	-0.7		V
Input Low Voltage (CLK, NCLK)		I		-1.8	-1.5		-1.8	-1.5	V
Clock Pulse Width High (t_{PWH})		I	1.0	0.67		1.0	0.67		ns
Clock Pulse Width Low (t_{PWL})		I	1.0	0.67		1.0	0.67		ns
Clock Synchronous Input Currents		V		2			2		µA
DIGITAL OUTPUTS									
Logic "1" Voltage		I	-1.1	-0.9		-1.1	-0.9		V
Logic "0" Voltage		I		-1.8	-1.5		-1.8	-1.5	V
POWER-SUPPLY REQUIREMENTS									
Supply Voltage (V_{EE})		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Supply Current (I_{EE})		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Note 1: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device test actually performed during production and Quality Assurance inspection. Unless otherwise noted, all tests are pulsed tests; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	D2B, D3B, D4B	Data Output Bank, Bits 2, 3, and 4
4, 5, 19, 20, 22, 23, 27, 28, 38, 39, 40, 46, 47, 49, 60, 67, 79	V_{EE}	Negative Supply, nominally -5.2V
6	D5B	Data Output Bank B, Bit 5
7, 9, 11, 54, 56, 58, 69, 71, 73, 75, 77	DGND	Digital Ground
8	D6B	Data Output Bank B, Bit 6
10	D7B	Data Output Bank B, Bit 7 (MSB)
12	D8B	Data Output Bank B, Bit 8 (OVR)
13, 14, 31, 34, 41, 63, 64	N.C.	No Connection. Not internally connected.
15–18, 25, 26, 29, 30, 36, 37, 44, 45, 51, 52	AGND	Analog Ground
21	VRBF	Reference-Voltage Force Bottom
24	VRBS	Reference-Voltage Sense Bottom
32, 33	VIN	Analog Input Voltage. Can be either voltage or sense.
35	VRM	Reference-Voltage Middle, nominally -1V
42	VRTF	Reference-Voltage Force Top
43	VRTS	Reference-Voltage Sense Top
48	NCLK	Inverse Clock Input
50	CLK	Clock Input
53	DRA	Data Ready Bank A
55	NDRA	Not Data Ready Bank A
57	D0A	Data Output Bank A, Bit 0 (LSB)
59, 61, 62, 65, 66, 68	D1A–D6A	Data Output Bank A, Bits 1–6
70	D7A	Data Output Bank A, Bit 7 (MSB)
72	D8A	Data Output Bank A, Bit 8 (OVR)
74	NDRB	Not Data Ready Bank B
76	DRB	Data Ready Bank B
78	D0B	Data Output Bank B, Bit 0 (LSB)
80	D1B	Data Output Bank B, Bit 1

Detailed Description

The MAX1150 is one of the fastest monolithic, 8-bit, parallel, flash analog-to-digital converters (ADCs) available today. The nominal conversion rate is 500Msps, and the analog bandwidth is in excess of 900MHz. A major advance over previous flash converters is the inclusion of 255 input preamplifiers between the reference ladder and input comparators (see *Functional Diagram*). This not only reduces clock transient kickback to the input and reference ladder, but also reduces the effect of the input signal's dynamic state on the input comparators' latching characteristics. The preamplifiers act as buffers to stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges, making the part easier to drive than previous flash converters. The preamplifiers also add a gain of +2 to the input signal, so that each comparator has a wider overdrive or threshold range to trip into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The MAX1150 has true differential analog and digital data paths from the preamplifiers to the output buffers (current-mode logic) for reducing potential missing codes while rejecting common-mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The device's output drive capability can provide full ECL swings into 50Ω loads.

Typical Interface Circuit

The circuit of Figure 1 shows a method of achieving the least error by correcting for integral linearity, input-induced distortion, and power- supply/ground noise. This is achieved with the use of external reference-ladder tap connections, an input buffer, and supply decoupling. Contact the factory for the MAX1150/MAX1151 evaluation kit manual, which contains more details on interfacing the MAX1150. The function of each pin and external connections to other components are described in the following sections.

V_{EE}, AGND, DGND

VEE is the supply pin with AGND as ground for the device. The power-supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 1µF tantalum can also be used for low-frequency suppression. DGND is the ground for the ECL outputs, and should be referenced to the output pulldown voltage and appropriately bypassed, as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense, while the other is used for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The MAX1150 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew-rate distortion.

CLK, NCLK (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50%, to avoid causing larger second harmonics. If this is not important to the intended application, duty cycles other than 50% may be used.

D0 to D8, DR, NDR (A and B)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 130Ω to 1kΩ loads. All digital outputs are gray code, with the coding as shown in Table 1.

Table 1. Output Coding

V_{IN} (V)	D8	D7 . . . D0
0	1	10000000 10000001 10000011 • • •
-0.5	0	10100001 10100000 11100000 • • •
-1.0	0	11000001 11000000 01000000 • • •
-1.5	0	01100001 01100000 00100000 • • •
-2.0	0	00000011 00000001 00000000

VRBF, VRBS, VRTF, VRTS, VRM (Reference Inputs)

There are two reference inputs and one external reference voltage tap. These are -2V (VRB force and sense), mid-tap (VRM), and AGND (VRT force and sense). The reference pins and tap can be driven by op amps (as shown in Figure 1), or VRM can be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression, if desired.

Thermal Management

The typical thermal impedance has (θ_{CA}) for the MQUAD package been measured at θ_{CA} = 17°C/W, in still air with no heatsink.

To ensure rated performance, we highly recommend using this device with a heatsink that can provide adequate air flow. We have found that a Thermalloy 17846 heatsink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application-specific conditions should be taken into account to ensure that the device is properly heat sinked.

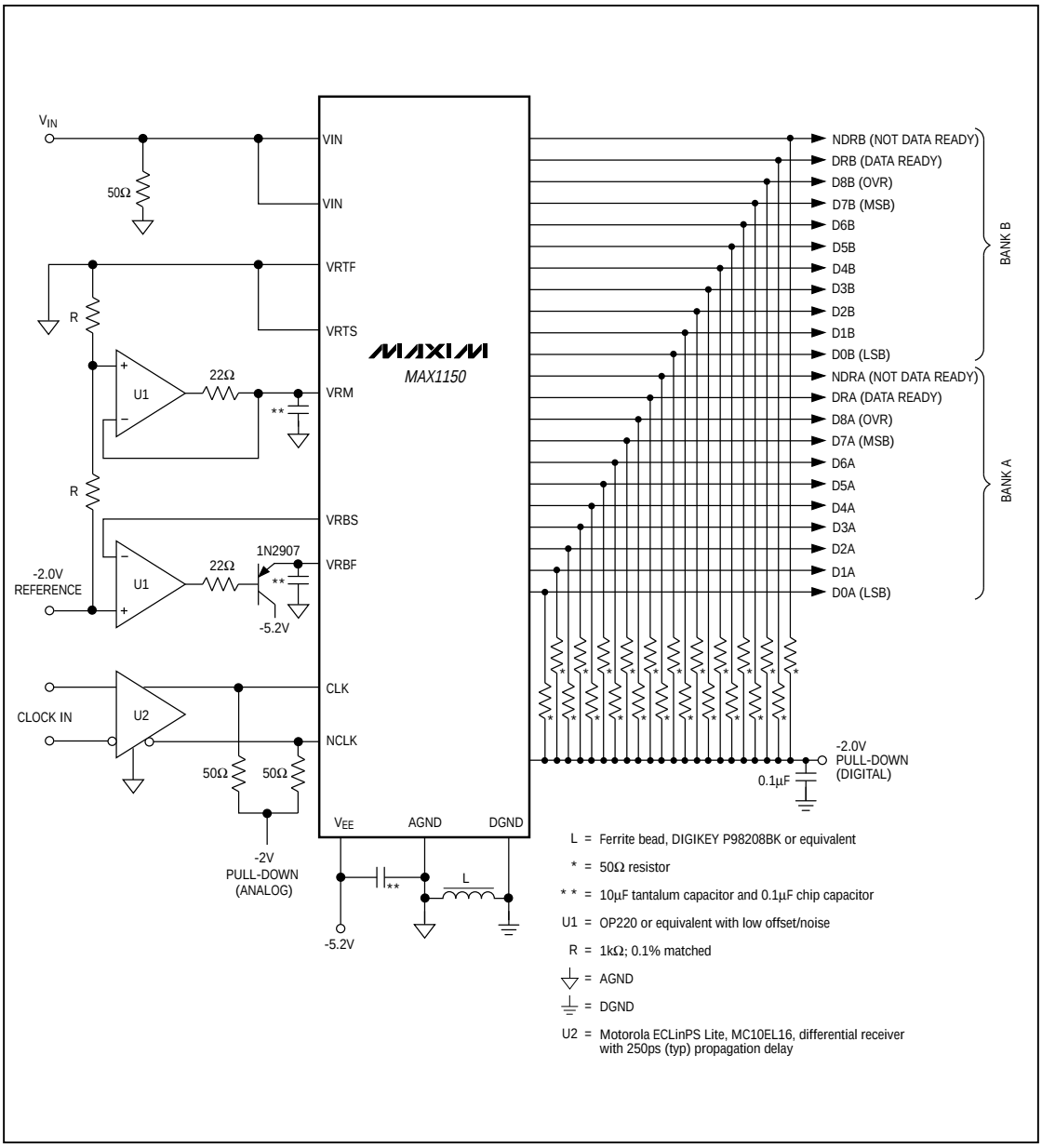


Figure 1. Typical Interface Circuit

Operation

The MAX1150 has 255 preamplifier/comparator pairs; each is supplied with the voltage from VRT to VRB, divided equally by the resistive ladder as shown in the *Functional Diagram.* This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches that are enabled (track) when the clock changes from high to low. From here, the output of the latches is coded into six LSBs from four columns, and four columns are coded into two MSBs. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

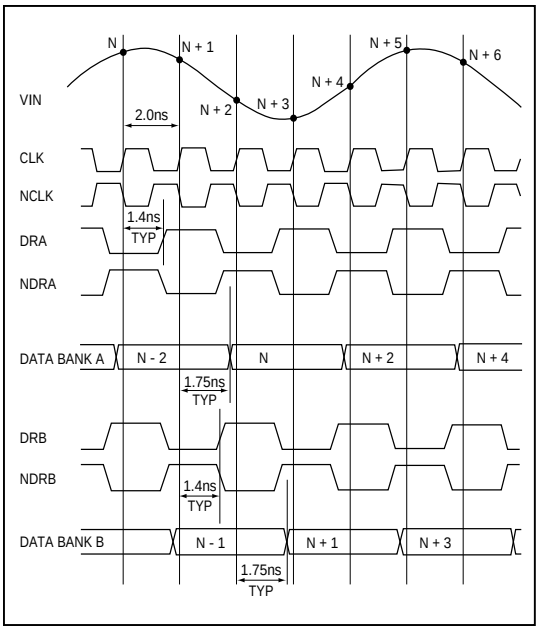


Figure 2. Timing Diagram

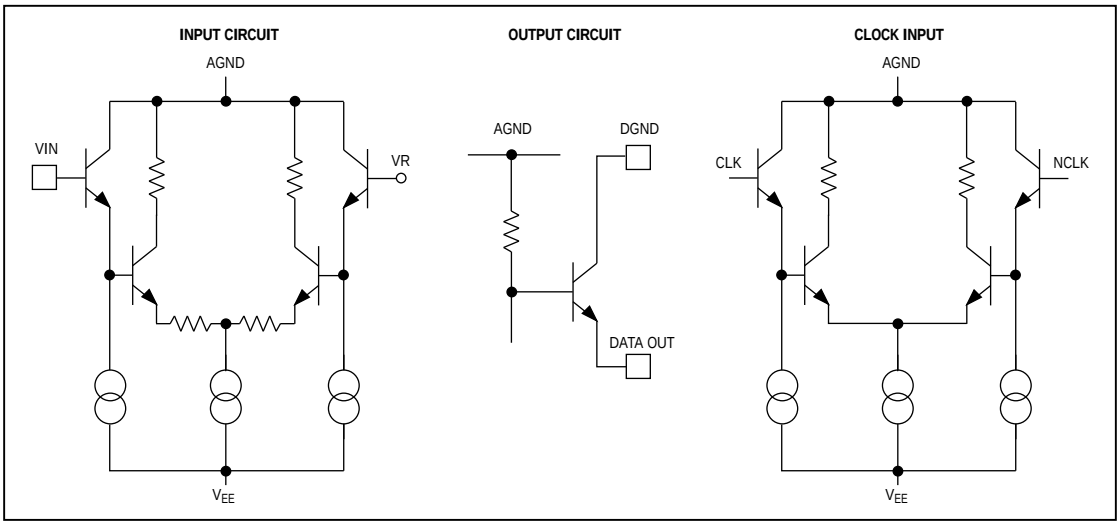
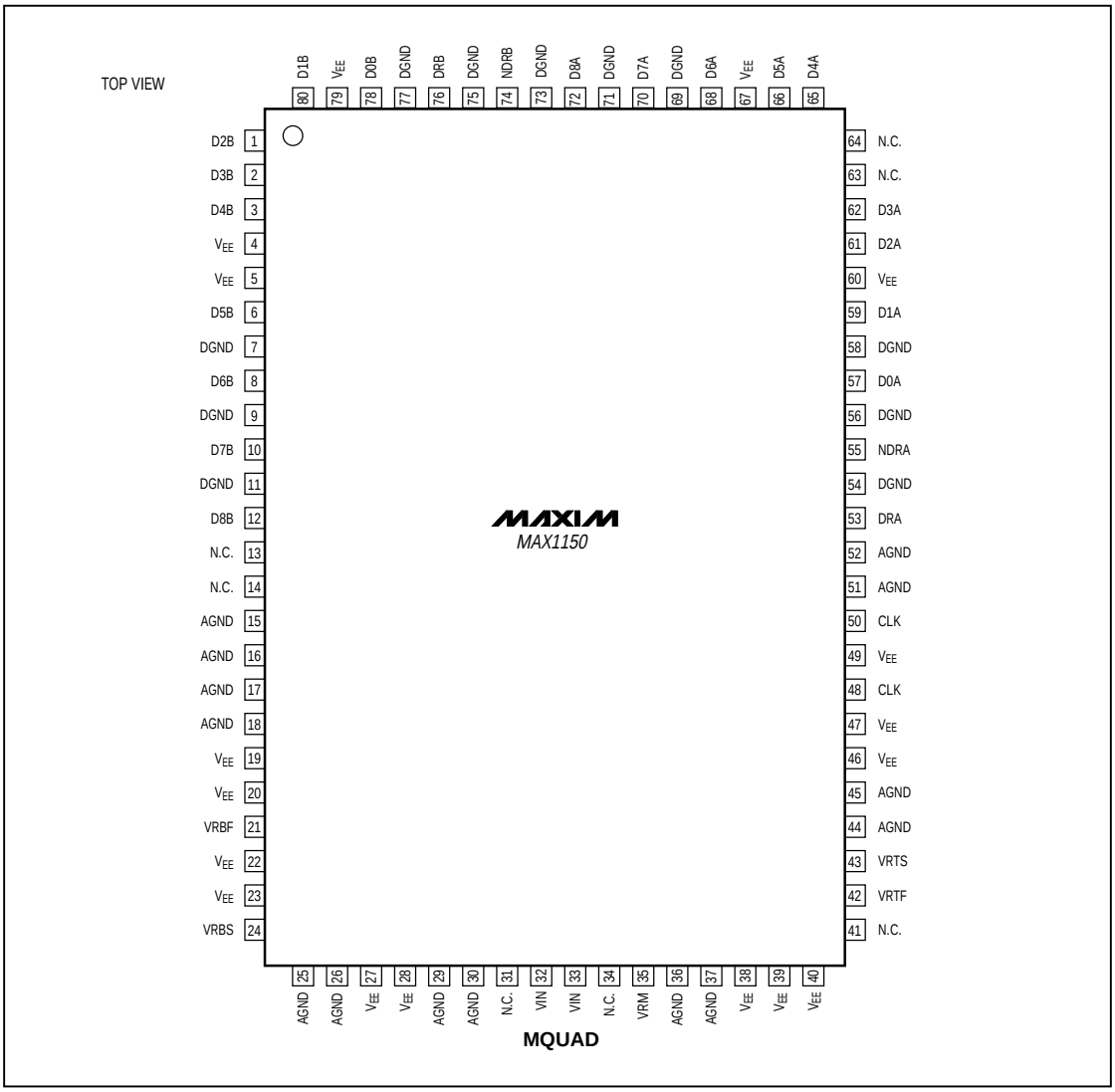


Figure 3. Subcircuit Schematics

Pin Configuration



MQUAD